

Invited: An Active Filter Balun and Frequency Doubler for Parametric Phase Noise Reduction Systems

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Abstract—This paper introduces an active filter balun and frequency doubler intended for an on-chip parametric phase noise reduction system. The 2.4 GHz balun is designed with inductor-capacitor (LC) tanks to provide narrowband filtering. This architecture also leads to low amplitude and phase errors of the differential outputs by relying on the matching of passive devices in the two branches. The frequency doubler utilizes a push-push structure to enhance the second harmonic at its output. An analysis has been completed for optimization of its performance and to identify design tradeoffs. Tuning varactors have been included in the design to alleviate the deviation of the resonance frequency of the LC tanks in process corners. The balun and doubler circuits were designed in a standard 65 nm CMOS process with a 0.6V power supply, consuming 450 μ W. According to simulations, the active filter balun has a 1.2 degree phase mismatch and a 1.3% amplitude mismatch in the typical corner, and respective errors less than -3 to 4 degrees and -2% to 3% across corner and mismatch simulations. The doubler is able to provide a signal with its highest harmonic at 40 dB below the desired 4.8 GHz output component.

Keywords — Active balun, frequency doubler, phase noise reduction system, parametric circuits, radio frequency circuits.

I. INTRODUCTION

Receiver architectures with radio frequency (RF) analog front-ends using either direct conversion or a low intermediate frequency are commonly found in wearable and implantable electronic devices. Their design is accomplished with the generation of local oscillator (LO) signals. However, the phase noise produced by the oscillator proves to be a significant detriment to system performance. Recently, the nonlinear dynamics of parametric circuits have been successfully leveraged for phase noise reduction with discrete components on printed circuit boards (PCB) [1]-[3]. These systems contain a parametric frequency divider (PFD) in a feedback loop. When the system is in a steady state, the use of the feedback topology allows operating the PFD around special operating conditions (i.e., bifurcations) [4] such that it does not track the fast phase fluctuations in the input signal, hence reducing the phase noise. The aforementioned system design approach promises to be a formidable solution for reducing phase noise in integrated sub-6 GHz CMOS receivers and transmitters such as [5]-[10], and including those for medical implants [11]-[13]. Since the cores of parametric circuits are passive, they are generally suitable for low-power applications, such as for medical implants where the goal is to extend battery lifetime or to operate with harvested energy [14].

Measurements of a parametric phase noise filter (PFIL) on a PCB demonstrated phase noise reduction of 16 dB and 13 dB

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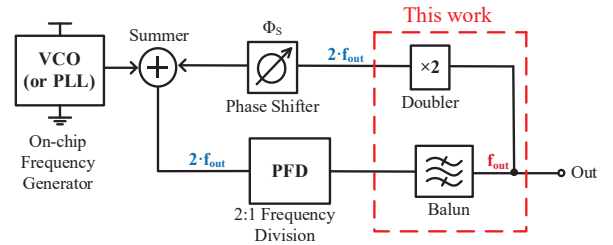


Fig. 1. Envisioned on-chip CMOS-compatible phase noise reduction system based on [3].

at 1 KHz and 10 KHz offsets from the carrier frequency [3]. With the goal of realizing the first on-chip CMOS-compatible implementation, Fig. 1 depicts a block diagram of such a phase noise reduction system. Here, the frequency of the voltage-controlled oscillator (VCO) or phase-locked loop (PLL) at the input is $f_{in} = 2 \cdot f_{out}$, where f_{out} denotes the output frequency of the system. For the system to operate correctly, there is a need for a frequency doubler [1]-[3], which in this case is placed within the feedback loop. It is also prudent for the system to provide a differential output to be used as an LO signal for up/down-conversion mixers.

This work includes the design of an active balun with embedded LC bandpass filtering. Furthermore, a frequency doubler is presented that is specifically designed for this application in mind. Its conversion gain and power consumption are optimized appropriately. Both circuits are meant to be used as components of an on-chip phase noise reduction system that is under development. This paper is organized as follows: Section II discusses the design of the proposed balun. Section III describes the frequency doubler design and optimization. Simulation results for both circuits designed in 65 nm CMOS technology are presented in Section IV. Finally, Section V provides the concluding remarks.

II. PROPOSED ACTIVE FILTER BALUN

In view of the fact that existing PFDs are usually single-ended, which can also ease signal processing complexity in some systems, a balun (balanced-to-unbalanced) circuit was designed to provide a differential output. When designing such circuits, both the amplitude and phase mismatches of the differential output signals prove to be of importance. With regards to the target application, other aspects worth considering are the magnitude and spectral characteristics of the PFD output [15]-[19], which is usually a large signal in magnitude and has considerable power present at higher order harmonics of its output frequency ($f_{out} = f_{in}/2$). This

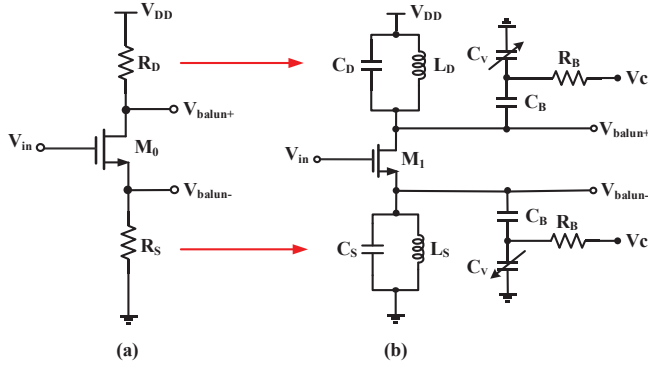


Fig. 2. Schematic of a conventional (a) and the proposed active filter balun (b).

necessitates that the chosen balun can operate with high-swing inputs and that it can provide filtering to suppress unwanted harmonics. Although there are viable on-chip active balun topologies available that are well-suited for small-signal operation [20]-[21], the need to provide filtering and effective operation with substantial input swings led to the construction of the balun topology introduced in this section.

Fig. 2(a) illustrates a conventional active balun [22]-[24]. The output is typically generated with resistors at the drain and source terminals of M_0 . If $R_D = R_S$, then the gate-to-source and gate-to-drain voltage gains are approximately equal. Nevertheless, at higher frequencies, the parasitic capacitances at the drain and source nodes limit the operational bandwidth and create phase imbalance. The use of resistors also requires substantial voltage headroom. Furthermore, as mentioned above, the output of the preceding PFD contains significant power at the output frequency harmonics. Hence, replacing the source/drain resistors with LC tanks that resonate at 2.4 GHz proves beneficial.

Fig. 2(b) depicts the proposed active filter balun. The signal at the input of the balun is expected to have a large amplitude around $1.2 V_{pp}$, which in turn will cause transistor M_1 to be in cutoff for part of the signal cycle. Accordingly, M_1 is intentionally biased to operate in class-B mode, such that M_1 only conducts for approximately half of the signal period, and the power consumption is greatly reduced compared to class-A operation. When transistor M_1 is conducting, its drain-to-source current flows from the power supply to ground, with the benefit that the same current flows through both LC tanks. Consequently, the mismatches between the differential outputs primarily depend on the mismatches between the passive devices, minimizing the impact of transistor parameter variations on output amplitude/phase mismatch. At the drain and source terminals of M_1 in Fig. 2(b) are a pair of identical LC tanks designed to resonate at the balun output frequency (i.e., 2.4 GHz in this design). The current that flows into both LC tank impedances is approximately the same and therefore produces negligible amplitude mismatch at the output. Another benefit of the use of LC tanks is that they provide filtering of signal components away from the resonance frequency. They also permit the reduction of the supply voltage (V_{DD}) to 0.6 V.

The parasitic capacitance of M_1 is critical when evaluating the resilience of this topology to static amplitude/phase mismatches: 1) the signal traverses uneven parasitics from the

input to each output respectively, which leads to a small inherent phase shift; 2) an AC current leakage flowing from V_{DD} occurs when parasitics are large, which can eventually result in gain mismatch. Therefore, the LC tank at the source terminal of M_1 has been intentionally designed with a slightly different resonance frequency. Its nominal frequency diverges by 100 Hz from the LC tank at the drain. Such deliberate introduction of asymmetry leads to minimization of the amplitude/phase mismatch. Inductors L_D and L_S both have a value of 1 nH, whereas C_S has a value of 2.5 pF while C_D has a value of 2.525 pF to compensate for the source-drain imbalance of M_1 . The resonance frequency of the LC tanks in process corners tends to be different from the typical corner case by $\pm 9.2\%$ according to simulations. Consequently, this effect leads to reduction of gain and filtering at the output. To compensate for process variations, the MOS varactors (C_V) in Fig. 2(b) were included to allow tuning for the realignment of the resonance frequency. The capacitance of these devices is controlled by the shared voltage V_C , where C_V ranges from 166 fF to 569 fF with simulated quality factors from 49 to 120. Multiple control schemes have been reported in order to generate such a tuning voltage (V_C) [25]-[27], which in filter applications typically involve on-chip amplitude monitoring within an automatic control loop.

III. PROPOSED FREQUENCY DOUBLER

In general, key characteristics-of-interest of frequency doublers are the conversion gain (CG) and the capability to produce an output with most of its power concentrated at $f_{out} = 2 \cdot f_{in}$. A suitable candidate for the target application is the push-push frequency doubler [28]-[29] because of its simplicity and satisfactory performance. Fig. 3 depicts the schematic of a proposed push-push doubler variant, where transistors M_1 and M_2 are identical. The input terminals of the doubler are connected at the outputs of the active filter balun described in Section II. The drain current of each transistor can be written as

$$i_{d1,2} \cong a_1 \cdot v_{gs} + a_2 \cdot v_{gs}^2 + a_3 \cdot v_{gs}^3 + a_4 \cdot v_{gs}^4, \quad (1)$$

where v_{gs} is the gate-to-source voltage of transistors M_1 and M_2 , a_1 is the transconductance gain; and $a_2, a_3, \dots$ are the non-linearity coefficients of the drain currents. With a differential input signal (180° phase difference between V_{in+} and V_{in-}), the odd harmonics of the drain currents of M_1 and M_2 are suppressed at the common output node [28]-[29], which contributes to a summed current at the common drain node as approximated below.

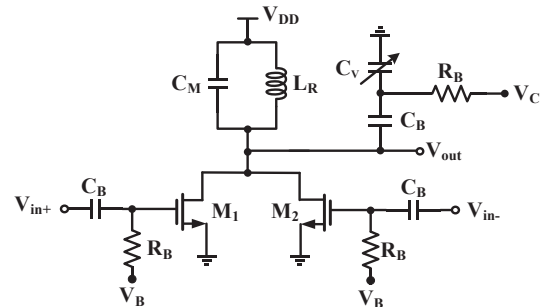


Fig. 3. Proposed frequency doubler with tunable resonance frequency using an on-chip varactor (C_V).

$$i_d \cong 2 \cdot a_2 \cdot v_{gs}^2 + 2 \cdot a_4 \cdot v_{gs}^4 \quad (2)$$

Thus, the current flowing at the output contains the desired second harmonic and other even-order harmonics, while the fundamental and third harmonic are cancelled under ideal conditions. One can use an LC tank resonating at $2 \cdot f_{out}$, in this case 4.8 GHz, to extract the second harmonic further through bandpass filtering, which suppresses unwanted spectral byproducts such as higher-order harmonics.

The conversion gain of the doubler in Fig. 3 can be obtained through small-signal analysis. Let i_{d1} , i_{d2} and r_{ds1} , r_{ds2} be the drain currents and drain-source resistances of M_1 , M_2 respectively; and Z_T the equivalent impedance of the LC tank at resonance. The parasitic capacitances at the output node can be absorbed as part of the tank at resonance. Assuming both transistors are identical: $i_{d1} = i_{d2}$, $r_{ds1} = r_{ds2} = r_{ds}$. Since Z_T , r_{ds1} and r_{ds2} are in parallel, we can denote their combination as

$$Z_{out} = Z_T // (r_{ds}/2) \quad (3)$$

We can now write the output voltage of the doubler as

$$V_{out} \cong -(2 \cdot a_2 \cdot v_{gs}^2 + 2 \cdot a_4 \cdot v_{gs}^4) \cdot Z_{out} \quad (4)$$

With a small-signal input of $v_{gs} = V_{amp} \cdot \cos(2\pi \cdot f_{in} \cdot t)$ at the gates of M_1 and M_2 , where V_{amp} is the AC amplitude, the conversion gain (CG) can be determined as

$$CG \cong -a_2 \cdot V_{amp} \cdot Z_{out} \quad (5)$$

According to equation (5), a higher input signal amplitude and larger 2nd-order nonlinearity coefficient (a_2) are necessary in order to increase the doubler conversion gain. Operating M_1 and M_2 in the subthreshold region with a higher g_m/I_d ratio can increase the ratios of a_2/a_1 and a_3/a_1 [30] while also improving power efficiency. However, imperfect cancellation of odd harmonics can occur due to finite phase error and amplitude mismatch at the balun outputs, which is further elaborated in the next section with simulation results.

The inductor L_R (1 nH) and the metal-insulator-metal (MIM) capacitor C_M (620 fF) in Fig. 3 are standard devices from the process design kit library. As mentioned in Section II, the resonance frequency of the tank changes with process corners, and in this case its nominal value deviates by $\pm 8.3\%$. For this reason, the same varactor-tuning scheme has been implemented for the frequency doubler as for the LC tanks in the balun, which shares the same control voltage (V_C).

IV. SIMULATION RESULTS

Circuit-level schematic simulations were carried out with foundry-supplied device models from a standard 65 nm CMOS technology using Cadence Spectre. A sine wave with a 1.2 V_{pp} amplitude and 2.4 GHz frequency has been used as the input of the active filter balun based on anticipated conditions in the target application. During the simulations, the balun circuit was loaded by connecting it to the frequency doubler. Fig. 4 displays the transient voltages of the differential balun outputs with a dashed line representing V_{balun-} and a continuous line for V_{balun+} , which have a phase mismatch ($\Delta\phi$) of 1.2° and an amplitude mismatch (ΔA) of 1.3% in the typical corner.

TABLE I: ACTIVE FILTER BALUN PHASE/AMPLITUDE MISMATCHES FOR PROCESS CORNERS

Process Corners	Slow	Typical	Fast
Phase Mismatch, $\Delta\phi$ (degrees)	-2.6	1.2	3.9
Amplitude Mismatch, ΔA (%)	-1.6	1.3	2.5
Control Voltage, V_C (Volts)	0.4	0.2	0.07

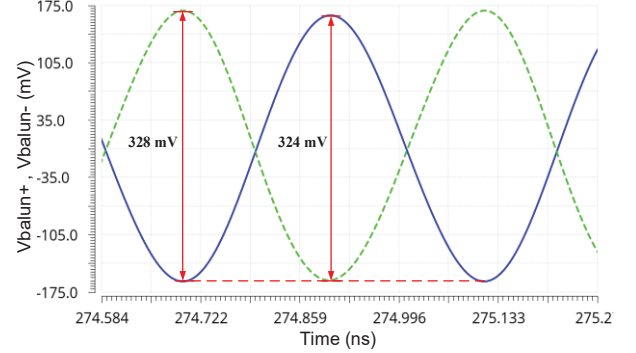


Fig. 4. Transient signals of the differential balun outputs V_{balun-} (dashed green line) and V_{balun+} (solid blue line).

Table I summarizes the phase mismatch ($\Delta\phi$), in degrees, and amplitude mismatch (ΔA), as percentage, of the active filter balun over corner simulations. The required control voltage (V_C) to tune the added varactors in each case is also listed. The phase mismatch indicates the deviation between the phase difference of the actual differential outputs and the ideal value of 180°. As mentioned in Section II, the resonance tanks at the drain and source terminals of M_1 in Fig. 2 can be slightly tuned to achieve a smaller phase mismatch at the cost of amplitude mismatch, and vice versa. In this case, optimizations were conducted using simulations to balance the phase and amplitude mismatches for increased spectral purity of the final doubler output signal rather than the balun output.

Fig. 5 to Fig. 7 depict the output spectra of the frequency doubler for the three process corners. It is evident that the 4.8 GHz harmonic is the most pronounced frequency component. As discussed in Section III, phase/amplitude mismatches lead to the residues of odd-order harmonics in addition to the even-order components of the approximation based on cancellations in equation (2). Furthermore, as exhibited in Table I, the phase and amplitude mismatches have their highest values in the fast corner. This is also evident in Fig. 7, where the odd harmonics are more noticeable than in the other two corner cases. Nevertheless, in all three cases there is enough margin for the target application, considering that all harmonics are at least 30 dB below the desired component at 4.8 GHz. Note that the above results were obtained with the varactors tuned using the shared control voltage V_C , in each case with the appropriate DC voltage for the required LC tank center frequencies, making it apparent how vital the tuning is. Using scaled inductor values and varactors that are multiples of a common unit capacitance helps in ensuring a robust suppression of undesirable spectral byproducts due to the finite amplitude/phase mismatches.

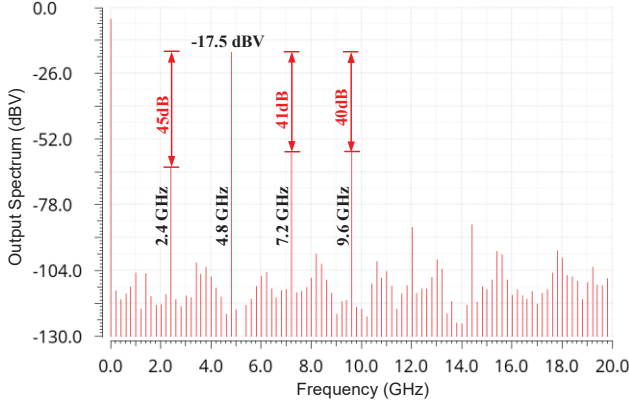


Fig. 5. Output spectrum of the frequency doubler: typical corner simulation with $V_C = 0.2$ V.

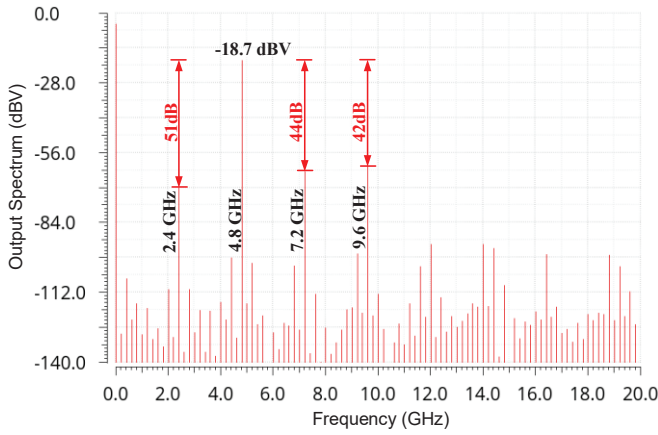


Fig. 6. Output spectrum of the frequency doubler: slow corner simulation with $V_C = 0.4$ V.

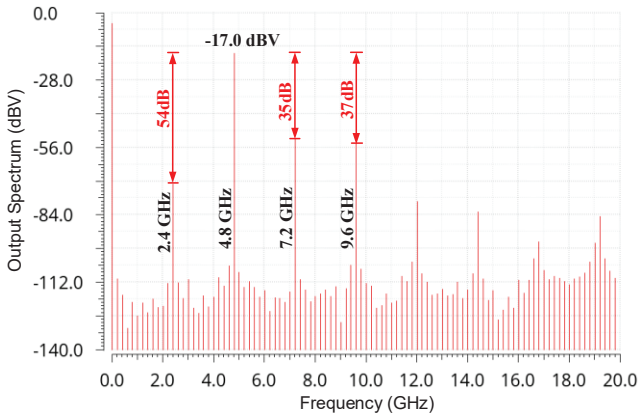


Fig. 7. Output spectrum of the frequency doubler: fast corner simulation with $V_C = 0.07$ V.

Monte Carlo simulations were conducted using statistical foundry-supplied device models for all active and passive devices. Fig. 8 and Fig. 9 display the histograms for the amplitude and phase mismatches of the active filter balun from simulation of 100 samples. The mean of the amplitude mismatch is 1.3%, and the standard deviation is 0.055%. For the phase mismatch, the mean and standard deviation are 1.2°

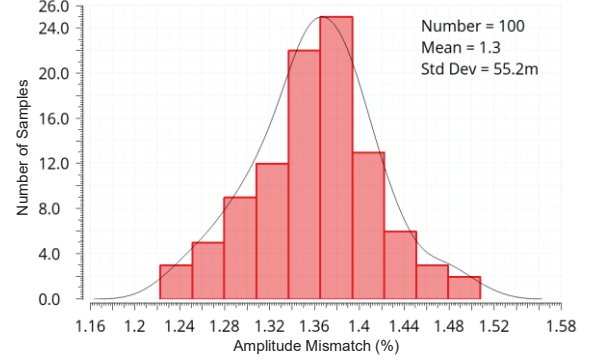


Fig. 8. Monte Carlo results for amplitude mismatch after 100 runs.

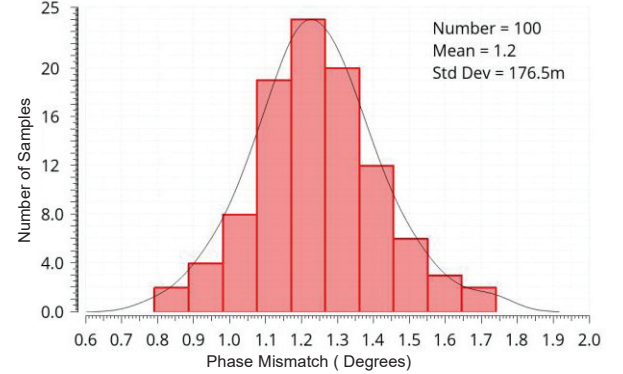


Fig. 9. Monte Carlo results for phase mismatch after 100 runs.

and 0.176° respectively. These results show that smaller variations are achieved compared to active baluns relying on the combination of transistors and resistors. As described in Section II, this is in part attributed by the same small-signal current flowing through both LC tanks in Fig. 2. Thus, the voltage variation at $V_{\text{balun}+}$ due to the variation of the current of M_1 is highly correlated to that at $V_{\text{balun}-}$. Furthermore, in [31] it was established that the mismatch between two inductors can be less than 1% even in the higher 20 GHz range. Similarly, in [32] it was demonstrated that the mismatches of metal-oxide-metal capacitors can be expected to be below 0.2%. These aspects are the foundation of the active filter balun's mismatch immunity.

V. CONCLUSION

This paper introduced an active filter balun and a frequency doubler for an on-chip parametric phase noise reduction system. Tuning varactors have been incorporated into both circuits to allow for compensation of process corner variations. The circuits were designed in 65 nm CMOS technology and simulated to evaluate their performance and suitability for the target application. The 2.4 GHz active filter balun achieves a 1.2° phase error and a 1.3% amplitude error. Furthermore, the doubler's 4.8 GHz output signal has high spectral purity while driven by the balun, and both circuits together consume $450 \mu\text{W}$ from a 0.6 V power supply. Monte Carlo simulations revealed that the circuit topologies are robust to device mismatches.

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