Digital Close-Loop Active Gate Driver for Static and Dynamic Current Sharing of Paralleled SiC MOSFETs

Liyang Du, *Student Member*, *IEEE*; Xia Du; Shuang Zhao, *Member*, *IEEE*; Yuqi Wei; Zhiqing Yang; Lijian Ding; H. Alan Mantooth, *Fellow*, *IEEE*

***Abstract*- SiC power devices have been extensively for the high-power density application scenarios. To increase the current rating, SiC devices are usually connected in parallel. However, the mismatching current brought by unbalanced electrical parameters can increase the current stress of a device and pose reliability concern of the converter system. Aiming at addressing the current imbalance for paralleled SiC devices, this paper reports the application of an improved active gate driver (AGD) on the paralleled SiC MOSFETs to address the current imbalance problems. The three-level driver voltage can minimize the overshoot voltage and current. The adjustable turn-on voltage and gate signal delay time can realize the current sharing of both static and dynamic process. Current sensors and a digital controller are utilized for close-loop control. The functionality of the proposed AGD is validated in continuous operating experiment.**

I. INTRODUCTION

Silicon carbide (SiC) semiconductor devices are approaching ideal switch due to their reduced switching loss and higher operating temperature which enable them to be extensively applied in the industry [1]. SiC MOSFETs are replacing silicon counterparts in the application scenarios such as electric vehicles, distributed energy generation, electronic devices, etc. [2]. For high-power conversion systems, multiple power devices are usually connected in parallel to increase the current rating such as grid-connected converter [3]. There are generally two paralleling conditions. A power module usually has multiple paralleled dies in the package while some power converters have a couple of paralleled discrete devices on the circuit board [4]. Therefore, device paralleling is a common solution for boosting the current rating.

However, the mismatched electrical parameters in the power loop can pose a current imbalance and increase the current stress of a device [5]. Generally, there are two types of current imbalance [6]: static imbalance due to unequal on-state resistance (R_{dson}) and dynamic imbalance resulting from the asynchronous switching transient process. The static imbalance can lead to mismatched conduction loss while the dynamic imbalance can cause mismatched switching loss and high overshoot current on a device. It should be noted that most power devices have self-balance capability due to the positive temperature coefficient [7]. However, for some high-voltage SiC devices, the temperature coefficient is negative in some temperature ranges which will be demonstrated in the following section. Both static and dynamic imbalance can result in unequal junction temperature, imbalanced current stress and finally raise long-term reliability concerns [5]. The application of SiC can aggravate the current imbalance due to its shorter switching transient time.

Reliable current sharing solutions for paralleling SiC power devices are needed to enhance the long-term reliability of the converter [8] [9] [10]. The state-of-the-art current sharing methodologies include the preselection of devices or dice [11], optimizing the package or circuit layout [12] [13], adding external passive components such as coupled inductors [14] and utilizing active gate driver (AGD) [15] to optimize the dynamic current distribution. Among the aforementioned four methodologies, AGD is drawing more attention in terms of adjustment flexibility and online control ability. It is widely used to improve the switching performance, such as slew rate control [3] [16] [17] [18], crosstalk suppression [19], switching loss and overshoot optimization [20] [21] [22], dynamic voltage balancing of series connected devices [23] and current balancing of paralleled devices [24] [25] [26]. The switching trajectory adjustment capability of AGD has been validated in multiple references [27] [28] [29]. Even though AGDs have advantages that enable them to be employed for the current sharing of paralleled MOSFETs, the following challenges hinder them to be widely applied in the industry:

a) Close-loop control. Most references that propose new AGD circuitries only show the slew rate adjustment capability while close-loop control is not implemented. The close-loop control is difficult since the switching slew rate is usually finished at the nanosecond level [23]. This is particularly challenging for SiC MOSFETs due to the higher switching speed and reduced parasitic inductances [30]. This requires both signal sensing and control system calculation to be finished in a couple of nanoseconds [3]. In [15] and [31], the dynamic current sharing is realized by synchronizing the current edge and current slope by feedback on the current information through the intrinsic parasitic inductances to CLPD. To realize high-speed close-loop control, some references select analog control which is based on the operational amplifier circuit [32] and high-speed comparators for timing control [16]. Compared with digital control, analog

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control is not flexible since it requires changing the hardware when debugging [18]. Furthermore, one critical motivation to apply close-loop control is to improve the robustness of current sharing regarding switch parameter drift and ambient coefficient variations, while the analog feedback loop is more vulnerable to those factors.

b) Implementation of full current sharing. Most AGD-based current sharing strategies focus on dynamic imbalance while static imbalance is neglected since most MOSFETs have positive temperature-dependent ON-state resistance. However, [33] reveals that self-balancing effect of MOSFETs is limited in some conditions. The static current mismatch cannot be completely eliminated by self-balancing effect. This will be elaborated in Section II.

Considering the aforementioned problem, this paper proposes a digital close-loop AGD for the current sharing of paralleled SiC MOSFETs based on the patented three-level AGD circuit in [22] and [31]. Compared with the other circuits, the proposed method has the following advantages:

a) True digital close-loop control. This paper demonstrates the implementation of close-loop control for AGD with a local DSP controller. Compared with the extensively applied CPLD/FPGA solutions, DSP controller integrates both high speed analog and digital functions, which allows a more compact design for AGD. Moreover, digital control enables the system debugging to be more flexible.

b) Implementation of full current sharing. The proposed AGD circuitry can compensate both static imbalance and dynamic imbalance. Via changing the driver voltage in normal ON state, it can change R_{dson} and static current distribution. Via adjusting the delay time of the gate signal, it can change the dynamic current stress, thus the dynamic imbalance can be suppressed. With the continuous driver voltage adjusting level, it can realize high adjustment resolution and improve the control accuracy.

c) Based on the circuit proposed in [22], the three-level driver voltage profile can effectively suppress the turn-off voltage overshoot which is beneficial for long-term reliability enhancement of the system.

Apart from the circuitry, this paper summarizes the challenge of paralleling SiC MOSFETs from the physical mechanism. The transfer function is derived for static/dynamic current adjustment, which can provide theoretical fundamentals for close-loop control optimization. The detailed design process of the high-frequency current sensor and implementation of high-speed signal sensing with the DSP controller is demonstrated. The proposed current sharing strategy is validated via an experimental study on a buck converter. The experimental results show that the proposed method has not only superior static and dynamic current sharing capability, but also great overshoot voltage mitigation functionality.

The other sections are organized in the following way: Section II presents the challenges of paralleling SiC MOSFETs. Section III introduces the proposed AGD circuitry and the operating principle. Section IV comprehensively analyzes the design process of the close-loop control. The experimental study is demonstrated in Section V and the conclusions are drawn in Section VI.

II. Challenges of Paralleled SiC MOSFETs and Current Sharing Methodologies

In prior to proposing the current sharing strategy, it is needed to understand the switching behavior of the paralleled SiC MOSFETs. The operating modes of a power device can be categorized into transient process, off-state and on-state. Correspondingly, the current imbalance can be categorized into dynamic imbalance and static imbalance [34]. The dynamic imbalance occurs in the midst of switching transient. The static imbalance occurs when the MOSFETs are in normal ON mode. The equivalent circuit of a system with two paralleled SiC MOSFETs is given in Fig. 1.

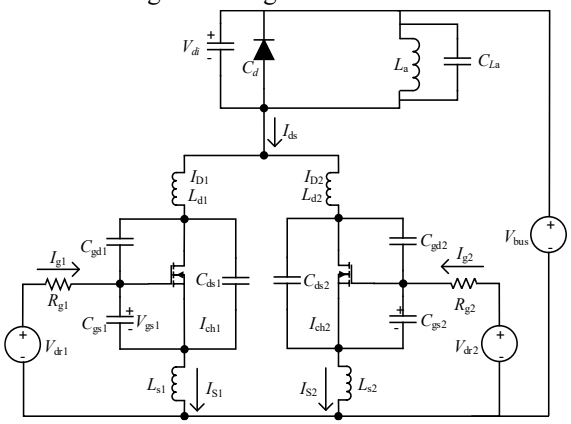


Fig. 1. The equivalent circuit of two paralleled SiC devices.

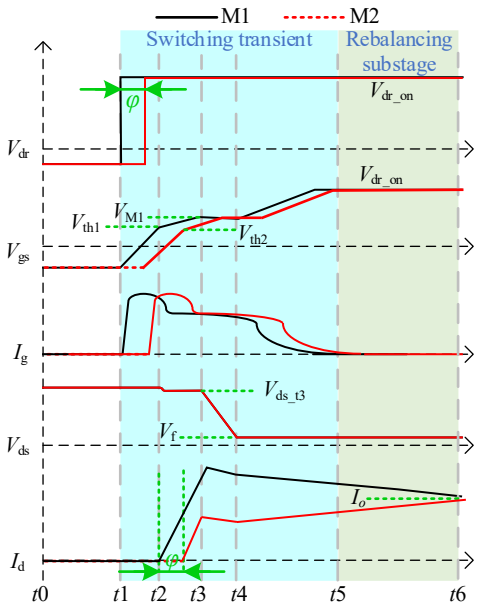


Fig. 2. A typical current waveform of paralleled SiC MOSFETs.

From the equivalent circuit, multiple variables that can impact the current distribution among the paralleled devices [20] include gate threshold voltage V_{th}, on-state drain-source resistance R_{dson}, gate driver voltage V_{dr}, gate signal lagging time

among devices φ, parasitic inductance on the PCB or the package (L_d, L_s, L_g), junction capacitance (C_{gd}, C_{gs}, C_{ds}), etc. Some parameters are equivalent parameters inside the die, while some parameters are introduced by the external circuit such as the package and the PCB. In general, parasitic inductance and φ have an impact on the dynamic transient while R_{dson} can affect the static current distribution. V_{th} and V_{dr} are coupled with both dynamic and static current distribution. Therefore, it is necessary to investigate and quantify the impact of each parameter on the current distribution.

The typical current waveform of two paralleled SiC MOSFETs, i.e., M1 and M2, is plotted in Fig. 2. M1 turns on slightly earlier than M2 and it can lead to current transient imbalance between the two MOSFETs. In Fig. 2, the turn-on transient of M1 starts at $t1$. The switching transient ends completely at $t5$. After $t5$, I_{ds} of the two MOSFETs will slowly come into a steady state and they are proportional to the conductance in the ON state.

A. Static imbalance

The static imbalance occurs due to the mismatched R_{dson} of each power MOSFET as shown in Fig. 3. It is straightforward that the current is proportional to the conductance of the MOSFET. Generally, R_{dson} can be calculated with (1).

$$R_{dson} = \frac{L}{W \mu_n C_{ox} (V_{gs} - V_{th})} \tag{1}$$

In (1), L, W, μ_n, and C_{ox} denote the length, width of each cell of power MOSFET, mobility of electron, and gate oxide capacitance, respectively. These parameters are determined in the midst of die manufacturing process and they are usually constant once the dies are fabricated. Thus, V_{gs} and V_{th} are the two variables that can affect the static current distribution.

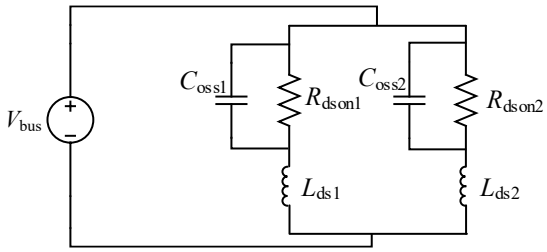


Fig. 3. The equivalent circuit of static current distribution.

For SiC MOSFET, the temperature coefficient of R_{dson} can be positive or negative which is determined by the junction temperature. For MOSFETs with positive temperature coefficient, R_{dson} increases when junction temperature rises and the conduction loss can reduce due to reducing I_{ds}. Therefore, these devices have self-balance capability and it is beneficial for paralleling. However, for some lower-voltage SiC MOSFETs, the drift region is usually designed to be thin to reduce the total R_{dson}. The resistance on the channel which has a negative temperature coefficient is the dominant part of the R_{dson}. Therefore, these devices have poor self-balance capability.

Another problem is the drift of gate threshold voltage V_{th} which is brought by the gate stress. For Si IGBT, V_{th} drift is not so serious that has a large impact on the current sharing. However, for SiC MOSFET, V_{th} drift is more frequent and it cannot be neglected. The static characterization results of a SiC power module are plotted in Fig. 4. Twelve groups of tests are conducted under each junction temperature. From Fig. 4, V_{th} occasionally changes from the typical value of 3.3 V to a random value between 2.4 V and 3.9 V. Also, V_{th} reduces as the junction temperature increases. The typical V_{th} under 150°C reduces to 2.2 V. Thus, V_{th} is not a constant value during the normal operation condition. H. Jiang [35] has conducted a comprehensive experimental study on the V_{th} drift for SiC MOSFET. It shows that negative bias of driver voltage can trigger large V_{th} variation. From (1), the V_{th} drift can change the R_{dson} and introduce challenges for current sharing. Note that the V_{th} drift not only affects the static imbalance but also the dynamic imbalance will be introduced in the following section.

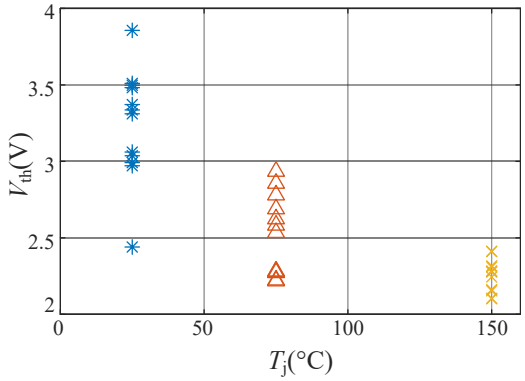


Fig. 4. The measured gate threshold voltage [53].

For the sake of the aforementioned problems, the self-balance effect cannot completely compensate the static current imbalance. Thus, it is necessary to propose an active current sharing method for static imbalance.

B. Dynamic imbalance

From Fig. 2, the turn-on transient of the drain current for paralleled devices comprises several stages including current rising (t2-t3), overshoot (t3-t4), and current rebalancing (t4-t5) as plotted in Fig. 5. The dynamic imbalance at current rising stage perform as delay time mismatch and *di/dt* mismatch. At the overshoot stage, it is the difference of peak current. In the rebalancing stage, which is the stage with the longest duration widely observed [5] [12] [14], the dynamic imbalance performs as a current rebalancing process from dynamic distribution to static distribution.

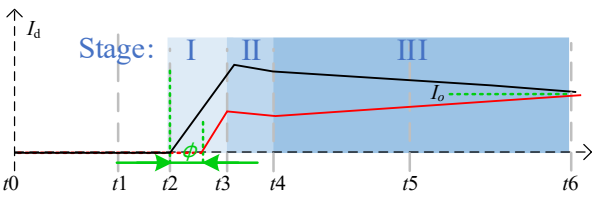


Fig. 5. The three stages of dynamic current imbalance.

(1) Stage I and II: Current rising and overshoot

Dynamic imbalance in the two stages is the consequence of mismatched switching transient process. There are two important indices for the switching transient: switching speed and switching start time. Changing of I_{ds} and V_{ds} occurs during the Miller plateau. The I_{ds} switching slew rate, i.e., *di/dt*, has a large impact on the degree of imbalance. The *di/dt* of the turn-on process can be roughly evaluated with (2) [22].

$$di/dt = \frac{g_{fs}\left(V_{dron} - 0.5V_{th} - 0.5V_{miller1}\right)}{R_g C_{iss} + L_s g_{fs}} \tag{2}$$

In (2), V_{dron} and $V_{miller1}$ denote the normal turn-on driver voltage and the Miller plateau voltage, respectively. Herein, $V_{miller1} = V_{th} + I_o / g_{fs}$ and g_{fs} is the transconductance of the SiC MOSFET. From (2), the mismatch of the multiple variables such as common source inductance L_s, g_{fs}, input capacitance C_{iss}, V_{th}, and driver voltage has a large impact on *di/dt*. Generally, if the two MOSFETs start synchronously, the MOSFET with higher *di/dt* will withstand a higher turn-on overshoot current and a lower turn-off overshoot current. To realize a current balance in the two stages, the di/dt should match with each other and the current rising action should be synchronized.

(2) Stage III: Current rebalancing

The current rebalancing process results from different distribution principles in turn-on transient and static on-state. When the dynamic current is mismatched at t3 in Fig. 5, there is an equivalent loop current between the two MOSFETs. Due to the parasitic inductance in the power loop, i.e., L_{ds1} and L_{ds2} in Fig. 3, the loop current cannot be eliminated immediately. It will slowly reduce to the steady-state current which is determined by the R_{ds_on} of both MOSFETs. Therefore, stage III is usually much longer than stage I and II.

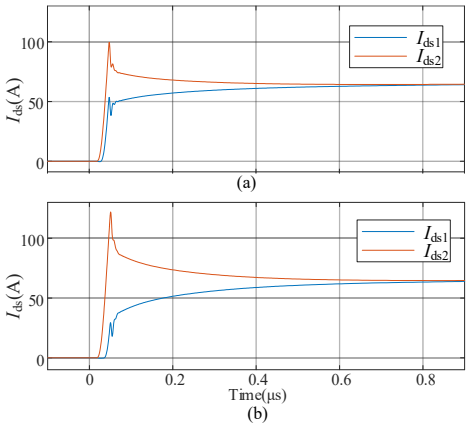


Fig. 6. The LTspice simulation results for dynamic imbalance caused by asynchronous gate signal. (a) φ=8 ns. (b) φ=16ns.

The LTspice simulation results of two paralleled SiC MOSFETs under an asynchronous gate signal are given in Fig. 6. In the simulation, the lagging time between the two SiC MOSFETs is φ. Longer φ leads to a larger degree of imbalance. In the worst case, when φ is very long, all turn-on stress will be withstood by a MOSFET while another MOSFET operates in zero-voltage switching mode.

C. Current sharing methodologies

From the analysis above, there are multiple variables that can affect the static and dynamic current distribution. Some parameters such as the junction capacitance, parasitic inductance, and V_{th} are the intrinsic parameters on the circuit or the dies, which cannot be actively controlled. From the gate driver side, the driver voltage V_{dr}, gate signal delay time φ, and gate resistance R_g can be controlled, which is usually implemented via utilizing AGDs.

The static current can only be adjusted by changing V_{dr}. [36] and [29] introduces several AGD circuitries with adjustable normal turn-on voltage V_{dron}. However, it should be noted that the larger V_{dr} also means higher saturation current and lower short-circuit withstand time, which are detrimental to the reliability of the system. Therefore, the design of the static current sharing should also consider this tradeoff.

The dynamic current can be changed by adjusting φ, R_g, driver current I_g and V_{dr}. Both R_g and V_{dr} can change *di/dt* according to (2). Several variable gate resistance AGD circuitries are introduced in [37] [16] while variable gate voltage AGD circuitries are proposed in [36] [38]. Changing φ can hardly adjust the slew rate, but it can realize the dynamic current sharing via changing the peak current. Generally, the MOSFETs that turn on earlier and turn off later undergo higher current stress when the slew rate is the same. Changing I_g can be implemented by using the current source gate driver, which is another promising approach to control the dynamic drain current. The current source gate driver has a different mechanism from (2) as it directly determines the charging speed of the input capacitance [39]. Current mirrors are widely applied as a branch path of gate loop to sink or source gate current [18] [40] [41], or directly function as a driving source array [42].

Another critical part of close-loop current sharing control is signal feedback. Due to the fast switching speed of SiC MOSFET, stage I and II are very short. They are generally finished in a couple of nanoseconds. Therefore, measuring the current in stage I and II requires ultra-high-bandwidth sensors which are usually expensive and challenging to hardware design. In contrast, stage III is much longer than stage I and II. Measuring the current in stage III is much easier. Even though the switching loss is not generated in stage III, it can still indicate the current dynamic imbalance. In other words, if drain current at stage III is not balanced, it can be claimed that the dynamic transient is not balanced. Based on this argument, the current in stage III can be utilized as the feedback signal for dynamic current sharing control.

III. Circuit of The Close-Loop AGD

Based on several state-of-the-art current sharing methodologies introduced in the last section, a close-loop

active gate driver circuit is designed for comprehensive current balancing and switching behavior optimization. First, the high-frequency current transformer is implemented for current error feedback and the design process is described. Then, the proposed circuit and its operating principle will be demonstrated.

A. Current sensing transformer

To implement close-loop control, current sensors are necessary to realize real-time current measurements. It should provide enough bandwidth since the proposed AGD needs to compensate for the dynamic and static current imbalance and the dynamic process can be finished in a couple of nanoseconds. Therefore, two current transformers are utilized for sensing drain-source current I_{ds}. They are embedded into the PCB to reduce the length of the power loop. Compared with the existing AGD solutions, the impact of current transformers on the power loop impedance is low while its bandwidth is enough for I_{ds} sampling of SiC devices. The transduced I_{ds} from the current transformer will be conditioned into an analog signal with a signal conditioning circuit and delivered to the Analog/Digital Converters (ADCs) of the DSP controller for control signal processing.

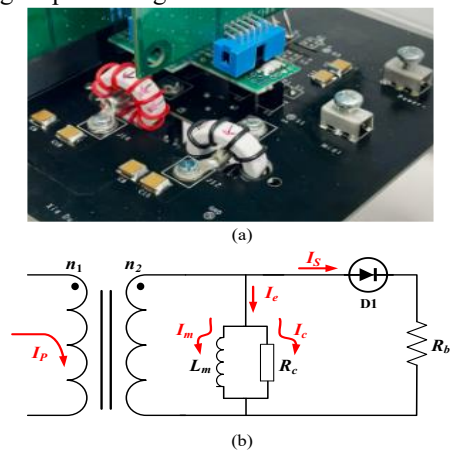


Fig. 7. Current transformer design. (a) Structure. (b)Equivalent circuit.

The basic structure of the current transformers is shown in Fig. 7 (a). 3E12 toroid core is selected for the transformer. The measured current flows across the center of the toroid and the secondary side has ten turns of winding.

TABLE I SPECIFICATIONS OF APPLIED CURRENT TRANSFORMER

Parameter	Value
Turn ratio	10
Magnetic core	MnZn Ferrite
Burden resistor	1 Ω
Primary turns	1
Secondary turns	10
Bandwidth	100 MHz
Accuracy	±4% within 50 A
Physical dimensions	22 mm x 14 mm x 6 mm

A 1 Ω current sensing resistor R_b is utilized to transform the transduced current into a voltage signal. The equivalent circuit of the current transformer can be drawn in Fig. 7 (b). To have high accuracy, the magnetizing inductance L_m should be larger so that there will be less current I_e diverted from secondary current I_s. To avoid saturation, a diode D_1 is connected in series with R_b. When the switch turns off, the reverse recovery voltage will quickly reset the magnetic core for the next switching cycle. Table I shows the current transformer specs.

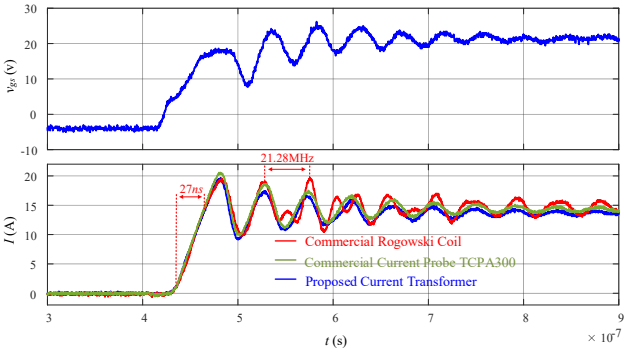


Fig. 8. Bandwidth validation waveforms of the current transformer.

Fig. 8 shows the results of the current transformer bandwidth validation test. The current transformer is compared with a 30 MHz commercial Rogowski coil and a 100 MHz TCPA300 current probe. It can be seen that the waveform of the proposed current transformer matches well with the TCPA300, while the 30 MHz commercial Rogowski coil has distortions. Therefore, the performance of the proposed current transformer is close to a 100MHz current probe which is enough for this application.

B. Analog conditioning circuit

To achieve reliable and accurate current measurements, it is essential to carefully suppress the noise. Common mode noise poses a major challenge to these applications [43]. The switching noise and ringing can be coupled into the analog signal chain through both conductive and wireless paths. To address this problem, a high-speed differential buffer circuit is designed as shown in Fig. 9. A 700MHz operational amplifier LTC6229 is applied to ensure the signal integrity [44]. The two voltage follower circuits in the first stage can cancel the influence from the output impedance of the current transformer. The differential circuit at the second stage cancels the common mode noise. To improve the common mode noise rejection ratio (CMRR), a high-precision 1kΩ resistor array LT5400 is used with an ultra-low match ratio of 0.0125% [45].

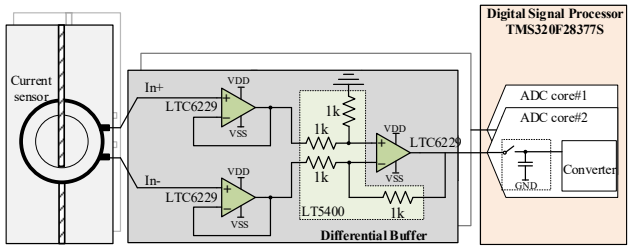


Fig. 9 Analog conditioning circuit.

C. The proposed AGD circuitry

The circuit and the control strategy of the proposed AGD

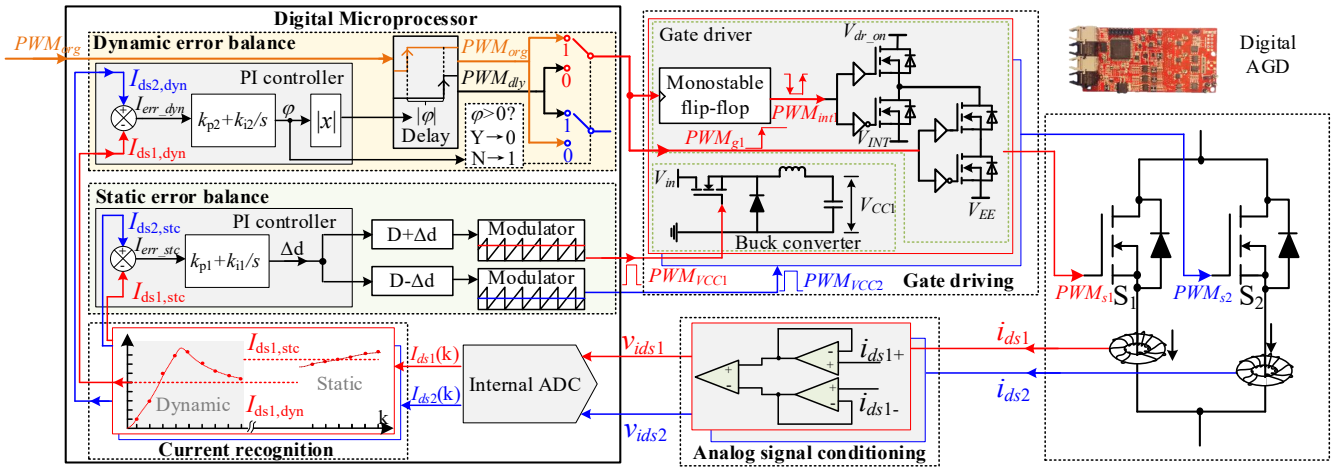


Fig. 10. The circuit scheme of the 3-L AGD and the control block diagram.

circuit are shown in Fig. 10. A gate driver with an integrated DSP controller is deployed to realize the drain to source current balancing control. Note that this DSP is a local controller for the AGD and it is not the converter main control unit.

First, the two drain-to-source currents are measured via two current transformers and then sent to the analog signal conditioning circuit to match the input range of internal ADC in the DSP. The drain-to-source currents are sampled with the 5 MSPS ADC, the sampling sequence of which is shown in Fig. 12. It should be noted that although the turn-on transient of SiC MOSFET can be finished in tens to hundreds nanoseconds, stage III has a longer duration with 1-2 us. A 5 MSPS ADC can sample enough points to capture accurate dynamic current error in stage III. A case is given in Fig. 11. The dynamic current imbalance at stage III can be clearly measured, while the current rising process cannot be identified.

Fig. 12 shows the sampling scheme of the proposed method. Continuous sampling is triggered with the sampling enable signal, which flips from low to high simultaneously with switching PWM signal PWM_{org}. Since the moment when the current starts rising is lagging with the flip instant of PWM_{org}, the sampling can cover the whole process of the current rising. When PWM_{org} flips from high to low, the sampling enables signal flips after a delay time T_{d_drv} for covering the whole process of current falling.

As shown in Fig. 10, according to the sampling results, the drain-to-source current is regarded as two stages: turn-on dynamic current and static current. The dynamic current is defined as the current at the first one μs after the rising/falling edge of gate signals. The stage III current is defined as the current from 1.2 to 2 μs. The average value of sampling points in the two stages is calculated respectively as $I_{ds1,dyn}$, and $I_{ds2,dyn}$ for dynamic current, $I_{ds1,stc}$ and $I_{ds2,stc}$ for static current. The dynamic currents are sent to the dynamic current error controller. The gate signal delay time φ between the two MOSFETs is adjusted via a PI controller to balance the dynamic current error as,

$$I_{err\_dyn} = I_{ds2,dyn} - I_{ds1,dyn} \tag{3}$$

$$\varphi = I_{err\_dyn} \cdot k_{p1} + I_{err\_dyn} \cdot \frac{k_{i1}}{s}, \tag{4}$$

where I_{err_dyn} is the dynamic current error. k_{p1} and k_{i1} denote the proportional and integral coefficients of the dynamic current sharing PI controller, respectively. To realize the flexible time delay φ, the EPWM deadband submodule is leveraged to switch the delay time between two gate signals [46].

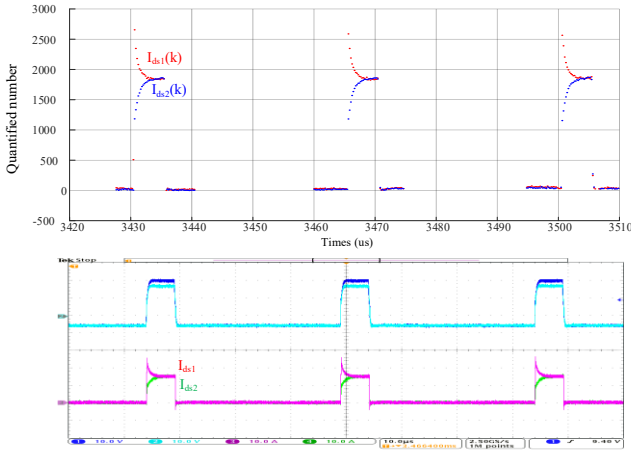


Fig. 11. Sampling results of drain current.

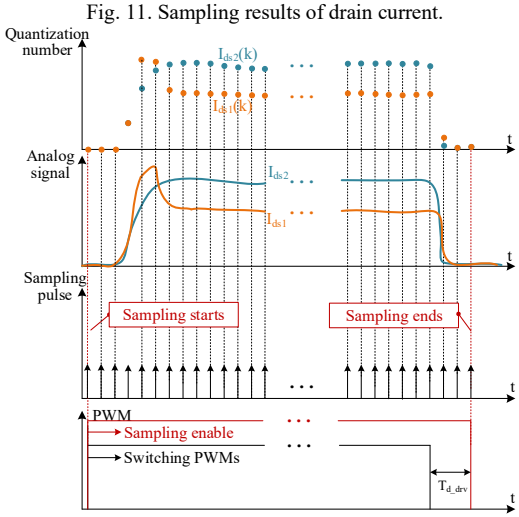


Fig. 12. Sampling scheme of the proposed method.

At the same time, the static current error is sent to the static current error controller. Via controlling the duty cycle of the buck converter, the on-state driver voltage can be adjusted for static current balancing, which is expressed as

$$I_{err\_stc} = I_{ds2,stc} - I_{ds1,stc} \tag{5}$$

$$\Delta \mathrm{d} = I_{err\_stc} \cdot k_{p2} + I_{err\_stc} \cdot \frac{k_{i2}}{s}, \tag{6}$$

where I_{err_stc} is the dynamic current error. k_{p2} and k_{i2} are proportional and integral coefficients of the PI controller for the static current sharing, respectively.

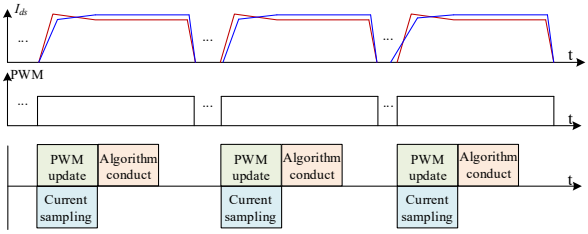


Fig. 13. Control sequence of the current balance.

To realize a close-loop current balancing continuously, a control sequence is designed as shown in Fig. 13. For each switching cycle, the gate signal profile is updated according to the computing result of the current balancing algorithm conducted in the previous cycle. At the same time, the drain-to-source current is sampled. Once the turn-on current error and static current error are sampled, the current balancing algorithm can be conducted, and the PWM gate signal will be updated in the next switching cycle correspondingly.

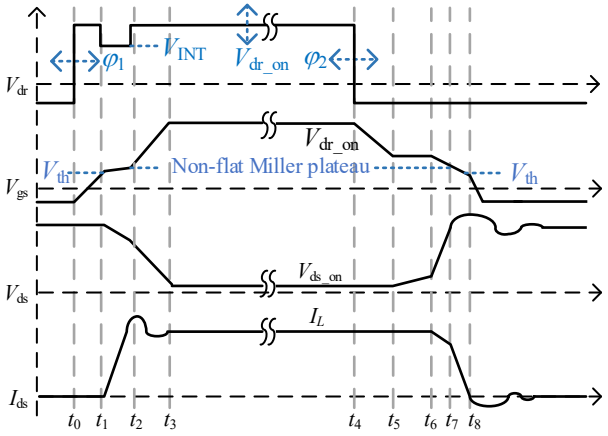


Fig. 14. The multi-level gate driver voltage profile.

The 3-L turn-on can be implemented with the cascaded-connected driver buffers and the operating principles are demonstrated in [47]. The 3-L driver voltage profiles are plotted in Fig. 14. During the miller plateau of turn-on transient, the driving voltage is switched from V_{dr_on} to an intermediate voltage V_{INT}. Via pulling down the driver voltage, the slew rate is adjusted, and the overshoot current can be suppressed.

An isolated power supply is utilized to generate the driver voltage V_{in}. Its output is connected to a buck converter. Via controlling the duty cycle of the buck converter, the DSP can regulate the on-state driver voltage, i.e., V_{dr_on} in Fig. 10, to the desired level. The gate signal delay time φ between the two MOSFETs is generated by the High-Resolution Pulse Width Modulation (HRPWM) register of the DSP controller.

From (1), higher V_{dr_on} can reduce R_{ds_on}, and the ON-state current is higher. Thus, adjusting V_{dr_on} can effectively change the static current distribution. The dynamic imbalance can be adjusted via changing the gate signal delay time φ between the two paralleled devices. Simulation is conducted with LTspice to study the impact of φ on the dynamic current distribution in Fig. 15. Manually delaying the gate signal of MOSFET #2 by 10 ns, the dynamic imbalance is alleviated. It can be seen that when the gate signal is synchronous, the I_{ds} overshoot of MOSFET #2 is higher than that of MOSFET #1 due to faster switching transient.

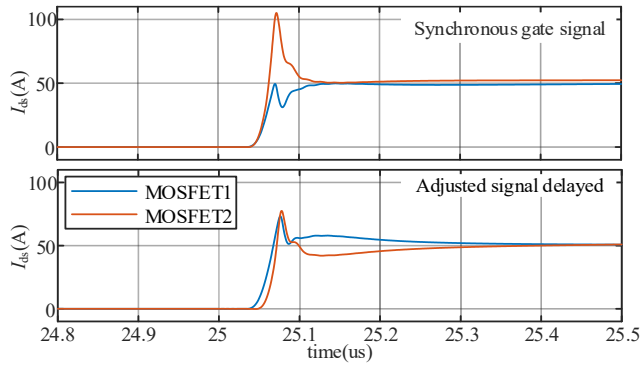


Fig. 15. Current waveform of two devices under different φ.

An experimental study is also conducted to quantify how φ can affect the current distribution. Twenty CREE C3M0021120D discrete devices are prescreened and two MOSFETs with the same R_{ds_on} and different C_{oss} are selected as the devices under test (DUTs). The experimental results which reveal the dynamic current distribution of the DUTs under different φ are plotted in Fig. 16 [48].

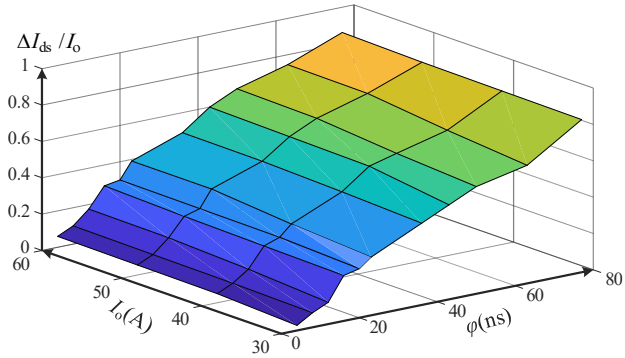


Fig. 16. The impact of φ and I_o on ΔI_{ds} [48].

IV. Close-Loop Control Design

From Fig. 10, there are two major control loops, i.e., static current and dynamic current loop. The static current control objective is V_{dr_on} while the dynamic current control objective

is gate signal delay time φ. In this section, the design of the two control loops will be demonstrated.

A. Static current adjustment

The feedback signal is the on-state current. The dynamic current can be adjusted by changing φ of the PWM signal. This section will demonstrate the design of the control parameters of the two loops.

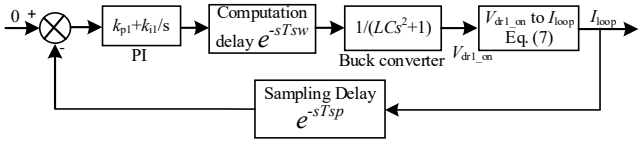


Fig. 17. The control block diagram for the static imbalance.

The V_{dr_on} adjustment is implemented with the buck converter. The control block diagram can be found in Fig. 17. The sampling delay is caused by the sensors and analog/digital converter. The computation delay is caused by the signal processing in the DSP controller. With the given signals from the DSP controller, the buck converter can regulate to the level desired. The control plant is the power MOSFET. The static current distribution is proportional to the conductance in the on-state. Therefore, I_{loop}=I_{ds1_on}-I_{ds2_on} of the MOSFET can be calculated with (7).

$$I_{loop}=\frac{\left(\alpha_1 V_{dr1\_on}-\alpha_2 V_{dr2\_on}-\alpha_1 V_{th1}+\alpha_2 V_{th2}\right)I_o}{\alpha_1 V_{dr1\_on}+\alpha_2 V_{dr2\_on}-\alpha_1 V_{th1}-\alpha_2 V_{th2}} \tag{7}$$

In (7), α denotes $W\mu_n C_{ox}/L$. To simplify the analysis, the AGD maintains V_{dr2_on} at a constant level. Via adjusting V_{dr1_on}, the current can be balanced. From (7), the equation is linear. The computation delay is introduced by the signal processing in the DSP controller. Since the signal of the last switching period will be utilized in this switching period, the computation delay is generally $e^{-sT_{SW}}$ where T_{SW} is the switching period. The sampling delay is e^{-sT_s} and T_{sp} is the sampling period of the sensor. The sensor frequency is much higher than the switching frequency, thus the sampling delay is very low. The isolated power supply can adjust V_{cc} with the control signal.

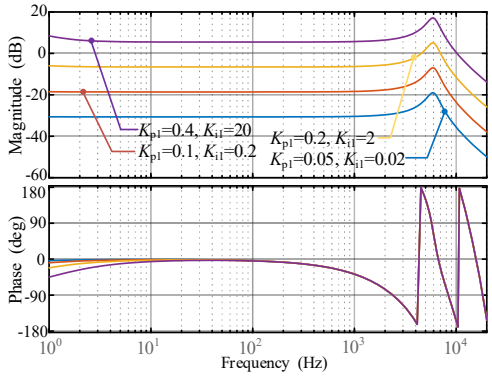


Fig. 18. The Bode plot of the static current sharing control.

The Bode plot of the open-loop transfer function for the static current control is illustrated in Fig. 18. Note that decreased control gains reduce the magnitudes, while the phase characteristics are not impacted. It is preferred to shape the loop gain below 0 dB to properly damp down the high-frequency disturbances.

B. Dynamic current adjustment

The dynamic current imbalance can be addressed by changing the delay time of gate signal φ. Similar to the static current imbalance, computation delay is introduced by the DSP control signal processing. With the control block diagram, the feedback loop can be designed. The control plant is gate signal φ to ΔI_{ds}. An experimental study is conducted to quantify the formula from φ to ΔI_{ds}. From Fig. 16, the relationship of ΔI_{ds} *vs*. φ can be fitted with an exponential function as shown in (8).

$$\Delta I_{ds}=I_o-I_o*e^{\alpha\varphi+\beta I_o} \tag{8}$$

In (8), β denotes the fitting coefficients. The close-loop control block diagram is given in Fig. 19. Also, the implementation of signal delay is very fast since it is generated inside the DSP controller. The calculated value in the n-th switching cycle will utilize in the (n+1)-th switching cycle. Thus, computation delay on the DSP is considered as a switching period T_{sw}. Combining (8) and Fig. 19, the stability for close-loop dynamic current sharing control parameters can be optimized using the bode plot that is given in Fig. 20.

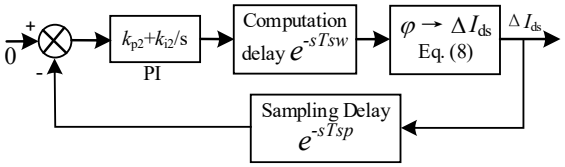


Fig. 19. The control block diagram for the dynamic imbalance.

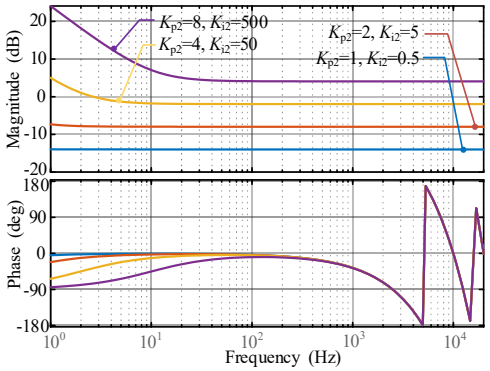


Fig. 20. The Bode plot of the dynamic current sharing control.

V. Experimental Verification

A multi-pulse test circuit experimental prototype, as shown in Fig. 21, is constructed to validate the functionality of the proposed AGD scheme. The local controller is a TI TMS320F28379D processor. The two DUTs in parallel are CREE C2M0045170D and Microchip MSC035SMA170B respectively to manually generate the current imbalance.

The AGD board can be found in Fig. 22 (a). The gate signal isolation utilizes fiber optics while the driver power supply is a

5W CUI isolated power supply that provides V_{in}. The buck converter is implemented on the driver board. The schematics of the AGD are shown in Fig. 22 (b).

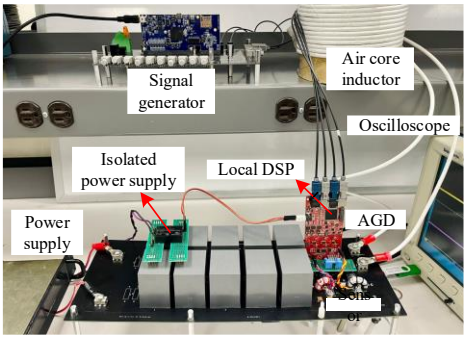


Fig. 21. The multi-pulse test setup.

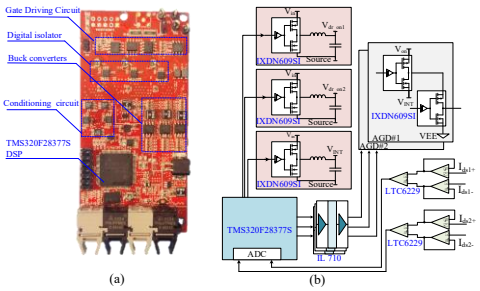


Fig. 22. Intelligent gate driver for close-loop current sharing. (a) Gate driver setup. (b) Gate driver schematics.

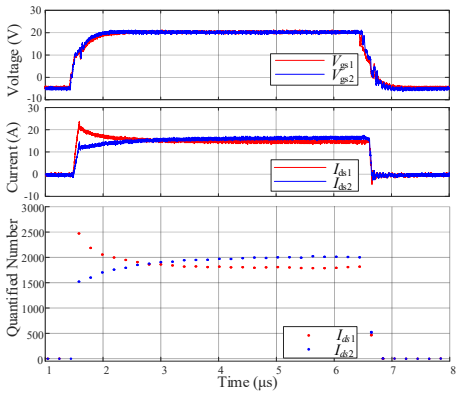
Two current transformers are utilized to transduce I_{ds} and the current signal is conditioned with two analog voltage follower circuits. An IL710 digital isolator is employed between the DSP and the cascaded driver buffer circuit to generate a three-level turn-off profile. To validate the functionality of close-loop control, 100 pulses are generated, and the maximum I_{ds} for each MOSFET. The bus voltage is 600V while the current is 15A for each device. The control parameters are listed in Table II.

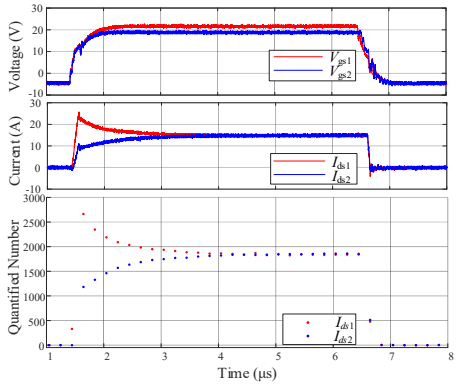
TABLE II THE CONTROL SYSTEM PARAMETERS

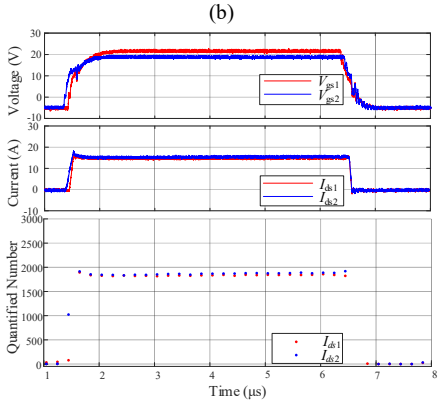
Elements	Parameter	Value
Control loop	Controller coefficient	K_{p1}=0.19, K_{i1}=0.21 K_{p2}=0.28, K_{i2}=0.15
	Switching frequency (f_{sw})	10 kHz
	Sampling frequency (f_{sp})	5 MHz
Control platform	Part number	TMS320F28377SPZPT
	Core processor	C28x 32-bit
	Speed	200MHz
	Number of I/O	41
	Program Memory Size	1 MB
	ADC	12bit, 4 modules, 14 channels
	PWMs	24 channels (16 HRPWMs)

The switching frequency of the continuous pulse is 10 kHz and the signal sampling frequency is 5 MHz which is enough to feedback the current signal. The experimental results and the current sampling points of the multi-pulse test are given in Fig. 23.

Fig. 23 (a) is the waveform of the original condition which shows that both static and transient I_{ds} on the two DUTs are not balanced due to mismatched electrical parameters. The V_{gs} of







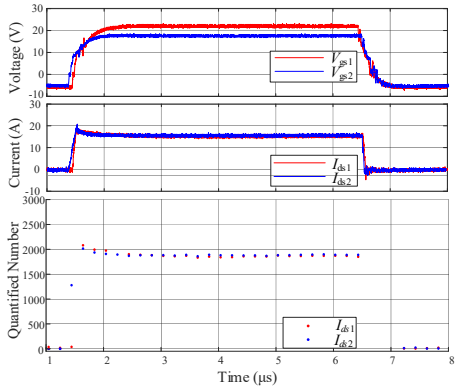


Fig. 23. The experimental results and current sampling points of multiple pulse test. (a) Without close-loop control. (b) With static currentclose-loop control. (c) With static and dynamic current sharing control. (d) Without 3-L turn-on driver voltage.

both MOSFETs is 20V. There are 1.5A static current mismatches, and the difference between the turn-on transient current peak is 10 Amps. To present the control effect of dynamic and static current control, the static current control is initiated first while the dynamic is disabled. The test results are shown in Fig. 23 (b). The V_{gs1} increases to 22 V while V_{gs2} reduces to 18 V. The static current imbalance is completely suppressed while dynamic current sharing is not compensated. After 60 pulses, the control loop for dynamic current sharing is enabled and makes V_{gs2} lag behind V_{gs1} for 72 ns as shown in Fig. 23 (c). The difference in peak turn-on I_{ds} reduces from 12 A to 0.8 A. Fig. 23 (d) shows the waveform without 3-L turn-on driver voltage. Comparing Fig. 23 (c) and (d), the 3-L turn-on can reduce the overshoot voltage from 25% to 12%. The experimental results have validated the functionality of the proposed AGD-based current sharing scheme. It can not only suppress the overshoot current but also compensate for the static and dynamic current imbalance. Note that the drain turn-off I_{ds} of the two devices match with each other in Fig. 22, which is realized by a pre-set turn-off delay time for two driving signals. Since the turn-off current error behaves as an overshoot [15] with a short duration, it is not included in this close-loop design.

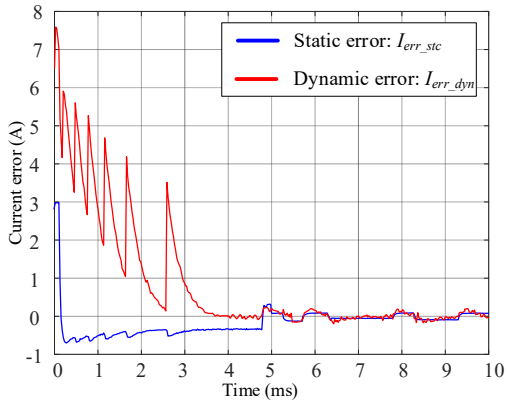


Fig. 24. The response curves of current errors with current balancing control.

Fig. 24 shows the response curve of current errors in the current balancing control process. Note that the dynamic control and static control for Fig. 23 are started simultaneously. The initial static error and dynamic current error are 3A and 7.5A, respectively. After 5ms, the PI controller operates to suppress the error and both errors decline rapidly.

A noteworthy phenomenon in Fig. 24 is that the static current error control is coupled with the turn-on dynamic current error control. During the convergence process, the dynamic current error response curve shows a fluctuation. This is due to the fact that the adjustment of V_{dr_on} for the static error balancing loop can affect the performance of the turn-on current transient as described in equation (2), which further impacts the turn-on dynamic current error. Any change in V_{dr1_on} results in a corresponding change in V_{gs} during the turn-on transient, which, in turn, affects the I_{ds} response. Therefore, in control parameter design, it is important to carefully consider the coupling between two control loops.

VI. Discussion

In practical application scenarios, to realize a higher current rating, more than two devices/modules are usually connected in parallel. For instance, a Tesla Model 3 EV uses six T-pak SiC MOSFETs in parallel in the main inverter. It poses higher the current sharing challenge. This section discusses the application of the proposed current sharing method in these scenarios.

A. Paralleling Device Amount

The amount of devices in parallel is highly associated with the employed hardware. In this section, this issue will be discussed via a case study. Each device requires an independent current transformer and a gate driver buffer as shown in Fig. 25. The number of paralleling devices is determined by the employed AGD DSP specs, such as ADCs and computation capability. For instance, a TMS320F-28377s DSP controller has four integrated synchronized sampling ADC modules. By sharing one ADC module between two current samplings and assigning interleaved samplings correspondingly, it can support up to 8-devices paralleling.

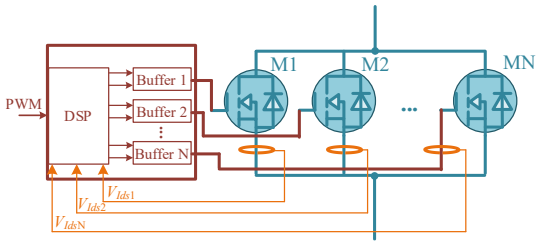


Fig. 25. Application scheme for multi-paralleled SiC devices.

The computation resources of a DSP are occupied by the calculation of average current value, current error, PI controller, and PWM configuration. To implement more devices paralleling, some parallel processing functions including Direct Memory Access (DMA) [49], Control Law Accelerator (CLA) [46], and Configurable Logic Block (CLB) [50] can be leveraged to reduce the computation load of the DSP. Besides, the equivalent high-speed sampling approach can be considered to increase the utilization of ADC resources [51].

B. Current sharing of multi-dice paralleling in a power module

A power module usually comprises multiple dice in parallel to boost the current rating. Therefore, in some conditions, when the current is unbalanced in a power module, it is desired to implement the proposed current sharing method. Fig. 26 gives a potential circuitry for the proposed current balancing method. In Fig. 26, the gate side of each MOSFET should be separated and driven by an independent buffer, which allows decoupled gate signal delay and driving voltage level adjustment on each die. Consequently, the gate pin of each die must be connected separately, necessitating additional considerations for the module's direct bonding copper layout design.

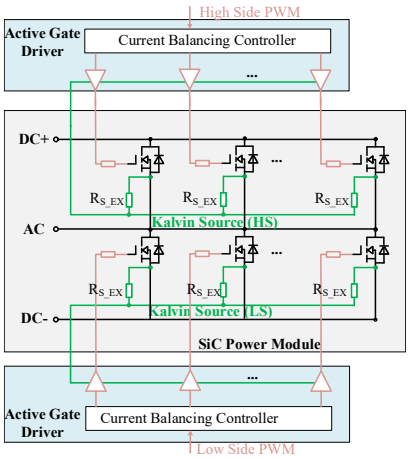


Fig. 26. Application of the proposed current sharing method in a multi-dice power module.

A close-loop current balancing approach for power modules requires accurate measurement of the drain-to-source current of each die. Designing a compact, non-intrusive, and high-bandwidth current sensor is a critical challenge due to the small size and the complex operating environment within the module [51]. Furthermore, integrating these current sensors inside the module requires advanced packaging technology.

VII. Conclusion

In this paper, a digital close-loop active gate driver based on the patent is proposed for both static and dynamic current sharing. A local DSP controller can compensate for the current imbalance with sensed current signals. Via changing the turn-on driver voltage and the lagging time between the gate signals, the static and dynamic current are effectively adjusted respectively. The 3-L turn-on driver voltage profile can effectively suppress the overshoot current. The continuous pulse test results have validated the functionality of the proposed circuit and the control strategy. The scalability in multi-dice current sharing inside a power module and the maximum amount of paralleling devices are discussed. They figure out the next research topic.

VIII. Acknowledgement

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