A Simple Gate Driver Design for SiC MOSFET Paralleled Operation

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***Abstract*-- Paralleling operation of SiC MOSFET is one of the essential solutions to improve current rating of SiC MOSFET applications. In this paper, a simple gate driver design is proposed for SiC MOSFET paralleled operations. The driving delay time and voltage level of on-state can be adjusted flexibly without any usage of digital processors; hence it is more cost-effective and reliable for complex EMI environment of high voltage and frequency applications. The operating principle to alleviate the current error of paralleled SiC MOSFETs is described and analyzed. The performance of the proposed gate driver is verified by the experiment.**

***Index Terms*-- Power Devices (Si / Wide band gap) and Applications, Gate Driver, SiC MOSFET Parallel Operation**

I. INTRODUCTION

SiC is a wide-bandgap semiconductor material that offers significant advantages over traditional silicon (Si) devices, such as higher electric field strength and improved thermal conductivity. These characteristics have led to the development of SiC MOSFETs, which exhibit reduced conduction and switching losses, allowing for higher switching frequencies and greater efficiency in power electronic applications. SiC MOSFET received increasing attention because of its superior feature over IGBT, including lower power losses, higher switching frequency, and higher temperature tolerance [1]. In high-power applications, such as electric vehicle (EV) traction inverters, renewable energy converters, and industrial drives, a single SiC MOSFET may not be sufficient to handle the required current levels. To achieve the desired power rating, multiple SiC MOSFETs can be connected in parallel, effectively increasing the overall current-carrying capacity while maintaining the benefits of SiC technology. Generally, the relative solutions can be divided as 4 levels: die module topology and converter. On die level, the improvement depends on the development of material and fabrication technique. On module level, the main challenge is how to keep a consistency of dies and compensate the mismatch between them. On topology level, the main topic is how to define an optimized driving signal for each module. And how to monitor the current error. On the converter level, the topic is usually related to coordination control of micro converters. Some techniques like virtual impedance, interleaving modulations, and bus communications are often discussed in this region [2]. All solutions can be combined to apply in field application according to specific scenarios [3]-[6].

One technical route to meet the expectation is to parallel several SiC MOSFETs [7] so that the drain to source current can be shared among several devices. The primary benefits of parallel operation of SiC MOSFETs include:

1). Increased Current Capacity: By connecting multiple SiC MOSFETs in parallel, the overall current-carrying capacity is increased, enabling the system to handle higher power levels [8].

2). Improved Reliability: Parallel operation can enhance system reliability by distributing the current evenly among the parallel devices, thereby reducing the stress on each individual MOSFET and extending its operational life.

3). Enhanced Thermal Management: Distributing the current across multiple devices allows for better heat dissipation, resulting in reduced thermal stress and improved overall system efficiency.

4). Modular Design Flexibility: Parallel operation enables designers to scale up or down the number of MOSFETs to match the requirements of various applications, facilitating a more flexible and modular design approach.

Despite the numerous benefits, the parallel operation of SiC MOSFETs presents several challenges that need to be addressed to ensure optimal performance:

1) Current Sharing: Uneven current distribution among parallel MOSFETs can lead to thermal imbalance and reduced reliability. This can occur due to manufacturing tolerances, variations in device parameters, or differences in gate drive circuitry.

2) Gate Drive Design: To achieve proper current sharing and fast switching performance, it is crucial to design a suitable gate drive circuit that minimizes the propagation delay and ensures a well-balanced gate-source voltage (Vgs) among the parallel devices.

3) Parasitic Inductance: The parasitic inductance in the power loop and gate drive loop can cause voltage overshoot, ringing, and increased switching losses. It is essential to minimize these parasitics through careful PCB layout and component selection.

Due to the characteristic mismatch of SiC MOSFET devices, a current error exists among devices and reduces the lifetime of the switch due to unbalanced thermal accumulation. There are several considerations to reduce or remove the current unbalance:

1) Device Selection: Choose SiC MOSFETs with similar on-resistance (R_{dson}) and threshold voltage (V_{th}) characteristics to ensure better current sharing and minimize the risk of thermal runaway.

2) Gate Drive Design: Implement a robust gate drive

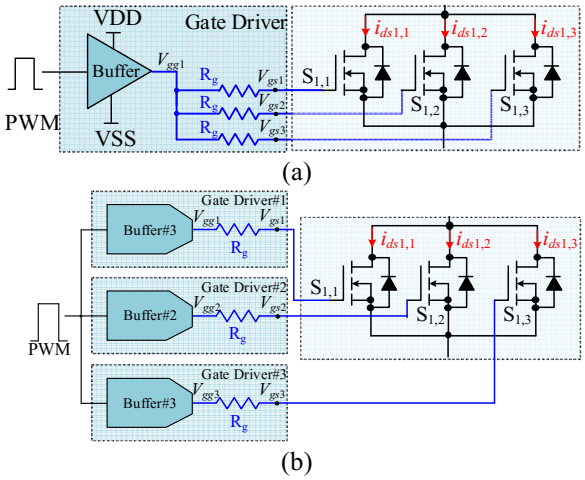


Fig. 1: Comparison of driving solution for paralleled SiC MOSFETs. (a) Single gate driver solution. (b) Multiple gate driver solution.

circuit with minimal propagation delay and adequate gate drive strength to ensure fast, synchronized switching among the parallel devices. This can be achieved by using matched gate resistors, dedicated gate drive ICs, or isolated gate drivers.

3) PCB Layout: Optimize the PCB layout to minimize parasitic inductance in the power loop and gate drive loop. This involves placing power devices close together, using short and wide traces, and incorporating a low-inductance ground plane.

4) Thermal Management: Employ an effective cooling solution to maintain a uniform temperature across the parallel devices. This may include using heatsinks, forced-air cooling, or liquid cooling systems.

5) Monitoring and Protection: Implement a monitoring system to track the individual device temperatures and current levels, as well as protection mechanisms such as over-temperature and over-current protection to ensure safe operation under various conditions.

One of the solutions for the current sharing issue is to differentiate the driving signals of paralleled devices via gate driver configuration [8]. Each SiC MOSFET is driven by an independent gate driver so that the driving signal can be separately defined as shown in Fig. 1. In Fig. 1(a), the three paralleled SiC MOSFETs are driven by the single gate driver. Although the gate resistance can be selected with different value to balance the current error at turn-on transient, the static driving voltage can not be differentiated to balance the static current error. In Fig. 1(b), three MOSFETs are driven by independent gate drivers, and hence the static and dynamic current balancing can both be balanced. There are several works about gate driver design for SiC MOSFET paralleling operations. The design of gate drivers for paralleling SiC MOSFETs can be analyzed from three different aspects:

1) Adjustable parameter gate drivers. The first aspect focuses on gate drivers with adjustable parameters, which allow for the active selection of gate resistance, driving voltage, and turn-on time delay [9]. These solutions require systematic debugging to find the optimal preset parameters for achieving the best current sharing performance. Essentially, these adjustable parameter gate drivers rely on knowledge of MOSFET circuit parameters to deliver a finely tuned gate driving signal for each MOSFET, minimizing the drain-to-source current discrepancy [10].

2) Online Parameter-Adjustment Capabilities. The second aspect considers gate drivers with online parameter-adjustment capabilities [11]. These drivers offer greater flexibility in testing and optimizing gate driver parameters and enable engineers to modify switching speed and on-resistance even during field operation. However, circuit and device parameters may change over time and under varying environmental conditions (e.g., temperature, humidity, etc.), potentially leading to abnormal operation of such open-loop current balancing methods.

3) Closed-Loop Current Balancing. The third aspect revolves around closed-loop current balancing approaches. In this aspect, the current error is fed back to the driving circuit, compensating the gate driving signals. In [12], an active gate driver is designed to balance the drain to source current of paralleled SiC MOSFET, where a CPLD is integrated into gate driver to insert an intermediate level and adjust the delay time of driving signals. For closed-loop active gate driver designs, it is common to incorporate analog circuits that convert voltage on parasitic inductors to current signals [13], thereby enhancing the robustness of current balancing. However, these methods still rely on estimating one or more MOSFET parameters to determine the current error between two SiC MOSFETs. Consequently, measuring or estimating parasitic inductors remains necessary, and any drift in this parameter can pose a risk of unsuccessful balancing. Another limitation of these techniques is the difficulty in scaling complex analog circuits for multiple parallel-connected devices. Measuring current errors among three devices is significantly more complicated than measuring errors between two devices. In such cases, a typical approach involves calculating the mean value of the current and comparing each device's current error to this mean value [14].

In this paper, a simple and low-cost gate driver design is proposed to realize the current balance of paralleled SiC MOSFET without any digital processors. The static driving voltage and the gate driving delay time can be adjusted flexibly and precisely via simple circuitry. The dynamic current error and static current error are both balanced by adjusting the turn-on time delay and gate-to-source driving voltage level, respectively. The operating principle to alleviate the current error of paralleled SiC MOSFETs is described and analyzed. The performance of the proposed gate driver is verified by the experiment.

II. The Proposed Gate Driver

A. Current Error Analysis in Paralleled SiC MOSFET

Fig. 2 illustrates the drain-to-source current error generation process for two paralleled SiC MOSFETs [14]. When the driving signals, V_{gg1} and V_{gg2}, are identical, the gate-to-source voltages, V_{gs1} and V_{gs2}, start to rise until entering into the miller plateau. Due to the mismatches in circuit parameters, a current error usually exists at the turn-on process, as described by equation (1).

$$I_{err\_on}(t)=\underbrace{\frac{1}{2}\beta_1\cdot(V_{gs1}(t)-V_{th1})^2}_{I_{ds1}(t)}-\underbrace{\frac{1}{2}\beta_2\cdot(V_{gs2}(t)-V_{th2})^2}_{I_{ds2}(t)} \quad (1)$$

$$V_{gs1}(t)=V_{CC1}\left(1-e^{\frac{-t}{R_{g1}\times C_{iss1}}}\right) \quad (2)$$

$$V_{gs2}(t)=V_{CC2}\left(1-e^{\frac{-t}{R_{g2}\times C_{iss2}}}\right) \quad (3),$$

where the $\beta_1$and β_2 are trans-conductance parameters of SiC MOSFET, C_{iss1} and C_{iss2} are parasitic input capacitance. t_p is the time entering into the miller plateau. At the steady on-state, the mismatch on trans-conductance and threshold voltage introduces the current error I_{err_steady} as follows:

When $t \geq t_{steady}$,

$$I_{err\_steady}(t)=\underbrace{\beta_1\left[(V_{CC1}-V_{th1})\cdot V_{ds1}-\frac{1}{2}V_{ds1}^2\right]}_{I_{ds1}(t)}-\underbrace{\beta_2\left[(V_{CC2}-V_{th2})\cdot V_{ds2}-\frac{1}{2}V_{ds2}^2\right]}_{I_{ds2}(t)} \quad (4)$$

$$V_{ds1}=V_{ds2} \quad (5)$$

Note that since V_{gs1} and V_{gs2} less vary during the miller plateau stage, the I_{err_on} always exists in this process. To remove the current error at the turn-on stage, as shown in Fig.3, inserting a small delay time between the driving signals, can re-distribute the drain-to-source current on two MOSFETs. So that the two MOSFETs can have the same current at the miller plateau. The turn-on overshoot can be balanced between two MOSFETs. For static current errors, as shown in Fig. 4, by differentiating the driving voltage, the on-resistance of two SiC MOSFET is changed so that the current can be balanced.

B. Proposed Gate Driver design

The circuit of proposed gate driver is shown in Fig. 5. An isolated power is used to transfer input voltage Vsupply to negative voltage VEE and fixed voltage V_{fix}. A synchronized buck IC is implemented for variable voltage generation. It should be noted that the buck IC is pretty typical with tremendous part numbers from different manufactures. In typical applications, the connection from Rc to FB pin does not exist, and the original output voltage VCCorg is fixed and defined by the R1 and R2 as,

$$\mathrm{VCC_{org}}=V_{FB}\cdot(1+\frac{R_1}{R_2}) \quad (6)$$

where V_{FB} is a fixed voltage value in FB pin and defined by the IC manufacturer. In the proposed design, an extra connection to FB pin is added to make the output driving voltage VCC adjustable, described as,

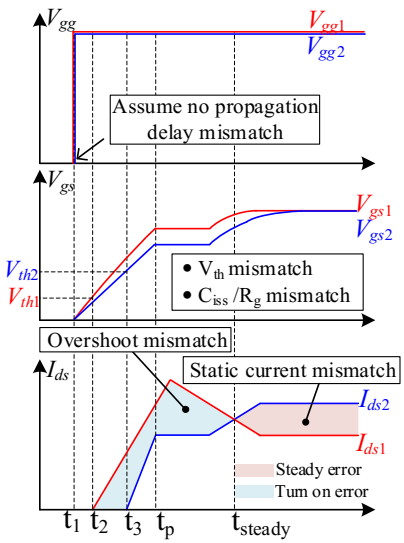


Fig. 2: Turn-on current analysis without current balancing

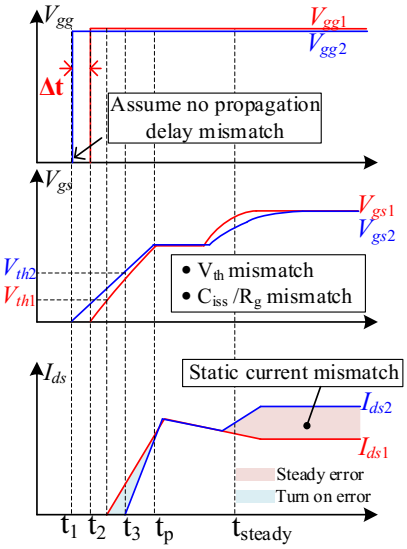


Fig. 3: Turn-on current analysis with only dynamic current balancing.

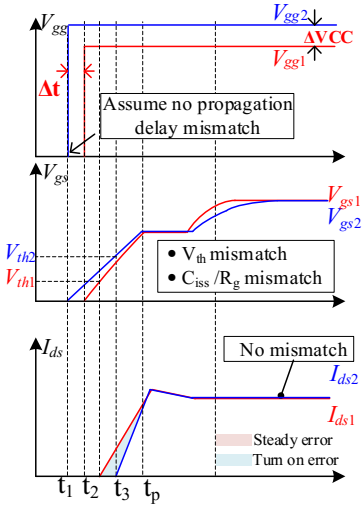


Fig. 4: Turn-on current analysis with both dynamic and static current balancing.

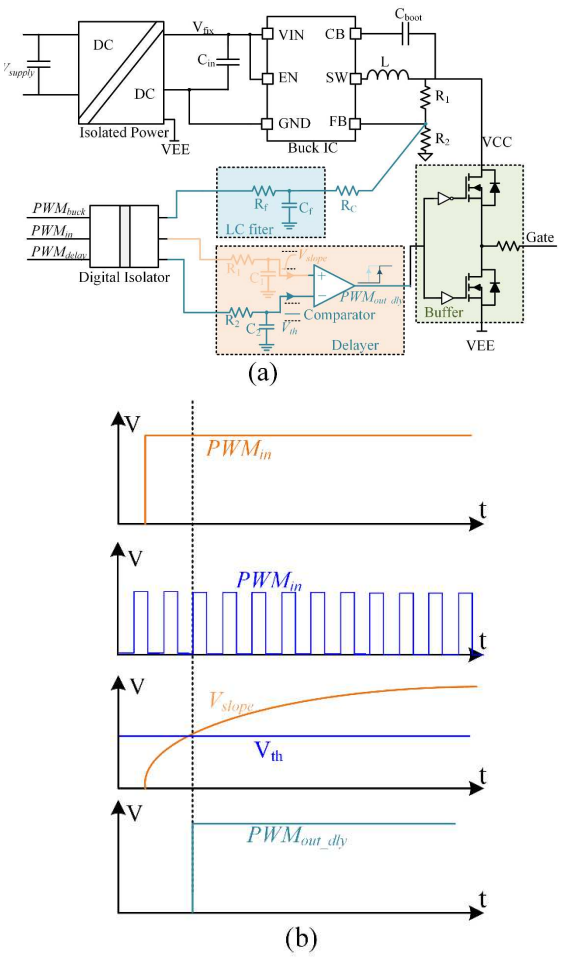


Fig. 5: Proposed gated driver circuit. (a) Block diagram of gate driver (b) Scheme of turn-on delay generation

$$\mathrm{VCC} = V_{FB} \cdot (1+\frac{R_1}{R_2}) - (VDD - V_{FB})(\frac{R_1}{R_f + R_C}) \cdot Duty \quad (7)$$

where *Duty* is the duty cycle of the variable voltage control PWM PWM_{buck}, *VDD* is the secondary side supply voltage of the digital isolator. By changing the PWM duty cycle of PWM_{buck}, the output voltage can be adjusted. Compared with driving a buck converter directly, this approach has two advantages: 1) there is no significant voltage drop caused by load current; hence the driving voltage is more robust. 2) The duty cycle from 0~100% can be assigned to adjust VCC in a specific range (like 16V to 20V) so that a higher resolution voltage adjustment can be realized.

A simple solution for adjustable driving signal delay time is also proposed in Fig. 5. The driving PWM signal PWM_{in} is sent to a digital isolator and then goes through an RC filter formed by R_1 and C_1. It should be noted that the RC filter has a very wide pass-band, so it can slow down the rise time of the PWM to form the waveform V_{slope} as shown in Fig. 5(b). At the same time, a PWM signal PWM_{delay} is sent from the digital isolator to a low pass filter formed by R_2 and C_2. Different from the filter of R_1 and C_1, R_2 and C_2 are designed with very narrow pass-band to generate a dc voltage V_{th} that is proportional to the duty cycle of PWM_{delay}. The two signals V_{slope} and V_{th} Compare to generate the delayed PWM driving signal PWM_{out_dly}. With the change of duty cycle of PWM_{delay}.

III. VERIFICATION

The proposed gate driver is tested in a field test bench, as shown in Fig. 6, and the circuit block diagram is given in Fig. 7. A double pulse test circuit is build with two paralleled SiC MOSFETs as the lower side switches. For higher side switch, a diode is given to maintain the charged current on inductor. The two MOSFETs are driven by two independent gate drivers, respectively. To monitor the drain to source current, two high bandwidth current transformers are installed at the source side. The experiment result is shown in Fig. 8. It can be seen that when there is no current balancing, as shown in Fig. 8 (a), the current error at turn-on and steady state is significant. When the current balancing is enabled, as shown in Fig. 8 (b), the drain to source current of two SiC MOSFETs is exactly the same, which verifies that the proposed gate

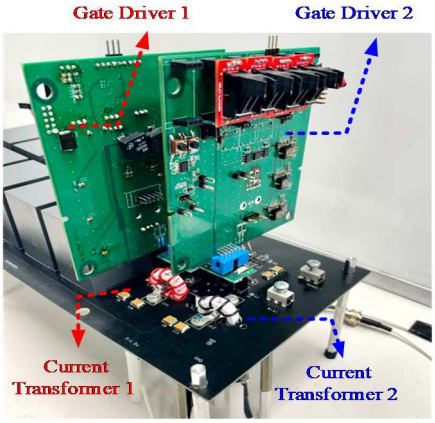


Fig. 6: Test setup for current balancing of paralleled SiC MOSFET.

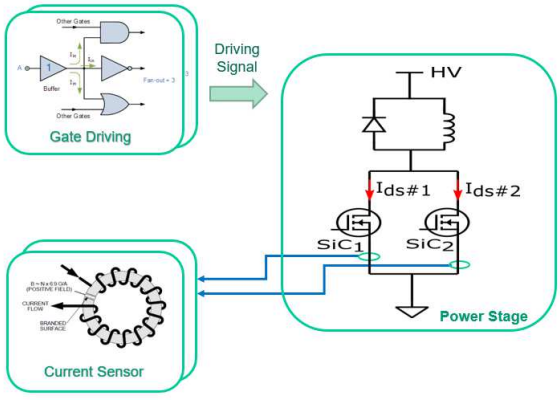
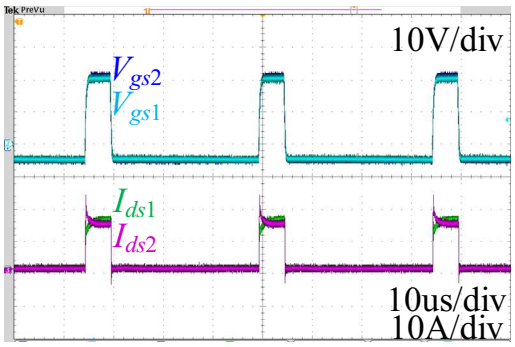
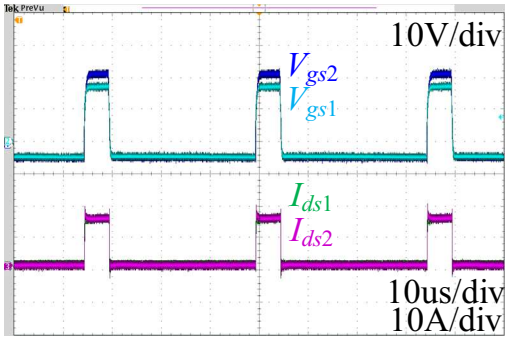


Fig. 7: The circuit block diagram for test setup.

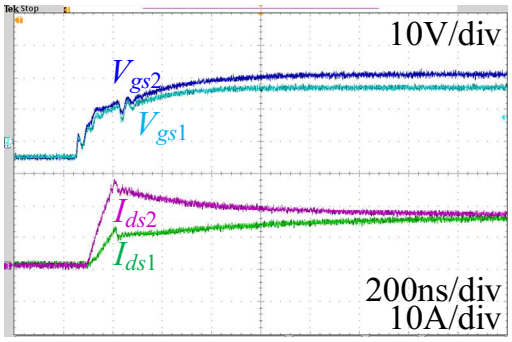
driver can work well. From the zoom-in result of the turn-on transient, as shown in Fig. 5 (c), it can be seen that the current error has a long transition from the miller plateau to the steady state, which causes a significant thermal impact from the turn-on current error. When current



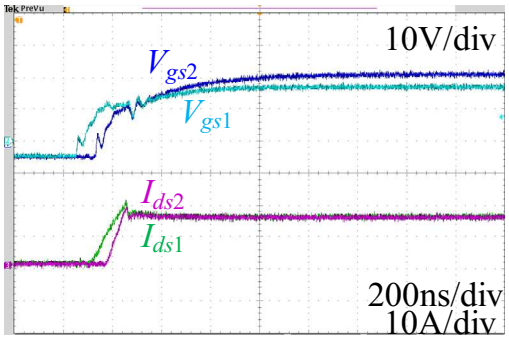
(a)



(b)



(c)



(d)

Fig. 8: Test result for current balancing. (a) Without current balancing. (b) With current balancing. (c) Turn-on transient without current balancing. (d) Turn-on transient with current balancing.

balancing is enabled, as shown in Fig. 8(d), the two current has only a slew rate difference with short duration. The thermal impact caused by this error is minimal and will not further differentiate the junction temperature of the two SiCs.

IV. Conclusions

In this paper, a simple gate driver design is proposed for SiC MOSFET paralleled operations. The driving delay time and voltage level of on-state can be adjusted flexibly without any usage of digital processors; hence it is more cost-effective and reliable for complex EMI environment of high voltage and frequency applications. The operating principle to alleviate the current error of paralleled SiC MOSFETs is described and analyzed. The performance of the proposed gate driver is verified in the test.

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