A 49-63 GHz Phase-locked FMCW Radar Transceiver for High Resolution Applications

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***Abstract*—This paper presents an mmWave FMCW radar that can achieve sub-centimeter-scale range resolution at 14-GHz chirp-bandwidth while maintaining the radar range beyond 50 meters. To meet the requirements on power efficiency, chirp linearity, and signal-to-noise ratio (SNR), a phase-locked stepped-chirp FMCW radar architecture is introduced. Specifically, a fully integrated radar transceiver comprising an interleaved frequency-segmented phase-locked transmitter and a segmented receiver architecture with high sensitivity is presented. The proposed design addresses the limitations of conventional type-II phase-locked loops (PLLs) in extending the radar bandwidth across multiple sub-bands with identical chirp profiles. Fabricated in a 22nm FD-SOI technology, the prototype chip comprises two sub-bands with 14 GHz of free-running bandwidth and 10 GHz of phase-locked bandwidth. The system achieves -101.7 dBc/Hz phase noise at 1 MHz offset, 8 dBm of effective isotropic radiated power (EIRP), 10 dB noise figure (NF), and 362.6 mW collective power consumption of transmitter and receiver arrays.**

***Index Terms*—CMOS, FMCW radar, Coupled PLL, off-chip antenna, range resolution, stepped chirp radar.**

I. Introduction

In light of growing interest in autonomous vehicles, the 60 GHz and 76-81 GHz bands for autonomous vehicle radars have been extensively explored in the past and various implementations of automotive radars have been demonstrated [1]. The range resolution of the state-of-the-art radars is sufficient for the automobile radar design; but cannot meet the requirements for many applications such as synthetic-aperture radar (SAR) imaging, surface roughness detection, material identification, and crack detection in manufacturing plants which demand sub-cm scale range resolution. The urge for improved range resolution has encouraged the development of sub-THz and THz FMCW radars with tens of gigahertz of unlicensed bandwidth and millimeter-scale range resolutions []. However, the inherent propagation loss of the THz frequencies limits the functionality of THz radars for applications that demand tens of meters of detectable range. This notion implies that broadband mm-wave radars below 100 GHz with sub-centimeter-scale range resolution are necessary to realize many of these emerging applications.

The current implementation of mm-wave radars revolve around two popular schemes of signal generation. As shown in Fig. 1(a), in one approach an external FMCW signal generated by direct digital frequency synthesizer (DDFS) is fed to a multiplier chain and a power amplifier (PA) is exploited to boost the output power. This architecture suffers from poor area and power efficiency for two major reasons: (1) The number of multiplier stages increases with frequency because of the difficulty in getting high frequency DDFS, and (2) the gain and efficiency of transistors deployed inside the PA dramatically decrease by increasing frequency. The second approach employs wideband voltage controlled oscillators (VCOs), as shown in Fig.1(b) which alleviates the aforementioned drawbacks. However, due to the lower quality factor of passive components and higher intrinsic noise of the active devices at higher frequencies, the oscillator phase noise deteriorates which negatively impacts the SNR of the intermediate frequency (IF) signal. Moreover, a calibration of external ramp generator is needed in Fig. 1(b) to compensate for the effect of non-ideal K_{VCO} on chirp linearity.

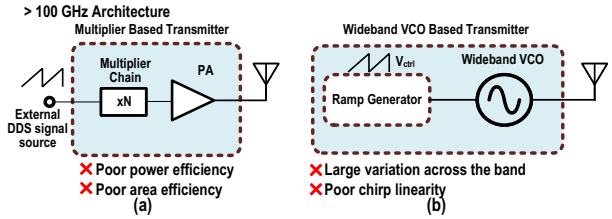

Fig. 1. Wideband radar transmitter deploying (a) multiplier chain, (b) VCO.

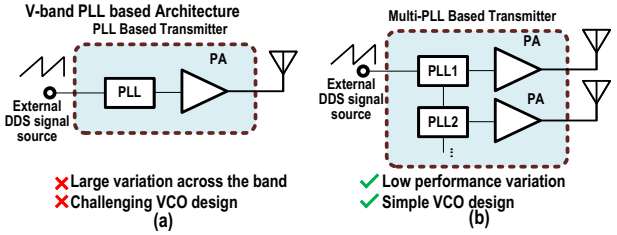

Fig. 2. Wideband radar transmitter deploying (a) one PLL (b) coupled PLL.

To overcome the limitations and disadvantages of conventional designs in Fig. 1, we propose a PLL-based architecture covering 49-63-GHz frequency range. Fig. 2 presents two possible architectures, one based on a single PLL with a large bandwidth (>10 GHz) coverage while the other uses multiple sub-band PLLs coupled together. In Fig. 2(a) the VCO's fractional bandwidth VCO should increase which is challenging at mm-wave frequencies due to dominant effect of device parasitics. Moreover, similar to Fig. 1(b), the variation of output power, phase noise, and K_{VCO} across the bandwidth degrades the radar performance. Alternatively, the coupled-PLL-based architecture in Fig. 2(b) is more effective in achieving bandwidth enhancement while preserving a consistent

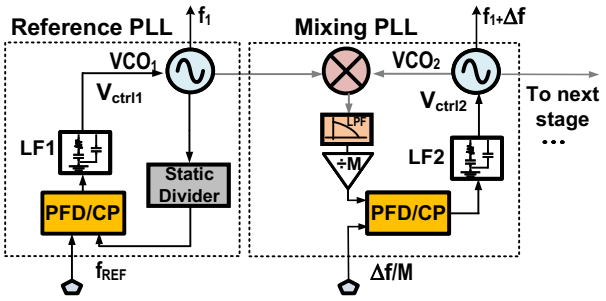

Fig. 3. Proposed coupled PLL system comprising reference and mixing PLLs.

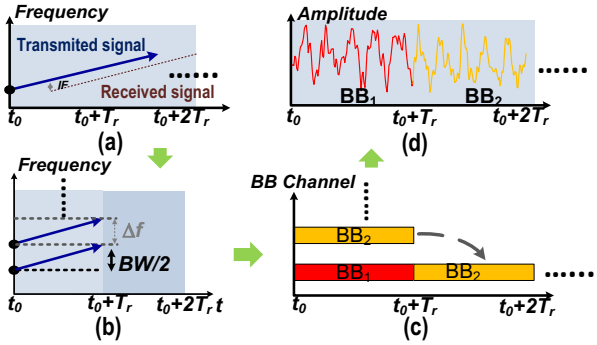

Fig. 4. (a) TX and RX chirps for one PLL, (b) TX and RX chirps of two coupled PLLs, (c) Concatenating two baseband, (d) Time domain waveform.

chirp profile across multiple sub-bands.

II. System Level Architecture

The key idea behind this work is to couple PLLs in a power-efficient fashion to combine multiple sub-bands. The proposed coupled PLL scheme in Fig. 3 consists of a reference PLL and a *mixing* PLL. The outputs of VCO_1 and VCO_2 are mixed and then lowpass filtered to generate the frequency difference component. The coupling through mixing allows several small sub bands to be concatenated and phase-locked with a deterministic phase relationship. To generate N phase-locked sub bands, instead of deploying N type-II PLLs with power hungry dividers, low-power mixing PLLs are introduced which incorporate digital dividers and passive mixers to define a precise phase/frequency relationship among the sub bands.

The proposed coupled-phase-locking technique facilitates the data combining of the baseband signals associated with individual sub-bands, which is briefly studied. Comparing Fig. 4(a) with Fig. 4(b), a single chirp is decomposed into two smaller chirps with identical chirp duration and bandwidth. Due to the deterministic phase relationship, the two baseband signals can be concatenated as shown in Figs. 4(c)-(d), resembling the same baseband achieved by one single PLL.

The proposed system architecture is shown in Fig. 5. The proposed radar comprises 2 transmitters and 2 receivers at 49-56 and 56-63 GHz. The receiver design in this radar is significantly relaxed in light of breaking down the total bandwidth of 14 GHz into smaller 7-GHz sub-bands, which allows for designing low-noise amplifiers (LNAs) and mixers with smaller bandwidth and improved NF.

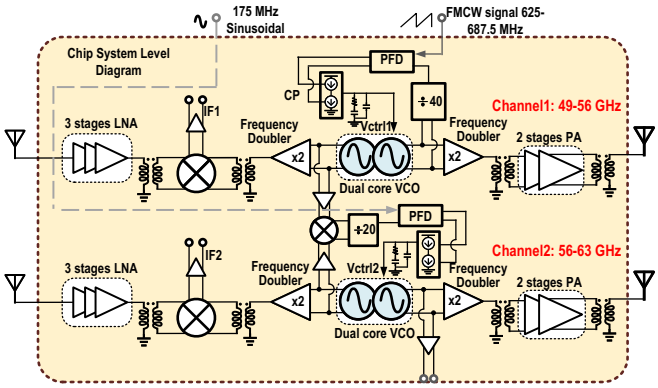

Fig. 5. Chip-level radar transceiver architecture

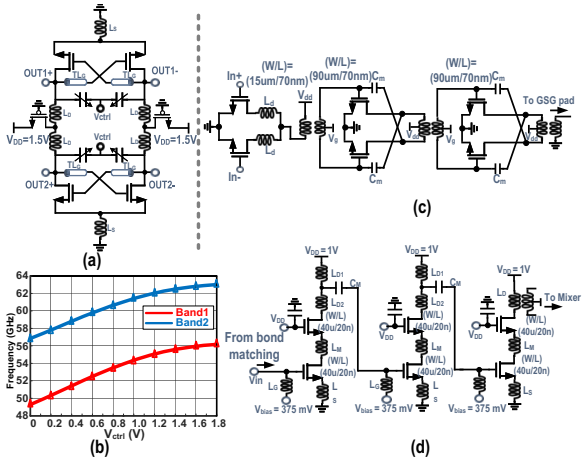

Fig. 6. (a) Dual-core VCO. (b) Measured frequency vs. V_{ctrl} for the VCOs. (c) Doubler and two-stage PA (d) Three-stage LNA.

III. Design of TX and RX Building Blocks

A. TX Building Blocks

Other than the coupled PLLs, the TX chain consists of VCOs, frequency doublers and PAs. The VCO employs a dual-core differential oscillator with transmission line, as shown in Fig. 6(a), to enhance the swing at the gate, enhance the output power and reduce the phase noise. The measured frequency profile of the VCOs in Fig. 6 illustrates the necessity of phase-locked operation to get rid of K_{VCO} nonlinearity. The doublers in Fig. 6(c), converting the VCO outputs at 24.5-28 and 28-31.5 GHz, deploy a push-push configuration for simplicity and sufficient conversion gain. Each sub-band incorporates a two-stage class-A PA with inter-stage matching and $k_f > 1$ across the bandwidth (Fig. 6(c)). The output signal of PAs is fed to series-fed linear patch antenna arrays on package with 7 dBi realized gain. The interface between the chip and PCB is realized by short gold wirebonds. The effect of wirebond is absorbed into the impedance matching networks on both chip and antenna PCB.

B. RX Building Blocks

Each sub-band receiver uses a cascode LNA, shown in Fig. 6(d), an on-chip differential passive mixer, an off-chip antenna, and a baseband amplifier (BA) on the PCB with more than 20

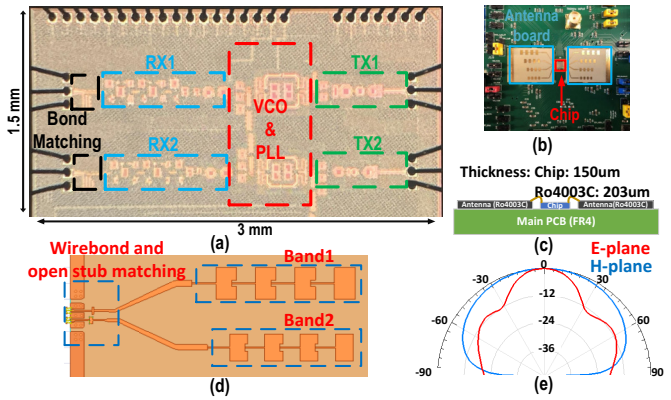

Fig. 7. (a) Chip microphoto, (b) top view, and (c) cross section view of the chip to board connection, (d) antenna structure, and (e) radiation pattern.

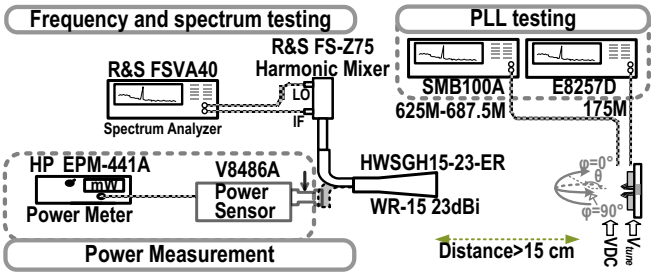

Fig. 8. TX and PLL measurement setup

dB gain and 10 dB NF (excluding BA). The total measured power consumption of each receiver is 20.5 mW.

IV. Measurement Results

The proposed radar transceiver is fabricated in 22nm FD-SOI CMOS technology occupying 4.5 mm^2 of die area, as shown in Fig 7(a). The transmitter and receiver antenna arrays, shown in Fig. 7(b), are fabricated using Rogers 4003C. Each linear-fed antenna array can achieve up to 7 dBi of realized gain and more than 8% radiation bandwidth. As shown in 7(c), the antenna board and chip are glued on top of the platform FR-4 PCB, which also includes the DC regulators and PLL input signal. The top view and radiation pattern of antennas are shown in 7(d) and (e). Two mechanisms in this design provide the isolation of adjacent bands on the receiver side: 1) the band-pass profile of the antennas, (2) the input matching network comprising the board-to-chip interface and input matching of LNA which are designed to only capture the bandwidth corresponding to the sub-band. The antenna board and the chip are connected with short wirebonds (less than 500 μm) which are characterized in HFSS EM simulator to design the chip-to-board interface.

The TX/PLL and RX measurement setups are shown in Figs. 8 and 9, respectively. On the transmitter side, for each sub-chirp the effective isotropic radiated power, bandwidth of free-running and phase-locked operation, and corresponding phase noise profiles were measured, as shown in Figs. 10, 11, 12, and 13, respectively. Compared to free running operation, the frequency difference in phase locked operation is strictly set by the input while the two pair of spurs due to input

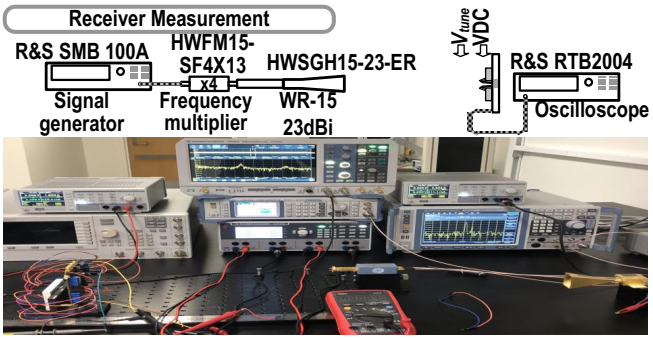

Fig. 9. RX measurement setup

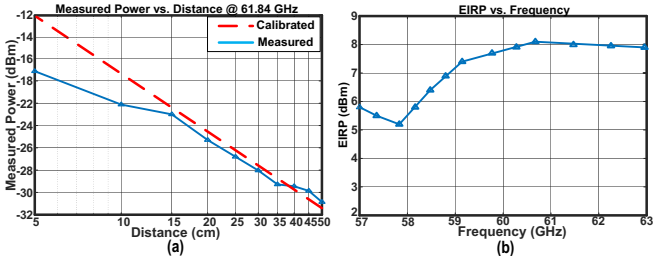

Fig. 10. (a) Close match of power profile with Friis formula at 61.84 GHz (b) Measured EIRP from 57 GHz to 63 GHz

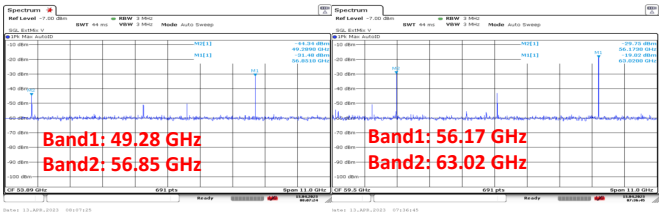

Fig. 11. Free running operation at minimum and maximum frequencies

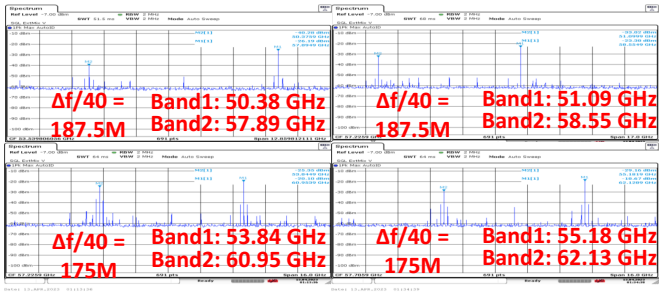

Fig. 12. Phase locked operation at two distinct PLL reference frequencies.

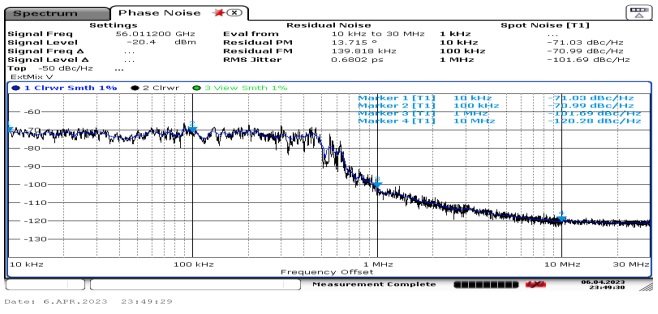

Fig. 13. Phase noise profile at 56.01 GHz

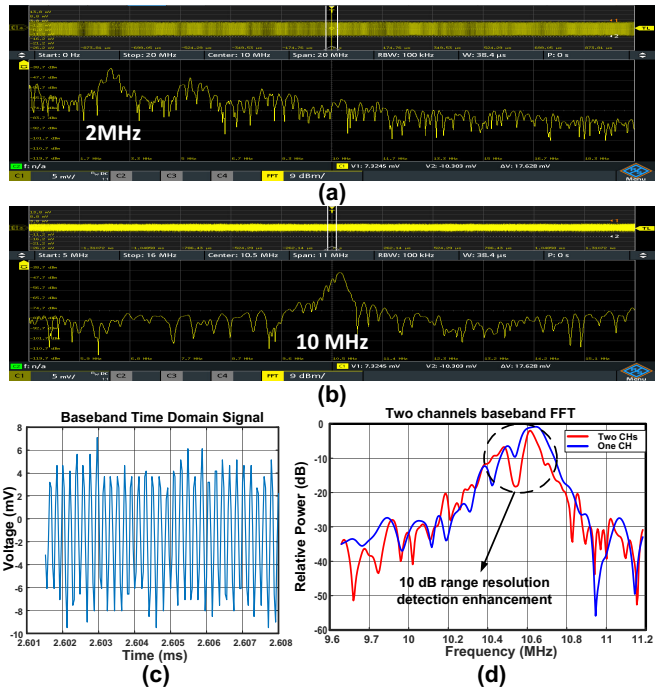

Fig. 14. (a) Baseband FFT at 2MHz and (b) 10MHz, (c) time domain baseband signal, (d) Range resolution enhancement

signals do not deteriorate radar operation. According to the measurement results, the transmitter can achieve a phase-locked radiation bandwidth of 10 GHz with phase noise of -101.7 dBc/Hz at 1 MHz offset. Based on the simulated 7 dBi antenna realized gain, a 4 dBm TX output power is thus estimated, taking into account the 3dB loss for deviated PA output load impedance and chip to antenna loss.

On the receiver side, the output SNR and conversion gain for each sub-band were measured and the baseband spectral and temporal profiles are demonstrated in Fig. 14. Two baseband FFT spectrums corresponding to objects at various distances are shown in Fig. 14 (a) and (b) at 2MHz and 10MHz with over 30 dB SNR, translating to a 10 dB NF of RX chain. In a separate measurement, to examine the range resolution enhancement, we apply FFT on the combined time-domain waveforms of the two sub-bands (Fig. 14(c)). As shown in Fig. 14(d), enhancement in range resolution is achieved by combining the baseband signals.

Table I summarizes the measured power breakdown of blocks and Table II compares the measurement results with prior art. This work outperforms the radars in the same frequency range in terms of phase noise, bandwidth. This design demonstrates the first phase-locked stepped chirp radar

TABLE I
MEASURED POWER CONSUMPTION

Block	PA	Doubler in TX	VCO
$V_{DD}(V)$	1.2	1.2	1.5
P_{dc} (mW)	89.4	45.72	98.25
Block	RX	Doubler in RX	PLL blocks
V_{DD} (V)	1.0	1.2	1.8
P_{dc} (mW)	41	57.96	30.24

TABLE II
PERFORMANCE SUMMARY AND COMPARISON WITH PREVIOUS ARTS

	This work	[1]	[2]	[3]	[4]
Process	22nm FD-SOI	45nm CMOS	350nm SiGe	130nm SiGe	SiGe BiCMOS
NRX/NTX	2/2	4/3	4/2	1/1	1/1
Frequency [GHz]	49-63	57-64	57-64	58.3-63.9	57-64
Architecture	Coupled PLL	PLL	VCO	VCO	VCO
PN [dBc/Hz]@1MHz	-101.7	-93	-105		-80
Bandwidth	14† 10†	4	-	5.6	2
TX P_{out} [dBm]	4	12.1	4(T_{psat})	6.4	6.3
Antenna gain [dB]	7‡	-	-	-	8
RX NF [dB]	10	12.5	9.5	-	13
RX Gain [dB]	20	-	19	-	28
P_{dc} [W]	0.36	3.5	0.99	0.52	0.92
Area [mm^2]	4.5	-	20.25	1.03∗	6.72

† 14 GHz free running bandwidth and 10GHz phase locked bandwidth
‡ Realized gain including matching structure
∗ TX and RX share same antenna

with more than 10 GHz synthetic bandwidth, and 50 meters detectable range.

V. Conclusion

A power efficient phase-locked stepped chirp mm-wave FMCW radar with more than 10 GHz synthetic bandwidth and sub-cm-scale range resolution was presented. On the transmitter side, by incorporating a novel coupled PLL approach, the power consumption was significantly reduced compared to conventional type-II PLLs. On the receiver side, by incorporating non-overlapping frequency bands for each receiver chain, the noise figure penalty of wideband radars was avoided and high isolation between the adjacent sub-bands was achieved. This work demonstrates an integrated FMCW radar with sub-cm-scale range resolution, 50 meter range of coverage, and phase-locked operation. This radar finds application in future generations of automotive radars, crack detection and surface roughness sensors in quality control, and material identification in industrial plants.

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