A 3.7V-to-1kV Chip-Cascaded Piezo-Driver IC Achieving over 96% Reactive Power Efficiency

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***Abstract*— This work presents a modular, scalable switched capacitor (SC) converter with integrated auxiliary boost converter for high-voltage electrostatic and piezoelectric (PZT) actuators such as could be used for microrobotics, haptics and ultrasound applications. Allowing multiple chips to stack and communicate across series voltage domains, the design can interface from 3.7V battery inputs to over 300Vpp/chip (VCR>80). With 3-chips stacked, the design provides up to 1kVpp (VCR>270), delivering and recovering >1W reactive power at >96% efficiency.**

Keywords—Microrobotics; Haptics, Ultrasound; Piezoelectric devices; MEMs; DC-DC converters;

I. Introduction

Due to their small size and versatility, microrobotics and microelectromechanical systems (MEMs) have promising applications in biomedicine, optics, industrial diagnostics, manufacturing and defense [1]–[4]. Electrostatic and piezoelectric actuators have been studied extensively for MEMs, soft robotics, and haptics due to their relatively high energy-density, high bandwidth, and high efficiency at mm- and cm-scale form factors [5]–[7]. Such systems are notoriously challenging due to the need for extreme conversion ratios to reach 100s of volts to kV from system batteries, often with stringent size (<<1cm^3) and weight (<<1g) restrictions [8]–[12]. As typical electrostatic/PZT actuators require significant reactive power (CV^2f_{sw}) to drive a bulk dielectric medium, past work [10]–[12] has shown a need to efficiently deliver and recover reactive energy to minimize system power loss, significantly improving on hard-switching drivers [8] or uni-directional boost circuits [9], [13].

II. Design Overview

Shown in Fig. 1, this work implements a modular/scalable switched capacitor (SC) converter allowing nominally 16-stage reconfigurable series-parallel (SP) chips to be stacked in series voltage domains with low-voltage control signals relayed up the stack to operate as a single high-voltage driver. Similar to [11] and illustrated in Fig. 2, each SP stage reconfigures the state of 15 off-chip flying capacitors sequentially from parallel to series, increasing V_{OUT} in integer steps of ~$V_{IN,SC}$ during actuator charge. While hard charging loss occurs in each step, overall it is reduced by ~ N (the number of steps in the drive sequence) compared to conventional full-swing hard charging [8]. During the mirrored step-down process, the flying capacitors recharge and recover an ideal fraction (N-1)/N of reactive energy stored in the actuator. Due to predominantly reactive power flow, this can be described as a pseudo-resonant process [11]. Here we use metrics: (1) effective quality factor Q_X to capture reactive over real power loss and (2) reactive power efficiency η_X to quantify delivery and recovery of reactive power.

$$Q_X = \frac{P_{OUT,reactive}}{P_{IN,real}} = \frac{C_L V_{OUT,PP}^2 f_{sw}}{P_{loss}} \quad (1)$$

$$\eta_X = \frac{P_{OUT,reactive}}{P_{IN,real}+P_{OUT,reactive}} = \frac{Q_X}{Q_X+1} \quad (2)$$

Compared to the related concept in [11], this work is the first to show modular multi-chip stacking which significantly improves scalability and extends voltage conversion beyond *the SOI buried-oxide (BOX) voltage limit* (here 400V) using only 5V and 32V-rated trench-isolated devices. Compared to [11] which used an unregulated 16-20V benchtop power supply, this

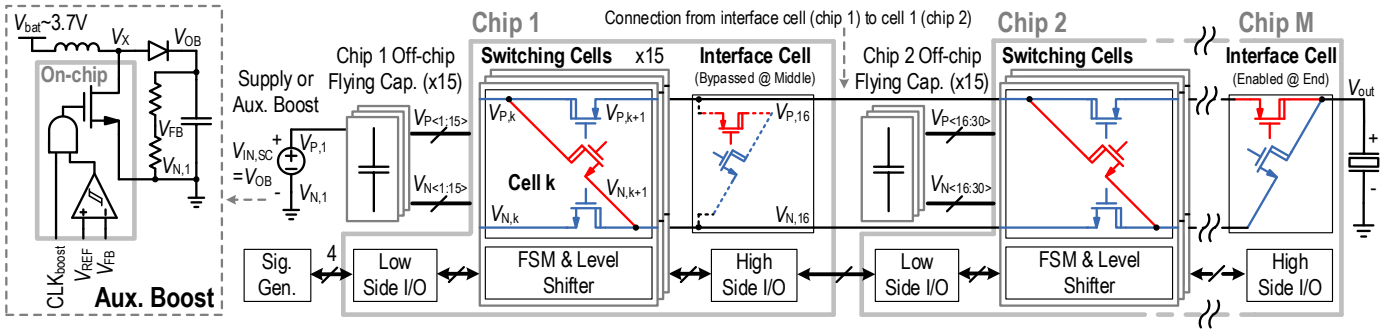

Fig. 1 High level architecture: auxiliary boost drives chip-cascaded reconfigurable series-parallel switched-capacitor converter with off-chip flying capacitors

design uses an integrated auxiliary boost converter to operate with low-voltage 3-3.7V battery inputs. The boost operates in discontinuous burst-mode operation with feedback to provide voltage regulation with low quiescent power. With typical output $V_{OB} = V_{IN,SC}$ = 20-30V (6-8x step up), the boost remains efficient with a physically small inductor.

III. Topology Overview

Fig. 3 shows the chip I/O interface circuitry. Four differential digital signals are processed through chip-boundary I/O: CLK (triggers FSM), UD (indicates whether in step up or down mode), SP (whether the next cell is in series or parallel) and MC (whether the current chip is connected to the load). At the chip input, only UD and CLK are needed to control switching.

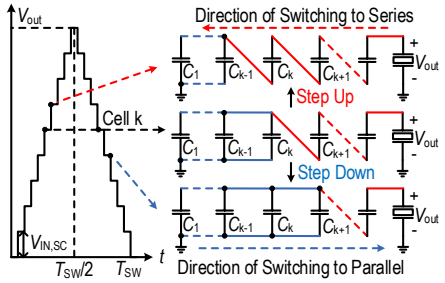

Fig. 2 Represented pseudo-resonant operation

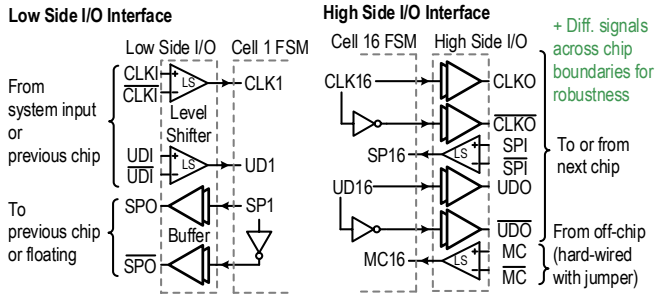

Fig. 3 Chip I/O interface circuitry

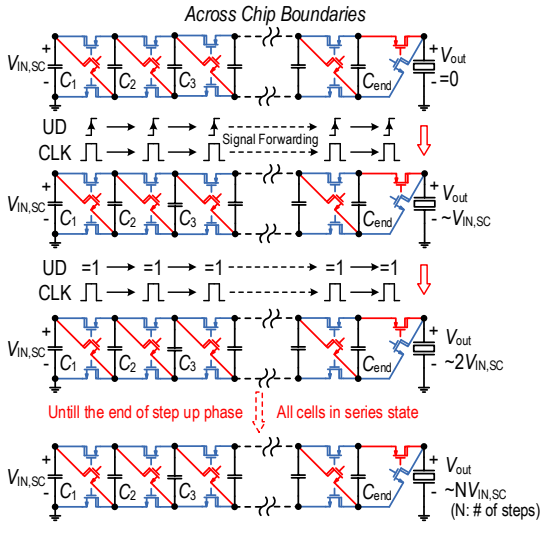

Fig. 4 Equivalent circuit and daisy chain control process during step up (step down is the dual process of step up)

Fig. 4 shows the daisy chain control process. At initial step-up, all parallel (blue) switches are on (V_{OUT} = 0V); signals UD and CLK are forwarded up the stack. With UD=1, when the CLK edge propagates to the last parallel cell in the stack, it switches to series (red switch on); this cell sets SP=1 which is passed to the previous cell. At the next CLK edge, the previous cell switches to series; thus with UD=1, at each CLK edge the parallel-series state transition ripples down from last cell to first cell. During step down (UD=0), UD and CLK only pass through parallel cells. Thus, at CLK events, the series-parallel transition ripples up from first cell to last cell. The interface cell (Fig. 1) is only used in the last chip to connect to the load; for other chips it is bypassed/unused. To inform chips of their position in the stack, signal MC is hardwired (PCB jumper to V_{REGN} or V_N of the last cell in middle and last chips respectively).

IV. Circuit Implementation

Fig. 5 shows local circuitry within each switching cell including FSM logic, local level shifters, gate drivers, power switches, and a local linear regulator (LDO). The LDO is needed for low-side and high-side supplies V_{REGN} (~4V above V_N) and V_{REGP} (~4V below V_P), which provides local voltage operating domain for FSM and gate driving. Fig. 6 shows the schematic of the class-B LDO with pseudo-bandgap reference. The pseudo-bandgap reference uses a MOS-degenerated 5V depletion device to form a pseudo-PTAT current reference (~250nA); when passed through a weak inversion diode MOS stack, it forms a pseudo-bandgap reference for the class-B LDO output. The class-B LDO, M_{L5N}, M_{L32P} for V_{REGP} and M_{L5P}, M_{L32N} for VREGN, is used to maintain the output voltage within one

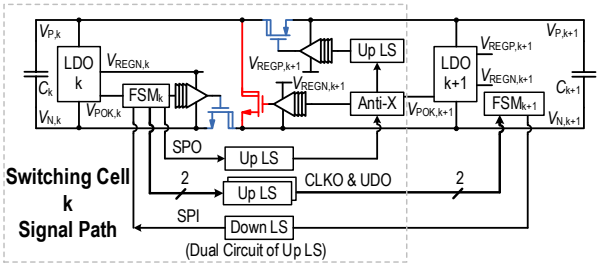

Fig. 5 Key circuit blocks in each unit switching cell

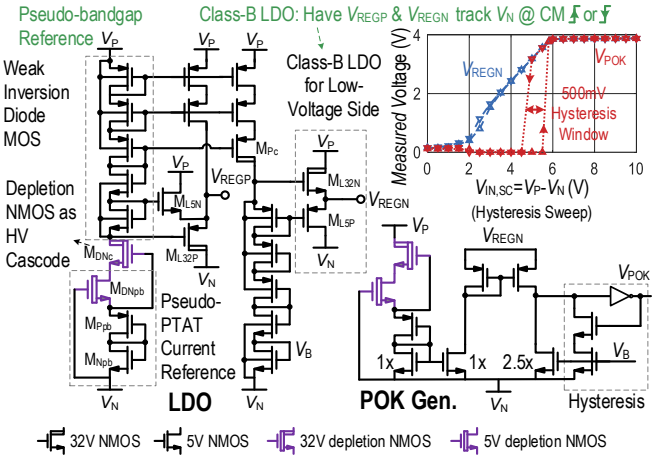

Fig. 6 Schematic of the class-B LDO with pseudo-bandgap reference and measured output voltage, V_{REGN}, and POK versus cell voltage, $V_{IN,SC}$

threshold voltage during the transit when the parasitic capacitance between the output nodes to the handle wafter gets charged or discharged due to the changing common mode. A 32V depletion cascode, M_{DNc}, shields the reference from $V_{IN,SC} = V_P - V_N$, nominally 20V-30V. A replica of the PTAT current reference between V_P and V_N is used for a power OK (POK) circuit to generate logical FSM reset and monitor the $V_{IN,SC}$ voltage level (resetting FSM state to parallel if low voltage detected). Measurement shows POK triggers when $V_{IN,SC}$ reaches ~6V; a 500mV hysteresis window prevents POK chatter.

Fig. 7 shows the schematic of local up level shifters. Level shifters use a floating latch with 32V cascodes to block voltage domain differences. A NAND-latch is used to lock state and reject common mode transients (charge on parasitic BOX capacitance C_{tub}) during step up/down. $INV_{a1,b1}$ are skewed with weak NMOS and strong PMOS for a lower threshold voltage to have fast response for low-high switching. However, $INV_{a3,b3}$ has strong NMOS and weak PMOS such that the PMOS can easily be overdriven $M_{Pa,b}$ during switching and the NMOS can discharge C_{tub} fast when the common mode voltage decreasing. High-side PMOS $M_{APa,b}$ is pulse-triggered during switching to accelerate latching (charge C_{tub} and other parasitics).

Fig. 8 shows a NAND-latch based chip-boundary level shifter. Chip-boundary level shifters are differential latching to overcome V_{REGN} mismatch across chips and use logical blanking to reject common mode errors.

V. Experimental Results

Fig. 9 shows a die photo and board level implementation. Total die area is 1.7mm^2 including 15 switching cells, interface cell, auxiliary boost converter (used only on the first chip), I/O and ESD. The testing platform includes three chips cascaded in a vertically-stacked assembly. The low voltage (3.7V ground-referenced) input is connected to the top chip while the output is located at the bottom. System ground passes through the peripheral headers around the assembly for shielding and safety but is only connected as reference for the first chip.

Fig. 10 shows time-domain measurements for a scenario with 3-chips cascaded, operating with the auxiliary boost for 3.7V-to-1kV conversion. The boost runs in discontinuous conduction mode (DCM) with hysteretic burst-mode control. When the boost output voltage V_{OB} is below a provided reference, it switches with fixed duty cycle and frequency of 1MHz (constant peak inductor current ~30mA). This provides charge and increases voltage $V_{IN,SC,1}$ of the first chip in the stack. When the SC stage is stepping up, providing charge to the load, $V_{IN,SC,1}$ decreases turning on the boost; thus the boost converter mainly operates during step up. When the boost output V_{OB} reaches the reference + hysteresis, it stops switching (effectively enters standby mode). During step-down, charge from the dominantly capacitive load is recovered (to the flying capacitors) such that the boost remains idle. Energy recovery in the SC stage can be seen in that during step down, flying capacitor voltage(s) are increasing as showing in Fig. 11. More energy is transferred and recovered in capacitors close to the load as seen in their larger voltage swing.

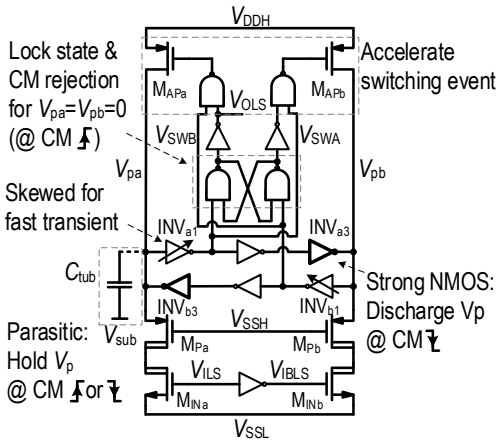

Fig. 7 Schematic of the local up-level shifter in each unit switching cell (local down-level shifters are the dual)

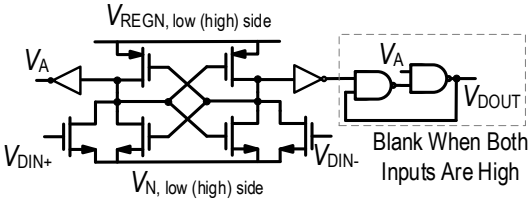

Fig. 8 Schematic of the NAND-latch based chip-boundary level shifter

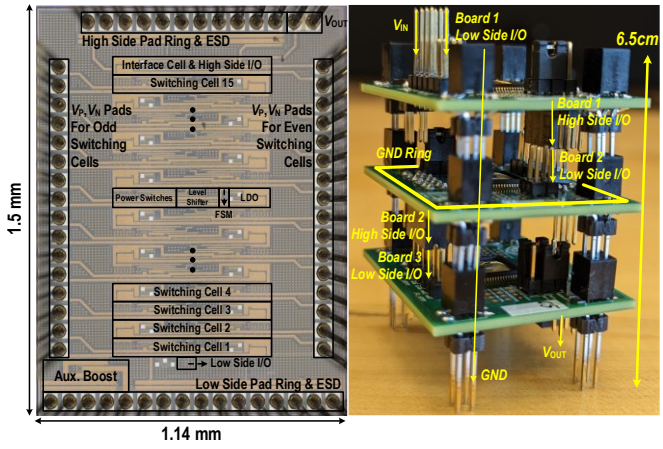

Fig. 9 Annotated die photo and the board level implementation showing chip-chip interconnect

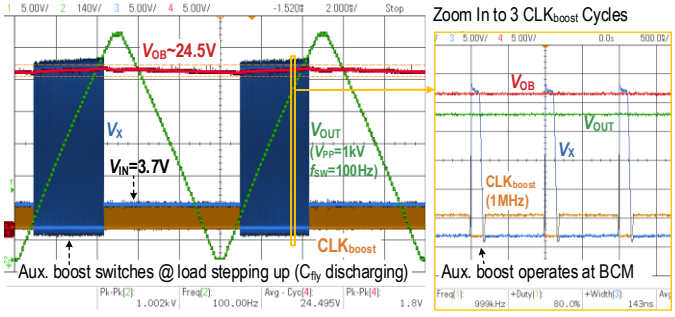

Fig. 10 Waveform of 3-chip cascaded SC w/ aux. boost driving 2nF load capacitor

Fig. 12 shows the efficiency of the aux. boost converter for different output power and different output voltages. Peak efficiency η_{boost} is ~89% and is above 80% for most of the useful range. However, boost efficiency only marginally impacts overall converter metrics due to the benefit of the associated SC stage. Based on (1) and (2), combining the auxiliary boost and SC, the performance of the converter can be quantified as

$$Q_{X,tot} = \frac{P_{OUT,reactive}}{P_{IN,real}} = \frac{P_{OUT,reactive}}{P_{SC,real}/\eta_{boost}} = Q_{X,SC} \cdot \eta_{boost}, \quad (3)$$

$$\eta_{X,tot} = \frac{P_{OUT,reactive}}{P_{IN,real}+P_{OUT,reactive}} = \frac{Q_{X,SC}\cdot\eta_{boost}}{Q_{X,SC}\cdot\eta_{boost}+1}. \quad (4)$$

It can be seen in (4) that η_{boost} leads to only a modest impact on efficiency $\eta_{X,tot}$ as long as $Q_{X,SC} \propto$ #steps, N, is high. Effectiveness of the daisy-chain relay is also highlighted in Fig. 13 which shows measured CLK signals as they are propagated across three stacked chips. At the rising/falling edge, total propagation delay through 16 cells from Chip 1-2 and 2-3 is roughly 60ns. This includes 16 level shifters and FSM logic blocks per chip, indicating fast switching of the daisy-chain-relay.

Fig. 14 shows measured $V_{OUT,PP}$ versus $V_{IN,SC}$ for 3-chip cascaded operation when driving calibrated class-I COG capacitor loads from 20pF to 5nF. The foundry-defined BOX and MOSFET voltage rating (400V/chip and 32V respectively) and measured breakdown limits (550V/chip and 40V resp.) are shown to highlight the reasonable operating range. Note that while the converter was able to drive output voltage exceeding the rated BOX and device limits without measurable leakage at room temperature (>1.5kV), here we only quote performance up to rated limits. For detailed testing and characterization, a derated limit of 1kV is used, regulated with $V_{IN,SC}$ or V_{OB}, while switching frequency was swept to adjust output power. Reliable switching frequencies extended well over 10kHz for 3-chip operation (depending on load cap and fast-switching limit FSL).

As showing in Fig. 15, driving C_L = 2nF, the 3-chip cascaded SC with auxiliary boost achieves Q_X ~ 31.8 ($\eta_{X,peak}$ = 96.9%) at roughly 1W reactive power. At peak power of ~4.5W it achieves η_X ~ 96%.

Table 1 compares this work with prior art. This work achieves higher performance metrics Q_X and η_X than past work. Importantly, for an efficient pseudo-resonant design, it achieves VCR = V_{OUT}/V_{IN} > 80 per chip, with highest output power and switching frequency. While additional components are needed (higher volume) for the boost stage, compared to [4] this work achieves ~2-3x higher volumetric and gravimetric power density. Importantly, the design provides a modular/scalable pathway to achieve high drive voltages efficiently for a variety of electrostatic/PZT actuator devices.

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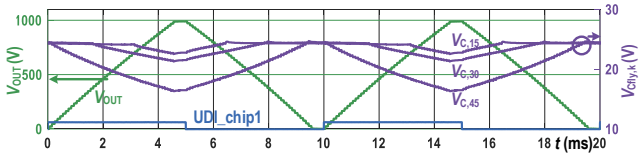

Fig. 11 Waveform of output voltage and voltages on flying capacitor at the end of each chip

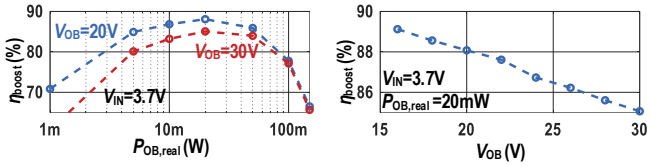

Fig. 12 The efficiency of the aux. boost at different output power and different output voltages

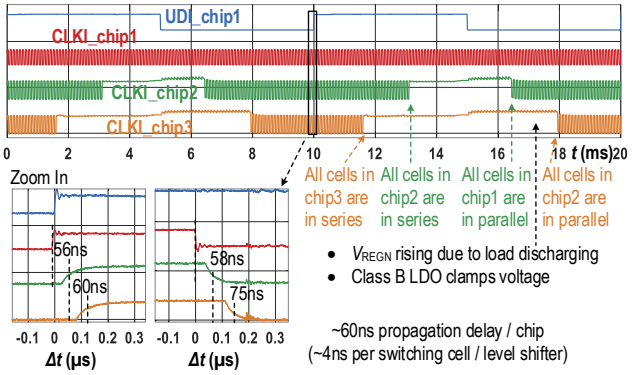

Fig. 13 Measured digital signals across different chip boundaries

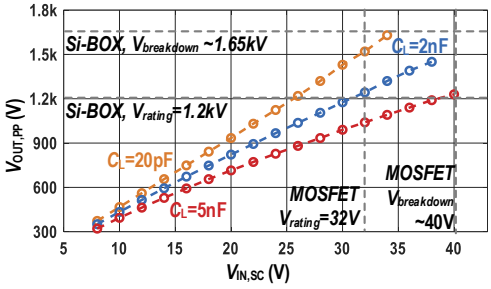

Fig. 14 3-chip cascaded SC transfer characteristics at 100 Hz

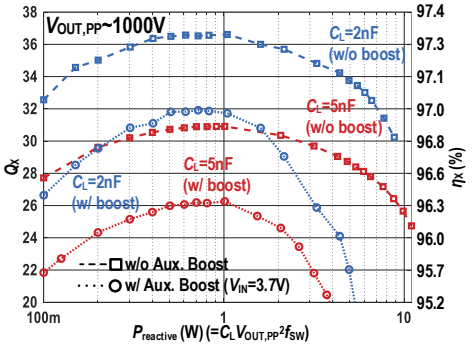

Fig. 15 Measured Q_X and η_X for 3-chip cascaded SC with 1kV $V_{OUT,PP}$

TABLE I. PERFORMANCE SUMMARY AND COMPARISON TO PRIOR ART

	Rentmeister VLSI20 [8]	Park ECCE [9]	Chaput ISSCC17 [10]	Li ISSCC21 [11]	**This work**
Topology	Hard Switching	Unidirectional Boost	Bidirectional buck-boost	Switched Capacitor (SC)	**3-chip cascaded SC w/ Aux. Boost**
Process	1µm SOI BCD	Discrete	0.18µm HV SOI	1µm SOI BCD	**0.18µm SOI BCD**
V_{IN} (V)	310	3.7	3.6	16 - 20	**3.7**
$V_{OUT,PP,max}$ (V)	310	2700	100	300	**1000**
VCR	1	730	27.8	15	**270**
C_L (nF)	0.04 - 1	N/A(2)	100 – 330	0.1 - 10	**0.02 - 5**
$f_{SW,max}$ (kHz)	1	0.04	0.2	1	**>10**
Passive components	1206 cap	1:11 Transformer + 4.7µF + 0603 cap x10 + 0201 cap x109	100µH + 10nF	0402 cap x16	**100µH + 27µF(4) + 0402 cap x48**
Weight(1) (mg)	38	178.6(3)	105.7(3)	49.6	**175**
Volume(1) (mm^3)	8.5	35.5(3)	29.1(3)	9.4	**35**
$P_{OUT,max}$ (mW)	80	162(2)	495	400	**4500**
Power Density (mW/mg) (1)	2.1	0.9(2)	4.7(2)	8.1	**25.7**
Power Density (mW/mm^3) (1)	9.4	4.6(2)	17.0	42.6	**130**
$\eta_{X,peak}$ (%)	49.8	34(2)	83.7	91.2	**96.9**
$Q_{X,peak}$	0.99	N/A(2)	5.1	10.3	**31.8**

(1) Metrics are based on passive component weight & volume only (chip weight/volume is generally negligible, PCB package/assembly size is difficult to quantify and depends on PCB/assembly technology, therefore misleading to compare)
(2) Design in [2] was tested with a resistive (40MΩ) load; thus reactive power metrics are not applicable; real power & efficiency are reported here.
(3) Does not include size/weight of active components and/or bypass capacitors (although these may be significant)
(4) Derated to 3.7V

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