# High-Density High-Power Converter using 3.3-kV All-Silicon Carbide Modules

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***Abstract*—This work presents the development and validation of a high-power two-level converter using the latest 3.3 kV silicon carbide (SiC) module, in the 100 mm × 140 mm half-bridge package, aiming at high performance and high volumetric power density. The laminated busbar design together with the selection of the DC link capacitors are discussed, which leads to a compact busbar/capacitor assembly with low parasitic inductance in the current commutation loop. Switching test results are presented to show the low stray inductance. Thermal management is discussed to embody the superior performance of SiC modules versus state-of-the-art Si IGBT modules in terms of power density. Finally, the experimental results at 1800 V DC bus voltage with switching frequency sweeping are presented to verify the feasibility of the proposed design.**

**Keywords—Medium voltage, high-power converter, power density, SiC MOSFET modules.**

## I. Introduction

With the maturing of medium voltage (MV) silicon carbide (SiC) technology, commercial MV SiC modules, especially 3.3 kV modules, have started to replace their silicon counterparts, such as the Si IGBT, in high performance applications, which demand high power density, increased lifetime and/or reduced system costs. The MV SiC technology can contribute to this trend since it offers considerable advantages over their silicon counterparts such as faster switching speed, lower losses, the ability to operate at higher temperature and the potential to achieve higher power density [1]. These merits enable the device to switch at higher frequencies thus improving the system characteristics, e.g., reducing the passive component size and total harmonic distortion (THD), increasing system efficiency, etc. Moreover, the higher thermal capacity of the SiC device enables higher operating temperatures, which further simplifies the thermal management design for the converter, compared to the converter using silicon-based devices. This contributes to a higher power density for the entire system.

Recently, with the advancement in packaging technology, many 100 mm × 140 mm half-bridge modules have been released, which have started to take over the state-of-the-art 140 mm × 190 mm IGBT package in some MV applications. The half-bridge package, an example is shown in Fig. 1, can accommodate the higher switching speeds of the SiC MOSFET due to the significantly reduced module parasitic inductance. The laminated positive and negative terminals is a key feature to reduce the stray inductance. In addition, it can also enable a straightforward low inductance external bussing design.

In this paper, the design and validation of a high-power high density three-phase inverter using the latest 3.3 kV modules are presented. The proposed inverter system can be used as the power stage in many applications, such as traction applications for railway systems [2] and heavy-duty off-road vehicles, aerospace propulsion drives [3],[4], central inverters for solar and wind [5], etc. The 3.3 kV SiC MOSFET module from Wolfspeed [6] is used in this work for converter demonstration. The overall volume of the inverter is approximately 15 liters. The maximum output power is close to 1 MW with a premium power density over 50 kW/L. Experimental results are presented in this work to show the lower losses and reduced THD enabled by the SiC devices during the continuous operation test.

Fig 1. Photograph of the 100 mm × 140 mm LM3 package from Wolfspeed.

## II. Power Stage Design

The proposed converter is designed using power modules packaged in the industry standard 100 mm × 140 mm package. Hence, it is compatible with many commercially available silicon IGBT and/or SiC MOSFET power modules.

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TABLE I. COMPARISON AMONG DC-LINK CAPACITORS FOR THE CONVERTER PROPTOTYPE

| DC voltage | Capacitor configuration | Total capacitance | Total rms current @ 55 °C, 10 kHz | ESR | $R_{th,\ cap}$ |
|---|---|---|---|---|---|
| 1500 V | 2 × LH30BT317 | 620 µF | 312 A | 1.27mΩ | 1.6°C/W |
| 1800 V | 2 × LH30BX247 | 480 µF | 290 A | 1.46mΩ | |
| | 2 × LH30CA207 | 400 µF | 282 A | 1.58mΩ | |

In this work, the LM3 3.3 kV half-bridge all-SiC power module from Wolfspeed is used. It is rated for 800 A with a 2.65 mΩ on-state resistance at 25 °C. Fig. 2 shows the three-dimensional (3D) rendering of the inverter highlighting the different components, while Fig. 3 is a photograph of the actual converter prototype used in the experimental study. The three (3) half-bridge modules are placed on a custom cold plate, which has a thermal resistance of 10 K/kW. The modules are driven by custom gate drivers optimized for MV SiC modules. The DC-link consists of a heavy copper laminated busbar and two (2) capacitors with low inductance in parallel. The AC terminals are also realized using heavy copper bars. The overall dimensions of the converter are 385 mm × 335 mm × 115 mm, which yields a volume of 15 liters.

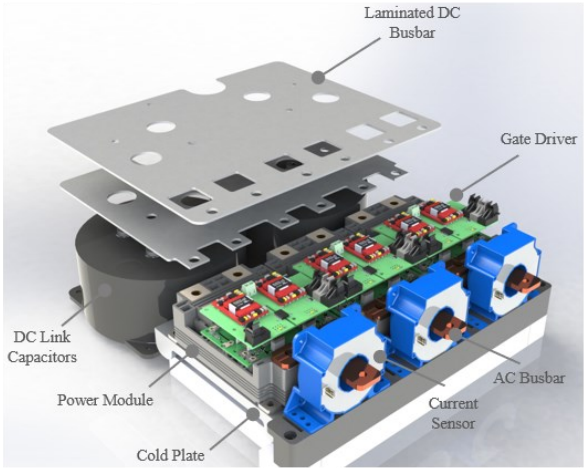


Fig. 2. 3D rendering of the converter [7].

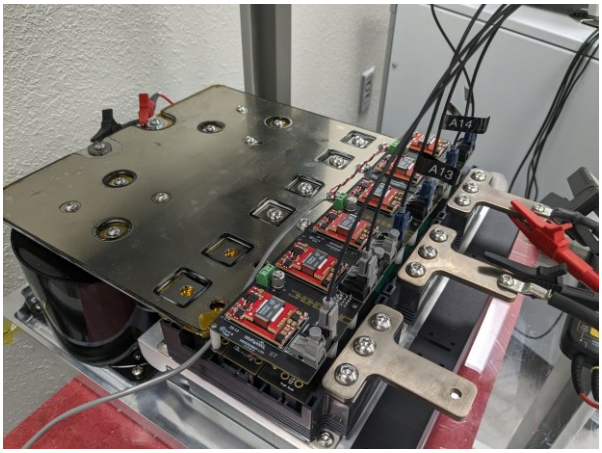

Fig 3. Photograph of the 2-level converter prototype.

The DC busbar is designed to ensure low stray inductance in order to eliminate the need for extra decoupling capacitors while maintaining a very low voltage overshoot. This is achieved by using two nickel-plated 3/32" thick 110 copper laminates, one for DC positive and the other for DC negative. They are separated by two 3-mil thick sheets of PEI insulation film. This minimizes the distance between copper layers and reduces overall inductance of the busbar while meeting the insulation requirements. Using two sheets of insulation increases converter reliability by reducing the chances of breakdown due to pinhole imperfections in the sheets or during its application.

The DC-link capacitors are a critical part of the converter design, and they are a major component that can substantially affect the power density and the performance of the converter. Traditionally, a number of cylindrical film capacitors must be connected in parallel in order to meet the rms current requirement [8], which adversely affects the power density of the converter. Therefore, in this work, two film capacitors, the LH3 series from Electronic Concepts [9], are used to form the capacitor bank in the DC link. They are characterized by their high current capability, very low equivalent series inductance (ESL) in a small package. Table I shows different capacitors from the LH3 series that can be connected to the busbar at each voltage node and their associated rms current limits. It should be noted that currents higher than in the given table could be achieved if active cooling for the capacitors is employed. In this design, the capacitors are not actively cooled for simplicity.

To validate the bussing design, double-pulse tests are carried out using one module connected to the busbar. Fig. 4 shows the switching waveforms taken from the double-pulse test at the rated condition of the power module, i.e., 1800 V DC bus voltage, 600 A load current and 150 °C junction temperature. The slew rates as shown in the figure were 9.3 V/ns and 18.0 V/ns during turn-on and turn-off, respectively. The estimated stray inductance from this test was roughly 20-25 nH (with one power module mounted on the busbar); this means that the stray inductance from the busbar and capacitors assembly is around 10 - 15 nH. Additionally, it is clear from the figure that there is still room to further increase the slew rates without causing oscillations or exceeding the SOA of the power module.

## III. THERMAL CONSIDERATIONS

### *A. Power Modules Thermal Performance*

The module's thermal performance is evaluated using PLECS simulation. A thermal model of the power module is constructed from its static and dynamic characterization data

[6]. The slew rates of the MOSFETs were slowed to ~ 9.3 V/ns and ~ 12.2 V/ns for turn-on and turn-off, respectively, in order to be comparable with IGBTs. Table II lists the conditions for this simulation.

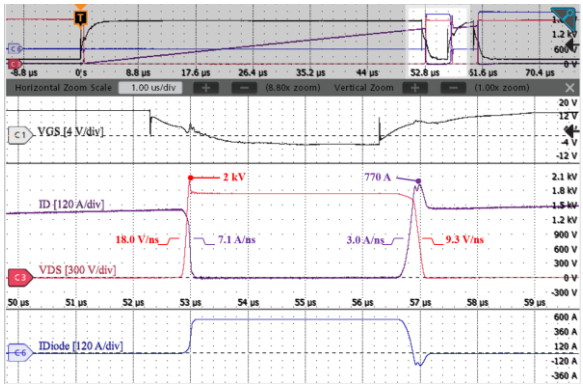


Fig 4. Transient switching waveforms of the 3.3 kV LM3 module at $T_{vj}$ = 150 °C, $V_{DC}$ = 1800 V and $I_D$ = 600 A with $R_{g\text{-}on}$ = 3.3 Ω and $R_{g\text{-}off}$ = 2.5 Ω.

TABLE II PARAMETERS USED IN THE SIMULATION

| Parameter | Value |
|---|---|
| DC voltage | 1500 or 1800 V |
| Switching frequency | 2–10 kHz |
| Line voltage | 690 or 1100 $V_{rms}$ |
| MOSFET $R_{th\text{-}jc}$ | 33.0 K/kW |
| IGBT $R_{th\text{-}jc}$ | 20.5 K/kW (IGBT) |
| | 34.0 K/kW (Diode) |
| $R_{th\text{-}ca}$ | 10 K/kW |
| $R_{th\text{-}cs}$/switch | 2.5 K/kW (λ=4 W/m-K, D = 70 µm) |
| Dead time | 2 µs |
| Ambient temperature | 40 °C |

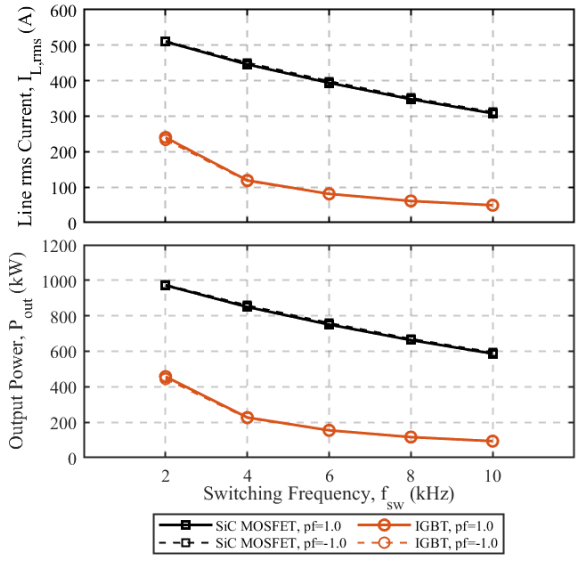


Fig. 5. Converter output rms current and output power as a function of switching frequency under $V_{DC}$ = 1800 V and $V_{LL,rms}$ = 1100 V.

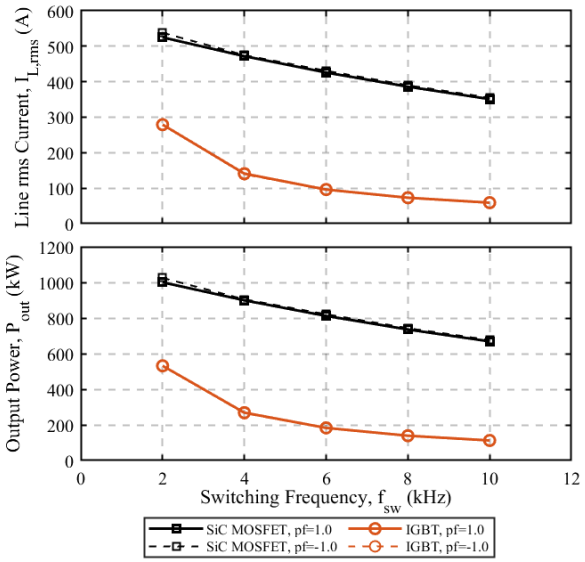


Fig. 6. Converter output rms current and output power as a function of switching frequency under $V_{DC}$ = 1500 V and $V_{LL,rms}$ = 690V.

Figs. 5 and 6 show the maximum converter rms current and the corresponding output power for both the IGBT-based and the SiC-based converters in bother the inverter and rectifier operating modes. Two different DC bus voltage scenarios are investigated, i.e., 1500 V and 1800 V, with corresponding rated output line-to-line voltage of 690 V rms and 1100 V rms, respectively. The maximum allowable junction temperature of the IGBT/diode and the SiC MOSFET is set to 155 °C to identify the maximum line current at a certain switching frequency. It is clear that the SiC MOSFET can outperform the IGBT mainly due to its low switching loss—even with relatively low slew rates. Therefore, for the same converter power stack, a much higher output power can be obtained by using the SiC MOSFET power modules and hence higher power density.

### *B. DC-Link Capacitor Thermal Performance*

The capacitor rms ripple current for a 2-level converter using space-vector PWM can be estimated using (1) [10], which only considers the ripple as a result of the converter.

$$I_{C,rms} = I_{Line,rms}\sqrt{2M\left[\frac{\sqrt{3}}{4\pi} + \left(\frac{\sqrt{3}}{\pi} - \frac{9}{16}M\right)cos^2(\emptyset)\right]} \quad (1)$$

From (1), it can be deduced that the highest $I_{C,rms}$ for a given $I_{Line,rms}$ is at unity power factor and $M \approx 0.61$.

Figs. 7 and 8 show the rms current stress on the capacitors calculated from (1) with the corresponding currents shown in Figs. 5 and 6, respectively. The capacitor temperature is calculated from (2), assuming 40 °C ambient temperature, and is overlaid in Figs. 7 and 8 showing that the capacitor temperature stays under 105 °C, which is the maximum operating temperature for these film capacitors.

$$T_{cap}(°C) = T_a(°C) + R_{th,cap}({I_{C,rms}}^2 \times ESR) \quad (2)$$

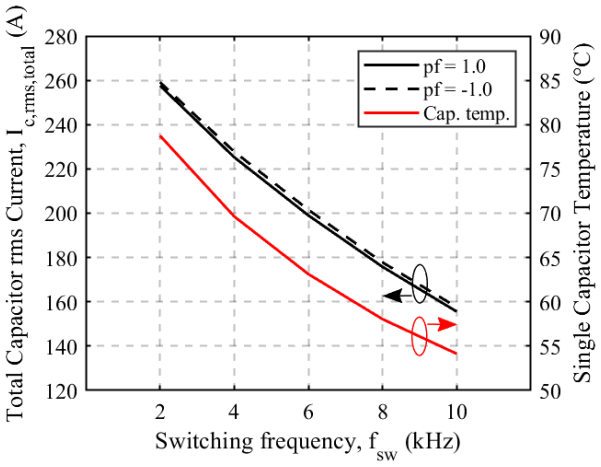


Fig. 7. Capacitor rms current and temperature under $V_{DC}$ = 1800 V.

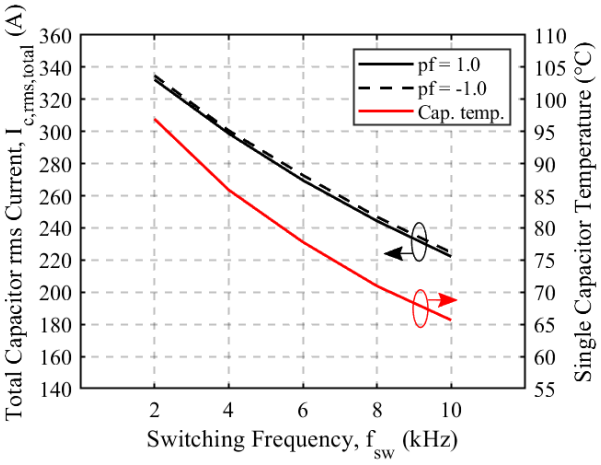


Fig. 8. Capacitor rms current and temperature under $V_{DC}$ = 1500 V.

## IV. Experiment Studies

To validate the operating ability of the prototyped power stage, the continuous power test is conducted. The converter is operated under 1.8 kV DC-link voltage with other key parameters listed in Table III. A reactive load is used to reduce the requirement for the power source, which only supplies the loss from the power stage and load parasitic resistances. To investigate the influence of switching frequency on the system, the inverter is tested at 1, 4, 6, and 8 kHz, with 3.3 Ω external gate resistors.

Table III. Parameters Used in the Experiment

| Parameter | Value |
|---|---|
| $V_{DC}$ | 1800 V |
| Modulation Index | Up to 1.0 |
| Load | 10 mH |
| | 127.7 µF |
| $f_{sw}$ | 1, 4, 6 and 8 kHz |
| $f_{ac}$ | 60 Hz |
| $R_{g\text{-}on}$ & $R_{g\text{-}off}$ | 3.3 Ω |

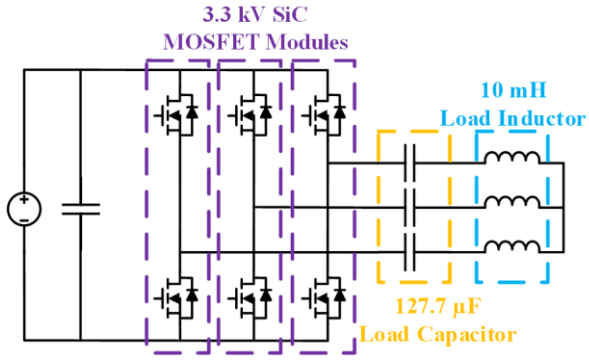


Fig. 9. Schematic of the converter testing setup.

### A. Test Setup

The electrical setup is outlined in the schematic diagram shown in Fig. 9. The inverter power stage and the load are shown in Fig. 10 within a rack assembly utilized to contain the DUT and allow for ease of access and mobility of the setup.

To achieve the desired test load current, a capacitive-inductive load is adopted to yield the required impedance at the test ac frequency, i.e., 60 Hz. Their values are given in Table III

A DSP control board is used to transmit PWM signals. Fiber optic lines and a shield box are used to avoid EMI from affecting the control signals. Waveforms are recorded with a Tektronix MSO58 ooscilloscope.

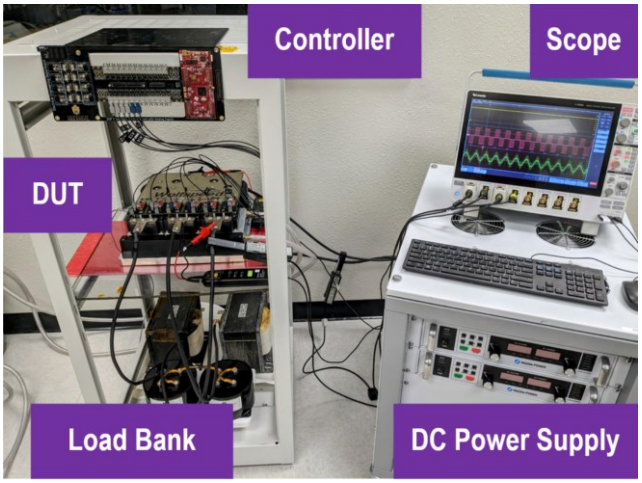


Figure 10. Test rack containing the power converter and the load bank.

### B. Experimental results

The results of the continuous operating test with 1 kHz and 8 kHz switching frequencies are shown in Figs. 11 and 12, respectively. As shown in the results, the current waveforms have much less distortion when the switching frequency of the devices increases. The effect of the switching frequency on the THD of the output current is presented in Fig. 13, where the THD drops sharply with the frequency change from 1 kHz to 4 kHz.

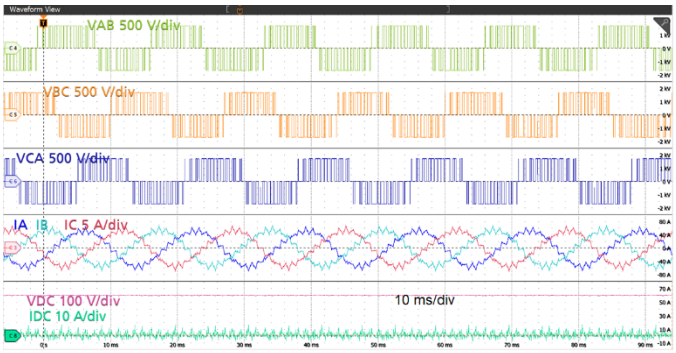


Fig. 11. Test waveforms at 1 kHz switching frequency.

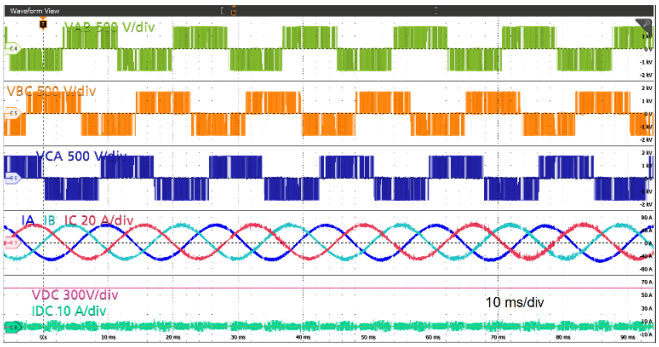


Fig. 12. Test waveforms at 8 kHz switching frequency.

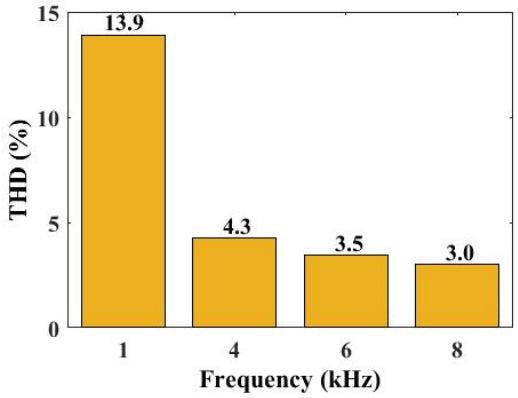


Fig. 13. The measured output current THD vs. switching frequency.

## V. Conclusion

This work presents a high power MV three-phase converter design using the latest 100 mm × 140 mm half-bridge module package. To achieve high power density, 3.3 kV SiC MOSFET power modules are adopted with the utilization of ultra-low inductance busbar and film capacitors. Detailed converter design processes are presented. The operating ability of the power stage is validated by the thermal performance simulation and continuous operating experiment.

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