Low-Loss D-band SIW Power Divider for Integrated Systems

Weifeng Wu[(1)], Xiaopeng Wang[(2)], Lei Li[(2)], James C. M. Hwang[(2)], and Patrick Fay[(1)]

[(1)] University of Notre Dame, Notre Dame, IN 46556, USA
[(2)] Cornell University, Ithaca, NY 14850, USA

***Abstract*—This paper demonstrates a novel approach to the design of D-band power dividers, capitalizing on the benefits of Substrate Integrated Waveguide (SIW) technology in 100-μm thick SiC substrate. By leveraging the unique characteristics of SIW and utilizing silicon carbide as the substrate material, an average insertion loss as low as 0.26 dB, and average return loss of up to 24 dB has been achieved in simulation in D-band. Although D-band dividers employing coplanar waveguides and microstrip lines have been reported, to the best of our acknowledge, this is the first work on D-band SIW power dividers. The SIW technology is compatible with GaN-on-SiC MMIC fabrication process flows, and provides a novel platform for the integration of low-loss millimeter-wave combiners with III-N based electronics.**

I. Introduction

The continuous demand for higher data rates and increased bandwidth in millimeter-wave (mm-Wave) communication systems has led to a growing need for advanced signal distribution components operating in the D-band frequency range (110-170 GHz). Power dividers play a pivotal role in these systems, enabling efficient signal splitting. As shown in Table I, conventional designs employing microstrip and coplanar lines [1]–[6] have been explored in the literature to address this requirement, yet challenges persist in achieving low insertion loss (IL) and wide bandwidth.

This paper proposes a solution by harnessing the potential of Substrate Integrated Waveguide (SIW) technology for D-band power divider design. SIW offers a unique platform that combines the benefits of waveguide structures with the advantages of planar circuit integration, low IL, low crosstalk, and high power capacity. Additionally, employing silicon carbide (SiC) as the substrate material bolsters the performance of the proposed power divider and provides a path to integration with III-N based electronics. SiC's exceptional material properties, including high thermal conductivity, dielectric constant, electrical resistivity, mechanical toughness and low loss tangent, make it particularly well-suited for high-performance mm-Wave power applications.

II. Power Divider Design

SIW-based dividers based on both Y- and T-junction architectures, in combination with SIW bends and transitions to planar waveguides have been designed and evaluated. Initial designs were based on analytical calculation [7], followed by numerical simulation (HFSS) to optimize performance. The D-band SIWs are designed on 100-μm-thick 4H-SiC wafers with $\geq 10^7\ \Omega \cdot cm$ resistivity, employing Au for metalization, with conductivity of 4.1×10^7 Siemens/m. SIW offers very low loss, as shown in Fig. 1, the IL of a straight SIW section is projected to be 0.20 ± 0.06 dB/mm.

TABLE I
Simulation-based power dividers above 110 GHz.

Bandwidth (GHz)	Waveguide	IL (dB)	RL (dB)	Reference
102-140	Microstrip	0.5-0.6	>20	[1]
140-205	Microstrip	<1	>10	[2]
140-220	GCPW	1.4-2.4	NA	[3]
135-165	GCPW	0.8-1.5	>15	[4]
140-180	GCPW	1.2-2.0	>10	[5]
110-130	GCPW	<1.25	>15	[6]
110-170	SIW	0.20-0.65	>10	This Work[a]

[a] Y-junction divider.

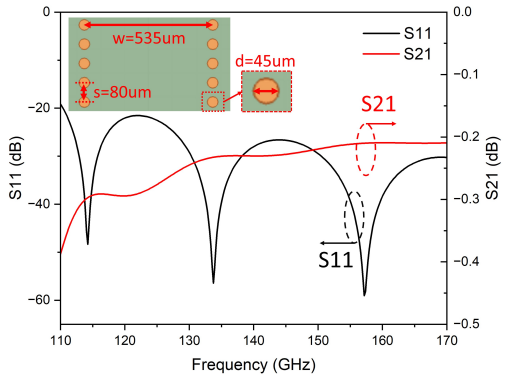


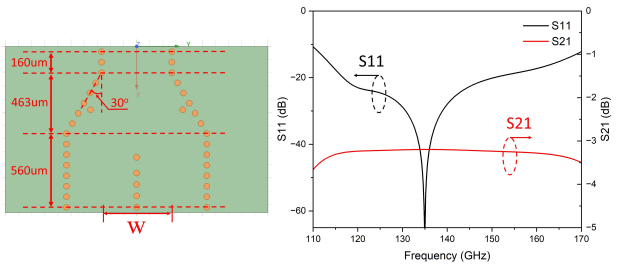
Fig. 1. S-parameter simulation of a straight SIW section. Insert: dimensional details of SiC SIW structure.

A. Y-junction Divider

As shown in Fig. 2 (a), the Y-junction divider consists of a input SIW, 30^o tapered transition and two output SIWs. Based on HFSS simulation, a low average IL of 0.26 dB is achieved with average return loss (RL) $>$ 24 dB over the D-band. Due to the symmetry, we can expect good phase matching between the two output signals.

B. T-junction Divider

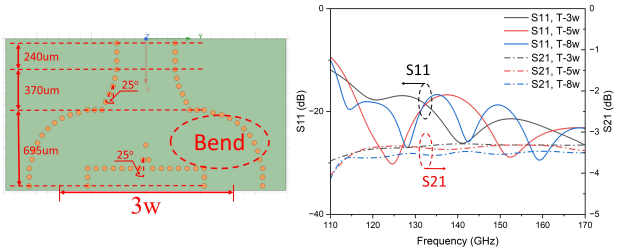
Fig. 3 (a) is the overview of the T-junction with SIW bends which, compared to the Y-junction, gives the flexibility to adjust the output SIW spacing. The T-junction dividers consist of a input SIW, a taper, and two output SIWs with 90^o bends. In Fig. 3 (b), the simulated S-parameters of the T-dividers with different output SIW spacing are compared. As can be seen,



(a) (b)

Fig. 2. (a) Y-junction divider. (b) S-parameter simulation of Y-junction.

the performance depends only weakly on output spacing, with average IL of 0.36-0.53 dB and average RL $>$ 20 dB over the D-band.



(a) (b)

Fig. 3. (a) T-junction divider with output SIW spacing of 3w. (b) S-parameter simulation of T-dividers with different output SIW spacing.

C. Transition Design

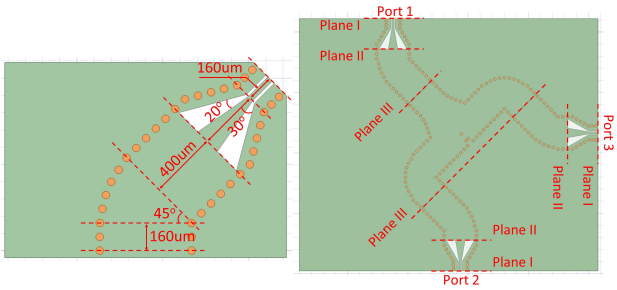
For monolithic integration of the SiC SIW with active electronic devices (e.g. GaN HEMTs), transitions to surface planar interconnections such as grounded coplanar waveguide are needed [8]. Therefore, a launch with the grounded coplanar waveguide transition has been designed. This provides the necessary connection between conventional MMIC interconnects and the SIW as well as facilitates the on-wafer measurements of the SIW elements as shown in Fig. 4 (a). A 45^o bend is introduced due to the configuration of on-wafer probe stations with orthogonal measurement ports. In addition to the dividers, Thru-Reflect-Line calibration and de-embedding standards have been designed to place reference planes at the reference planes I, II and III as shown in Fig. 4 (b).

III. Fabrication Progress

Fig. 5 shows a 4-inch SiC wafer in process, alongside micrographs of a single die on wafer. The process flow consists of top side metalization, through substrate via etching by ICP-RIE, and via and backside metalization by plating [8].

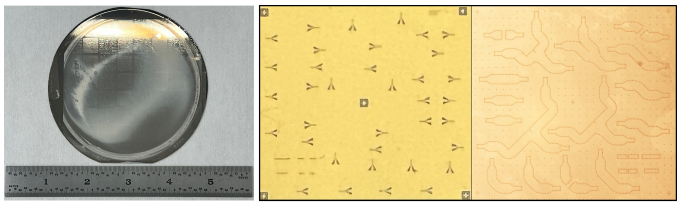
IV. Conclusion

In this work, we demonstrate a novel approach to the design of D-band power dividers, capitalizing on the benefits of SIW technology. An significant average IL as low as 0.26 dB, and average RL of up to 24 dB has been achieved in simulation in D-band, which provides a novel platform for integration of low-loss mm-Wave combiners with III-V based electronics.



(a) (b)

Fig. 4. (a) Launch design. (b) Example DUT: T-junction Divider with launches.



(a) (b)

Fig. 5. (a) A 4-inch SiC wafer in process. (b) Optical micrographs showing both sides of the die on wafer, showing Y- and T-dividers and calibration structures.

ACKNOWLEDGEMENT

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