Toward Wireless System and Circuit Co-Design for the Internet of Self-Adaptive Things

Diptashree Das, Mohammad Abdi, Minghan Liu, Marvin Onabajo and Francesco Restuccia
Department of Electrical and Computer Engineering, Northeastern University, United States

***Abstract*—The deployment of a growing number of devices in Internet of Things (IoT) networks implies that uninterrupted and seamless adaptation of wireless communication parameters (e.g., carrier frequency, bandwidth and modulation) will become essential. To utilize wireless devices capable of switching several communication parameters requires real-time self-optimizations at the radio frequency integrated circuit (RFIC) level based on system level performance metrics during the processing of complex modulated signals. This article introduces a novel design verification approach for reconfigurable RFICs based on end-to-end wireless system-level performance metrics while operating in a dynamically changing communication environment. In contrast to prior work, this framework includes two modules that simulate a wireless channel and decode waveforms. These are connected to circuit-level modules that capture device- and circuit-level non-idealities of RFICs for design validation and optimization, such as transistor noises, intermodulation/harmonic distortions, and memory effects from parasitic capacitances. We demonstrate this framework with a receiver (RX) consisting of a reconfigurable complementary metal-oxide semiconductor (CMOS) low-noise amplifier (LNA) designed at the transistor level, a behavioral model of a mixer, and an ideal filter model. The seamless integration between system-level wireless models with circuit-level and behavioral models (such as VerilogA-based models) for RFIC blocks enables to preemptively evaluate circuit and system designs, and to optimize for different communication scenarios with adaptive circuits having extensive tuning ranges. An exemplary case study is presented, in which simulation results reveal that the LNA power consumption can be reduced up to 16x depending on system-level requirements.**

***Index Terms*—System-level validation, adaptive wireless systems and circuits, hardware/software co-design, energy-aware optimization, simulation-based system testing.**

I. Introduction

By 2030, over 50 billion devices will be absorbed into the Internet of Things (IoT) [1]. The sheer number of IoT devices implies that continuous and seamless adaptation of wireless communication parameters (e.g., carrier frequency, bandwidth and modulation) will become essential. One of the wireless system design goals is to provide sensing services for a plethora of applications. However, the implementations are constrained because sensing and communication circuit parameters have to be optimized for different frequency bands, modulation schemes and channel conditions [2]. For this reason, *reconfigurability* and *self-optimization* will be a cornerstone of IoT networking paradigms [3]–[5]. Furthermore, it becomes increasingly important to jointly simulate circuit and system level components for design optimization and validation prior to the fabrication of chips. On the other hand, conventional radio frequency integrated circuits (RFICs) are still statically optimized, which does not allow for real-time self-optimization at the intersection of hardware and software. Low-power RFICs are typically designed and optimized specifically for the worst-case scenario of a given communication standard, which leads to performance limitations and excessive power consumption. Furthermore, circuit-level tuning usually optimizes block-level performance. Conversely, in real systems, the circuit-level linearity and dynamic range requirements strongly depend on the presence of nearby interference signals and bias conditions [6]–[10], while slow-varying aspects such as temperature sensitivity or device-level aging effects can only be computed and compensated throughout the device lifetime [11]. Digitally-controlled calibration is a popular design approach to improve the performance and testability of mixed-signal integrated circuits [12], [13]. However, RFIC calibrations of multiple interconnected circuit blocks typically do not address the interdependence of the circuit-specific parameters during tuning, which creates limitations during simulations for design validations. They normally also do not account for system-level parameters such as symbol error rate (SER) or throughput, particularly when relying on single-tone/two-tone signals or other alternative test signals instead of the actual modulated signals [14]. A comprehensive survey about the integration of machine learning (ML) into integrated circuit design has been provided in [15], [16]. The use of ML during design and optimization can be another potential method to ensure functionality under consideration of interdependence between circuit and system parameters.

Considering the above-mentioned challenges and opportunities, we propose a new RFIC co-design and validation paradigm at the intersection of hardware and software, which is summarized in Fig. 1. Our joint simulation framework considers *system-level performance metrics* to facilitate the design of adaptive RFIC circuits. The developed interoperability between different design tools allows to (i) generate arbitrary modulated waveforms while modeling different wireless channel conditions, (ii) utilize foundry-supplied models that capture transistor-level non-idealities, (iii) simulate both behavioral analog RFIC blocks and circuit level designs, and (iv) extract circuit-level and system-level performance metrics. Furthermore, we introduce simulations with modulated signal packets and modeled channel impairments to extract system-level parameters such as bit error rate (BER) and error vector magnitude (EVM); and accordingly optimize several circuit conditions (e.g., gain, noise figure and linearity characteristics) for optimization of energy/performance tradeoffs. As a use-case scenario, we leverage our framework to optimize a receiver (RX) composed of a reconfigurable complemen-

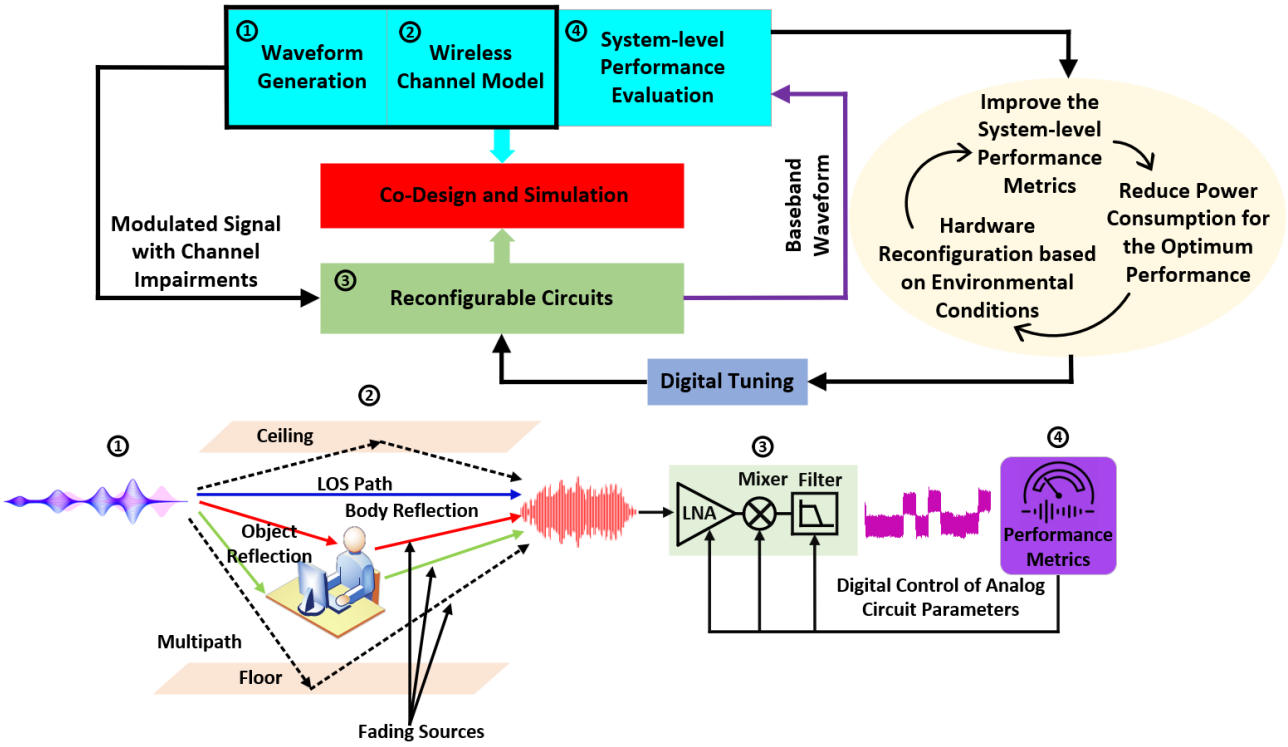

Fig. 1. Overview of the framework for co-design and optimization of reconfigurable RF circuits and wireless communication systems.

tary metal-oxide semiconductor (CMOS) low-noise amplifier (LNA) designed at the transistor-level, a behavioral model of a mixer and an ideal filter model. The simulation results show that our framework can reduce the LNA power consumption by up to 16x under varying BER requirements. In general, the simulation framework can be used as a tool during the design and validation of adaptive wireless RXs that operate with dynamically changing requirements.

II. Existing Work and Current Challenges

The fast-changing IoT ecosystem leads to a very dynamic nature of the wireless channel that calls for complex hardware and software systems, including adaptive and tunable transceiver designs. It has been explained in [17] how tunable and reconfigurable radio frequency (RF) technologies provide potential solutions for efficient spectrum sharing. In [18], a simulation-based approach develops a multi-user IoT communication system by taking into account carrier synchronization and data broadcasts on multiple channels for several of low-power devices present in the network. The work in [19] realized a learning-based RF signal classifier on a field-programmable gate array (FPGA) to reduce latency and power consumption, which requires prior knowledge of signals and spectrum.

Adaptability in the RX front-end opens up the opportunity to collect and process data from a dynamic wireless channel. CMOS RFIC prototypes have been designed to enhance linearity and power handling requirements for cellular applications [20]. However, RFICs can still be complemented with real-time adaptation algorithms to optimize transceiver operation. [21] introduces a real-time two-dimensional real-time adaptation method to configure a RX for optimum NF and linearity with a certain power budget and desired signal level. The design of adaptive wireless RXs with single or multi-parameter optimization is highly relevant for specific incoming signals, and requires validating performance for different wireless standards, channel conditions, and chip-level performance variations (e.g., CMOS fabrication process variations). A key consideration during the design of adaptive RFICs is that reconfigurability is tightly coupled with power consumption. In addition, the need for wide tuning range and energy/power scalable designs calls for the seamless combination of circuit and system level adjustments. An evaluation of performance versus power trajectory for RF front-end functional blocks has been explored in [22]. In addition to determining the inter-dependencies of circuit parameters for each block in the RF front-end, the optimization of analog RF circuits based on feedback control with digitally-controlled features has been demonstrated [13], [23]–[27], which requires to design complex control strategies for different conditions in the presence of channel and device level variations.

The problem of energy efficiency and channel conditions is conventionally controlled by adaptive modulation and coding [28], making it harder for the RF front-end to adapt to any changes in the channel. Integrating tunable RFICs into spectrum-agile wireless networks can allow to self-optimize RF circuit parameters to produce a desired output signal within the optimum power budget based on existing channel conditions. [29] describes a channel-adaptive RX design with pro-

cess variation tolerance. Furthermore, a neural network based self-learning RF system has been demonstrated in [30], which is able to reduce power consumption of wireless transceiver systems by dynamically tuning the circuit components while monitoring the effects of real-time wireless channel conditions and the fabrication process variations to produce a desired BER and threshold EVM. This is achieved with an on-chip look-up table that requires to be updated based on expected channel conditions.

The difficulty of simulating the entire system is a major impediment to verify the merits of the integrated hardware-software based wireless system. This work aims to design and validate a joint simulation platform that can address the inter-dependencies of circuit parameters in the RF front-end to develop self-optimized wide-range reconfigurable RX architecture together with wireless network that is capable of changing communication parameters. Furthermore, this approach to incorporate and verify system-level performance-driven tuning features using reconfigurable RFIC blocks is especially compelling to enhance resilience to sudden changes in the environment and accordingly optimize to achieve performance targets with optimum power consumption. Hence, the presented simulation framework is expected to ease the adaptive design and optimization of closed-loop self-supervised Internet of Self-adaptive Things with different modulated signals, wireless channel models and adaptive RFIC designs together with circuit level non-idealities.

III. Optimization Framework Overview

We consider a scenario as depicted in Fig. 1, where we model multipath effects and dynamic fading along with arbitrary modulated signal packets during the design of robust RFIC adaptability to receive and process information. Here, the waveform generation allows to change the modeled Physical-layer (PHY) parameters (such as modulation scheme, power carried by the spectrum components, RF sampling frequency, channel coding and bandwidth). Currently, only the Signal-to-Noise-Ratio (SNR) is used as a primary indicator of variable channel conditions. The variable SNR-based model encompasses several channel impairments such as additive white Gaussian noise (AWGN), multi-path fading, variable distance between transmitter (TX) and RX, and path-loss among other interference as indicated in Fig. 1. The sensitivity requirement of the RF front-end strongly depends on the SNR. [31] includes a description of typical SNR values for channels, where the comparative results with different modulation schemes provide insights into the expected SNR values for various channel conditions. It is also envisioned that future spectrum-agile TXs will lead to more variations of interference levels, SNR values, and modulation schemes.

As depicted in Fig. 1, the baseband waveform is processed to infer parameters associated with system-level performance such as BER, SER, EVM, modulation error ratio (MER) and packet error rate (PER). This approach is based on the goal to develop algorithms for accurate data-driven optimization of RFICs based on system performance. Next, we present an architecture with a reconfigurable RF front-end circuit that is evaluated through the simulation framework from this work.

IV. Design and Modeling of RF Front-end Circuits with Dynamic Reconfigurability

A. Flexible RF Front-end Architecture

Analog RF front-end reconfigurability enhances co-existence and spectrum sharing in crowded environments [32], as well as allows to vary parameters such as data rates on demand [33]. As shown in Fig. 2, the reconfigurable RF RX front-end in this work consists of a digitally programmable LNA circuit designed at the transistor-level with tunable bias current, a behavioral model of a direct down-conversion in-phase/quadrature (I/Q) mixer stage, and two ideal low-pass filter (LPF) models in the I and Q paths. Circuit-level simulations with device-level non-idealities can capture impacts of frequency response limitations, inter-modulation products, thermal and flicker noises, parasitic capacitances/resistances, and higher-order non-linearities of the transistors, that allows block-level specifications assessment such as gain, noise figure (NF), input third-order inter-modulation intercept point (IIP3) and impedance matching conditions. At the same time, the ability to include some behavioral models of circuit blocks aids the early design and system-level verification phase. Most importantly, the accurate transient simulations allow to account for the impacts of circuit-level imperfections to assess system-level metrics with changing environment.

To overcome existing inflexible wireless standards, inefficient spectrum use and potential security threats in the wireless network, the flexible adaptation of PHY parameters of the signal proves an effective and long-standing solution. The work in [34] demonstrated if TXs were allowed to dynamically switch PHY parameters such as carrier frequency and symbol modulation, the TXs would become less jamming-prone and achieve more efficient spectrum occupation. To give an example, Fig. 2 shows the selected test signal with a format that corresponds to the Zigbee PHY packet structure. This signal with any modeled channel impairments has been applied as input signal during circuit and behavioral simulations of the RF front-end. The frame starts with a known preamble for synchronization, which exhibits high auto-correlation and low cross-correlation features. The preamble is followed by a start-of-frame delimiter that marks the beginning of the header. The header consists of the frame length in bytes and the modulation code associated with the modulation scheme used. A data checksum (CSC) is attached to the header and data parts respectively, such that erroneous frames can be detected and discarded. The data part of the frame can support a MAC Protocol Data Unit (MPDU) with a size of up to $2^8 - 1$ bytes.

As depicted in Fig. 2, the emulated transmitted packets with added channel noise and imperfections are transferred to the signal source of a circuit simulator (Cadence Spectre) for the RF front-end simulation. The model-based design simulator (Matlab) is capable of saving the raw data in the comma-separated values (CVS) file format, which has been incorporated into the circuit simulator by the virtue of a piece-wise

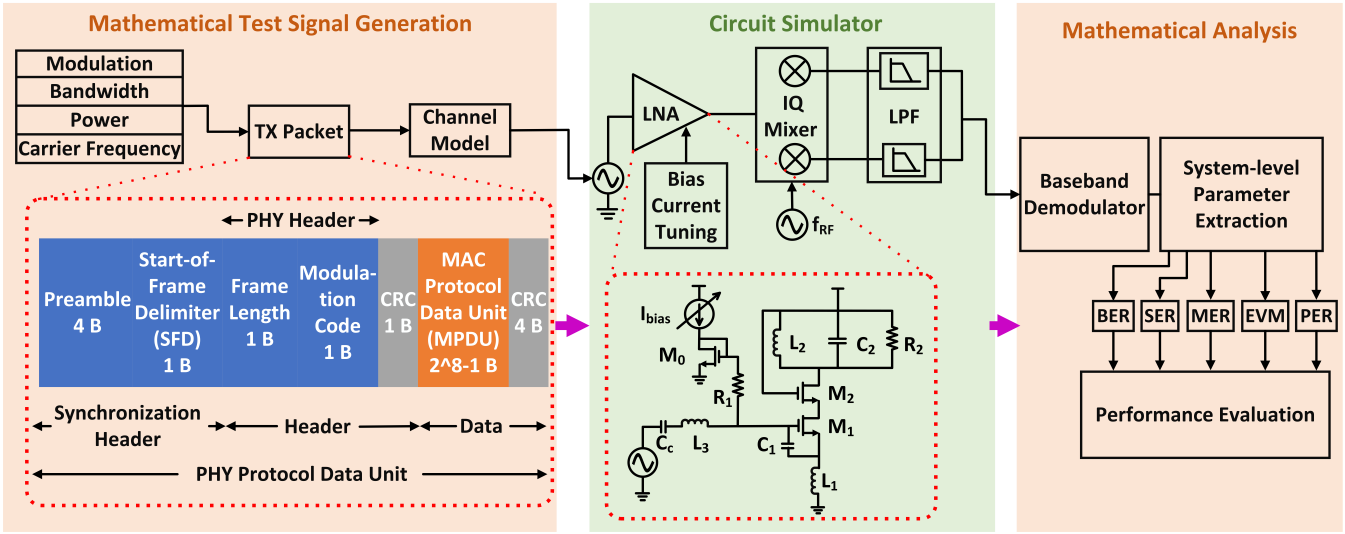

Fig. 2. Co-design simulation platform for wireless systems with dynamically reconfigurable RF front-end circuits.

linear signal source. Thus, the reconfigurability settings and biasing conditions of the RF front-end blocks can be evaluated during the circuit design phase to optimize characteristics such as noise levels, linearity, RX sensitivity and impedance matching conditions. As mentioned earlier, the mathematical analysis of the circuit simulator output provides system-level performance metrics (such as BER, SER, MER, and EVM) for both circuit and system-level optimization with modulated signals. Here, the BER is considered as one of the most significant PHY performance indicators. Since not all inaccuracies lead to bit flips, EVM is another appropriate measure to quantify the quality of the received signal after processing in the RF front-end, which allows to capture important channel and RX non-idealities [35], [36]. Various imperfections such as changing channel conditions have impacts on the EVM since they can cause the received constellation points to deviate from their original ideal locations.

B. Reconfigurable LNA

A 2.4 GHz single-ended cascode common-source LNA with inductive source degeneration has been selected as an exemplary reconfigurable narrowband LNA design, of which the bias current is tuned to control performance/power tradeoffs as shown in Fig. 2. Since the LNA is the first block of the RF front-end, its performance is particularly crucial when receiving noisy packets at low power levels. The standalone LNA was designed in a standard 65nm CMOS technology, and simulated for bias currents ranging from 31.25 μA to 500 μA. By changing the bias current +/-20% to +/-50% from its design point (125 μA), the circuit characteristics such as gain, IIP3, and NF can be adjusted with a corresponding change of the power consumption that is directly proportional to the bias current. Fig. 3 summarizes the gain, NF and IIP3 of the LNA from transistor-level simulations.

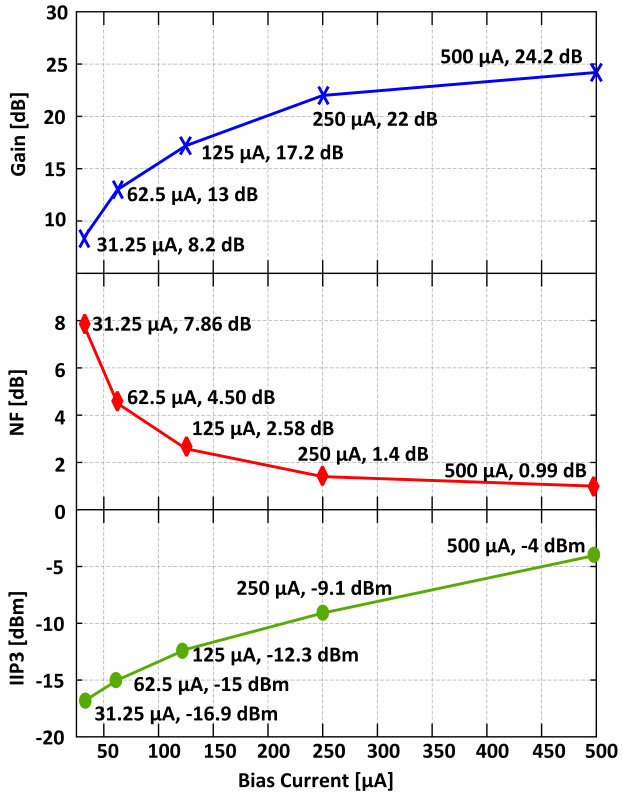

Fig. 3. Simulated LNA performance parameters vs. bias current.

C. Mixer and Baseband Signal Processing

To portray the capability of combining transistor-level schematic simulations (i.e., the LNA) with behavioral blocks during transient circuit simulations to assess system-level metrics under specified/changeable wireless channel conditions, a direct down-conversion I/Q mixer has been modeled in VerilogA, followed by two ideal LPFs (one in each RX path). The mixer model includes variable gain, IIP3 and NF based on

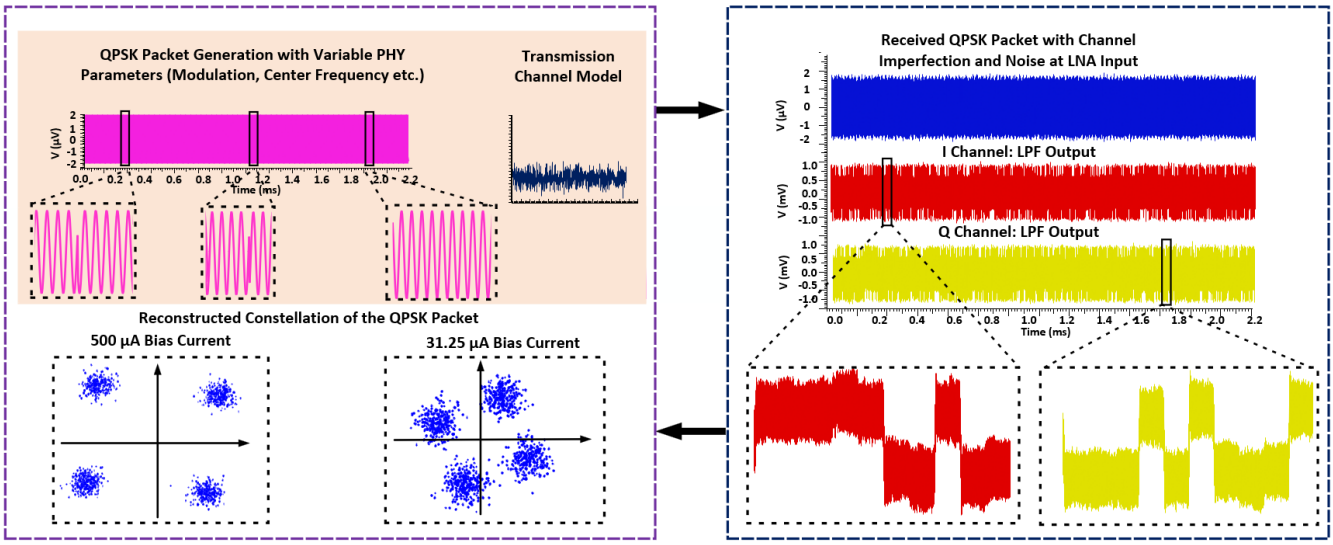

Fig. 4. Results from the simulation with generated QPSK packets: transient RF front-end characteristics and reconstructed constellations.

TABLE I
SYSTEM-LEVEL PERFORMANCE SUMMARY FOR THE RE-CONFIGURABLE RF FRONT-END WITH LNA BIAS TUNING FROM SIMULATIONS WITH A QPSK BURST (4272 BITS) HAVING A POWER OF -100 DBM.

Bias Current (µA)	BER	SER	EVM (%)
500	0.24×10^{-5}	0.31×10^{-5}	15.07
250	0.36×10^{-5}	0.40×10^{-5}	19.56
125	0.59×10^{-5}	0.62×10^{-5}	21.04
62.5	3.39×10^{-4}	3.66×10^{-4}	32.11
31.25	1.9×10^{-3}	2.01×10^{-3}	44.56

typical reconfigurable circuit parameters of down-conversion mixers. In this proof-of-concept, the performance assessment of the RF front-end was with QPSK-modulated signals and channel impairments according to the signal generation in Fig. 2.

The channel model accounts for AWGN, path-loss and generic frequency-selective multi-path fading that can introduce different path attenuation, delay, and Doppler shift. The baseband demodulator after the LPF is also implemented mathematically, where according to the decision boundaries defined by the associated constellation, the I/Q samples are detected and compared against the ground-truth I/Q samples to compute the desired system-level parameters. Future work will be devoted to automatic parameter tuning parameters in the RF front-end circuits based on the extracted system-level performance metrics to optimize with varying spectrum conditions under specified power consumption targets.

V. CASE STUDY: RECONFIGURABLE RF FRONT-END SIMULATION

This section summarizes results from the use of our co-simulation framework for the example RF front-end configuration described in the previous section. The simulations were primarily carried out to evaluate the performance vs. power trade-offs associated with the reconfigurable LNA design. As mentioned in the previous section, the complete testbench used for the simulations includes a VerilogA based mixer and ideal LPF. The mixer has been modeled with flexible circuit parameters in which the gain, IIP3 and NF can be changed as part of the design exploration. In this work, we have used an ideal behavioral mixer model with a gain of 10 dB, IIP3 of 5 dBm and NF of 10dB for the proof-of-concept simulations [37]–[39]. The upper left image in Fig. 4 displays the generated QPSK-modulated signal with the packet structure defined in Fig. 2. A binary ground-truth message is randomly generated and up-converted to produce the QPSK modulation with a center frequency of 2.4 GHz. The SNR of the received signal was selected as 20 dB to emulate typical wireless network conditions with channel impairments and distortion [40], [41]. The corresponding waveform of the generated QPSK signal in Fig. 4 is corrupted by the channel imperfections and noise, and fed to the RF front-end. The simulated I/Q signals at the LPF outputs are shown on the right side of Fig. 4. These I/Q signals are transferred for mathematical baseband processing using an envelope detector and moving average filter (as displayed in Fig. 2) during model-based simulations.

The demodulated I/Q samples are then compared and ver-

ified with the ground-truth data to extract BER, SER, EVM and MER. The lower values of the BER and SER relust from high accuracy of demodulation process. In this case, the BER and SER are in the range of 10^{-5}-10^{-3} for all LNA bias current conditions. On the other hand, the MER values are 18.9 dB and 11.2 dB for LNA bias currents of 500 μA and 31.25 μA respectively. The proximity of the MER value to the specified channel SNR (20 dB) is an indication of a noise resilient system, which results from the LNA bias with high current (i.e., high power consumption) to achieve a low NF. Fig. 4 includes the extracted constellations of the QPSK signal after the processing by the RF front-end with the highest and lowest LNA bias currents, which also show the power vs. performance tradeoff. Table I includes an overview of the system-level performance for different LNA bias current settings. We have simulated two QPSK packets (4272 bits) with randomly generated ground-truth data to evaluate the high-level system performance with the co-design platform. It can be seen from Table I that the BER, SER and EVM are considerably lower for LNA bias currents in the 125 μA to 500 μA range. In addition, no packet errors (PEs) occurred in the 125 μA to 500 μA bias current range. The simulation results show robust adaptability, which will be realized with an application-specific feedback control loop as depicted in Fig. 1. Depending on the application-specific BER requirement and channel conditions, energy consumption can be significantly reduced through the 62.5 μA and 31.25 μA bias current settings.

VI. Next Steps: Beyond Traditional Wireless System and RFIC Integration

We foresee that the research presented in this paper will be the foundation for the development of reconfigurable RXs with real-time self-optimization capabilities. The work described in this article is the first step associated with the co-design and verification of wireless systems and circuits that can tolerate and adapt to interference conditions using novel RFIC optimization methods with unprecedented design flexibility based on specified system-level performance metrics. As depicted in Fig. 5, we anticipate that the presented co-simulation and design verification framework will contribute to the development of several novel features: (i) ML-based self-decisive CMOS RF front-ends to adapt changing network conditions, (ii) development of hardware-software prototypes based on joint integrated circuit simulations and wireless data collection for enhanced modeling, (iii) several digitally-controlled tuning knobs in each analog block as indicated in Fig. 1, and (iv) collection of waveform datasets through the experimental testbenches to train ML algorithms. (v) Once the ML algorithms are developed, the deep reinforcement learning (DRL) agent will be trained to collect data, both experimentally and synthetically utilizing the proposed framework. During the data collection, one can deploy the optimal policy on FPGA-based platforms such as software-defined radios (SDRs) [42], [43] to meet the challenging time constraints involved, and to reduce the overall power consumption. The presented simulation framework features tools to jointly optimize the power-efficiency of digitally-controlled analog circuits and the computation resources to implement adaptive ML-based control. Once the envisioned ML algorithm is developed and the DRL agent is trained experimentally and synthetically collected data using the proposed framework, one could deploy the optimal policy on FPGA-based platforms such as SDRs [42] so as to meet the challenging time constraints involved. To further minimize the power consumption introduced by running the ML method, one can change the operational frequency or even limit it to the times when the system-level performance drops below a certain threshold or experiences a sudden change. The simulation results in Section V show that the RF front-end in this case study has a sensitivity of -100 dBm. We have presented a case study with a QPSK packet, but other modulation schemes (e.g. ASK, BPSK) with different SNR values, data rate, bandwidth, center frequencies can be employed. The reconfigurable RX design and simulation approach is intended to facilitate the use of flexible wireless system parameters by reconfiguring circuit parameters for the optimum performance and spectrum sharing in real-time.

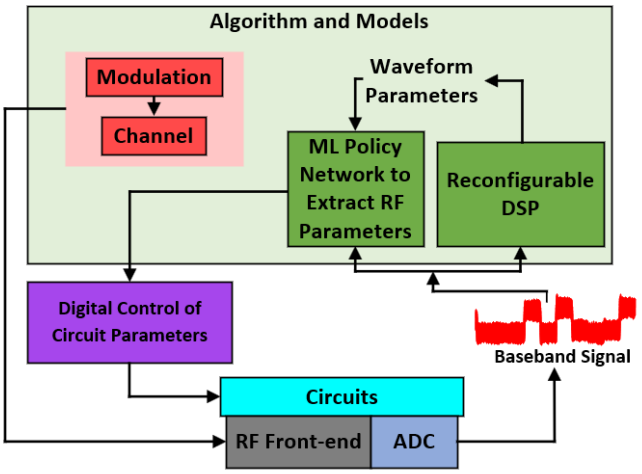

Fig. 5. Envisioned ML-based real-time RF front-end optimization.

VII. Conclusion

This article presented a new co-design simulation platform to evaluate trade-offs between performance and power consumption by integrating the design and modeling of wireless systems and reconfigurable RF front-end circuits together. A main contribution of the integrated framework is to provide an effective and long-lasting tool for the design of spectrum-agile RXs with adaptive RFICs for dynamic optimizations under changing environmental conditions. The execution of the joint summation taking into account combining dynamic wireless channel model and reconfigurable RF front-end with circuit level non-idealities accounts for incorporation of several modeling and design software to validate the performance. The reconfigurability of the RF front-end aims to reduce power consumption significantly based on application-specific

system-level performance targets. However, the primary goal is to execute the seamless adaptation of the RF front-end by optimizing its circuit parameters during real-time execution with spectrum-agile transmission to produce desired end-to-end system level performance. The integration of digital tuning capabilities in each of the analog blocks within RFICs will be particularly useful for realizing future wireless system paradigms with an unprecedented degree-of-freedom.

VIII. Acknowledgement

This material is in part based upon work supported by the NSF under grant no. ECCS-2146754, CCF-2218845, CNS-2134973, CNS-2120447, ECCS-2229472, and is supported in part by funds from OUSD R&E, NIST, and industry partners as specified in the Resilient & Intelligent NextG Systems (RINGS) program, as well as by the Air Force Office of Scientific Research under contract number FA9550-23-1-0261, and by the Office of Naval Research under award number N00014-23-1-2221. The U.S. Government is authorized to reproduce and distribute reprints for Governmental purposes notwithstanding any copyright notation thereon. The views and conclusions contained herein are those of the authors and should not be interpreted as necessarily representing the official policies or endorsements of the NSF and the U.S. Government.

References

[1] Federal Communications Commission (FCC), "Spectrum Crunch," https://www.fcc.gov/general/spectrum-crunch.

[2] A. Liu, Z. Huang, M. Li, Y. Wan, W. Li, T. Xiao-Han, C. Liu, R. Du, D. Kai Pin Tan, J. Lu, Y. Shen, F. Colone, and K. Chetty, "A survey on fundamental limits of integrated sensing and communication," *IEEE Communication Surveys and Tutorials*, vol. 24, no. 2, pp. 994 – 1034, 2022.

[3] M. D. V. Pena, J. J. Rodriguez-Andina, and M. Manic, "The internet of things: The role of reconfigurable platforms," *IEEE Industrial Electronics Magazine*, vol. 11, no. 3, pp. 6–19, 2017.

[4] M. Chen, A. Liu, W. Liu, K. Ota, M. Dong, and N. N. Xiong, "RDRL: A Recurrent Deep Reinforcement Learning Scheme for Dynamic Spectrum Access in Reconfigurable Wireless Networks," *IEEE Transactions on Network Science and Engineering*, vol. 9, no. 2, pp. 364 – 376, 2022.

[5] J. Tallon, T. K. Forde, and L. Doyle, "Dynamic Spectrum Access Networks: Independent Coalition Formation," *IEEE Vehicular Technology Magazine*, vol. 7, no. 2, pp. 69 – 76, 2012.

[6] M. Abdulaziz, E. A. M. Klumperink, B. Nauta, and H. Sjöland, "Improving receiver close-in blocker tolerance by baseband $G_m - C$ notch filtering," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 66, no. 3, pp. 885–896, 2019.

[7] D. Murphy, H. Darabi, A. Abidi, A. A. Hafez, A. Mirzaei, M. Mikhemar, and M.-C. F. Chang, "A blocker-tolerant, noise-cancelling receiver suitable for wideband wireless applications," *IEEE Journal of Solid-State Circuits*, vol. 47, no. 12, pp. 2943 – 2963, 2012.

[8] C. Andrews and A. C. Molnar, "A passive mixer-first receiver with digitally controlled and widely tunable rf interface," *IEEE Journal of Solid-State Circuits*, vol. 45, no. 12, pp. 2696 – 2708, 2010.

[9] N. Kim, L. E. Larson, and V. Aparin, "A highly linear saw-less cmos receiver using a mixer with embedded tx filtering for cdma," *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, 2008.

[10] Z. Ru, N. A. Moseley, E. A. M. Klumperink, and B. Nauta, "Digitally enhanced software-defined radio receiver robust to out-of-band interference," *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, vol. 44, no. 12, pp. 3359–3375, 2009.

[11] S. Arasu, M. Nourani, J. Carulli, and V. Reddy, "Controlling Aging in Timing-Critical Paths," *IEEE Design & Test*, vol. 33, no. 4, pp. 82–91, 2015.

[12] H. Chauhan, M. Onabajo, V. Kvartenko, R. Coxe, and T. Weber, "An optimization platform for digital predistortion of power amplifiers," *IEEE Design & Test*, vol. 33, no. 2, pp. 49–58, 2016.

[13] M. Onabajo and J. Silva-Martinez, "Analog Circuit Design for Process Variation-Resilient Systems-on-a-Chip," *Springer*, 2012.

[14] B. Georgescu, R. Salmeh, M. Fattouche, and F. Ghannouchi, "Two-tone phase delay control of center frequency and bandwidth in low-noise-amplifier RF front ends," *IEEE Transactions on Circuits and Systems II: Express Briefs*, vol. 60, no. 4, pp. 192–196, 2013.

[15] T. Chen, G. Zhang, B. Yu, B. Li, and U. Schlichtmann, "Machine Learning in Advanced IC Design: A Methodological Survey," *IEEE Design & Test*, vol. 40, no. 1, pp. 17–33, 2023.

[16] M. Rapp, H. Amrouch, Y. Lin, B. Yu, D. Z. Pan, W. Marilyn, and J. Henkel, "Mlcad: A survey of research in machine learning for cad keynote paper," *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, vol. 41, no. 10, pp. 3162 – 3181, 2022.

[17] L. Laughlin, F. Boccardi, G. Chris, E. Arabi, K. C. Balram, K. A. Morris, and M. A. Beach, "Emerging hardware enablers for more efficient use of the spectrum," *2019 IEEE International Symposium on Dynamic Spectrum Access Networks (DySPAN)*, 2019.

[18] L. Rodrigues, M. Figueiredo, L. Nero Alves, and Z. Ghassemlooy, "Carrier synchronisation in multiband carrierless amplitude and phase modulation for visible light communication-based iot systems," *IET Optoelectronics*, 2023.

[19] S. Soltani, Y. E. Sagduyu, R. Hasan, K. Davaslioglu, H. Deng, and T. Erpek, "Real-time experimentation of deep learning-based rf signal classifier on fpga," *2019 IEEE International Symposium on Dynamic Spectrum Access Networks (DySPAN)*, 2023.

[20] B.-V. Liempd, B. Hershberg, S. Ariumi, K. Raczkowski, K.-F. Bink, U. Karthaus, E. Martens, P. Wambacq, and J. Craninckx, "A +70-dbm iip3 electrical-balance duplexer for highly integrated tunable front-ends," *IEEE Transaction on Microwave Theory and Techniques*, vol. 64, no. 12, 2016.

[21] M. Meghdadi and M. S. Bakhtiar, "Two-dimensional multi-parameter adaptation of noise, linearity, and power consumption in wireless receivers," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 61, no. 8, 2014.

[22] G. Chang, S. Maity, B. Chatterjee, and S. Sen, "A medradio receiver front-end with wide energy-quality scalability through circuit and architecture-level reconfigurations," *IEEE Journal on Emerging and Selected Topics in Circuits and Systems*, vol. 8, no. 3, 2018.

[23] S. Devarakond, S. Sen, A. Banerjee, and A. Chatterjee, "Digitally assisted built-in tuning using hamming distance proportional signatures in rf circuits," *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, vol. 24, no. 9, p. 2918–2931, 2016.

[24] Y. Feng, G. Takemura, S. Kawaguchi, N. Itoh, and P. R. Kinget, "Digitally assisted iip2 calibration for cmos direct-conversion receivers," *IEEE Journal of Solid-state Circuits*, vol. 46, no. 10, p. 2253–2267, 2011.

[25] B. Murmann, "Digitally assisted analog circuits," *IEEE Micro*, vol. 26, no. 2, pp. 38–47, 2006.

[26] S. Li, J. Li, X. Gu, H. Wang, C. Li, J. Wu, and M. Tang, "Reconfigurable all-band rf cmos transceiver for gps/glonass/galileo/beidou with digitally assisted calibration," *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, vol. 23, no. 9, pp. 1814 – 1827, 2014.

[27] G. Banerjee, M. Behera, M. A. Zeidan, R. Chen, and K. Barnett, "Analog/rf built-in-self-test subsystem for a mobile broadcast video receiver in 65-nm cmos," *IEEE Journal of Solid-State Circuits*, vol. 46, no. 9, pp. 1998 – 2008, 2011.

[28] A. Goldsmith, "Adaptive modulation and coding for fading channels," *Proceedings of the 1999 IEEE Information Theory and Communications Workshop*, p. 24–26, 1999.

[29] S. Sen, V. Natarajan, S. Devarakond, and A. Chatterjee, "Process-variation tolerant channel-adaptive virtually zero-margin low-power wireless receiver systems," *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, vol. 33, no. 12, pp. 1764 – 1777, 2014.

[30] D. Banerjee, B. Muldrey, , X. Wang, S. Sen, and A. Chatterjee, "Self-learning rf receiver systems: Process aware real-time adaptation to channel conditions for low power operation," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 64, no. 1, pp. 195 – 207, 2017.

[31] Y. Shi, K. Davaslioglu, Y. E. Sagduyu, W. C. Headley, M. Fowler, and G. Green, "Deep learning for RF signal classification in unknown

and dynamic spectrum environments," in *2019 IEEE International Symposium on Dynamic Spectrum Access Networks (DySPAN)*, 2019, pp. 1–10.

[32] M. Mohamed, S. Handagala, J. Xu, M. Leeser, and M. Onabajo, "Strategies and demonstration to support multiple wireless protocols with a single rf front-end," *IEEE Wireless Communications*, vol. 27, no. 3, pp. 88–95, 2020.

[33] M. Ibrahim, Mahmoud A. A.and Onabajo, "A 0.061 nj/b 10 mbps hybrid bf-psk receiver for internet of things applications," *IEEE Wireless Communications*, vol. 69, no. 5, pp. 1919 – 1931, 2022.

[34] T. Vo-Huu, T. Vo-Huu, and G. Noubir, "Fingerprinting Wi-Fi Devices Using Software Defined Radios," *in Proc. 9th ACM Conference on Security & Privacy in Wireless and Mobile Networks*, pp. 3–14, 2016.

[35] E. Acar and S. Ozev, "Low-cost characterization and calibration of rf integrated circuits through i–q data analysis," *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, vol. 28, no. 7, pp. 993 – 1005, 2009.

[36] V. Natarajan, H. W. Choi, A. Banerjee, S. Sen, A. Chatterjee, G. Srinivasan, F. Taenzler, and S. Bhattacharya, "Low cost evm testing of wireless rf soc front-ends using multitones," *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, vol. 31, no. 7, pp. 1088 – 1101, 2012.

[37] M. H. Kashani, M. Asghari, M. Yavari, and S. Mirabbasi, "A +7.6 dbm iip3 2.4-ghz double-balanced mixer with 10.5 db nf in 65-nm cmos," *IEEE Transactions on Circuits and Systems II: Express Briefs*, vol. 68, no. 10, pp. 3214 – 3218, 2021.

[38] M. Lehne, J. Stonick, and U. Moon, "An adaptive offset cancellation mixer for direct conversion receivers in 2.4 ghz cmos," *2000 IEEE International Symposium on Circuits and Systems (ISCAS)*, 2000.

[39] H. Li and C. E. Saavedra, "Linearization of active downconversion mixers at the if using feedforward cancellation," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 66, no. 4, pp. 1620 – 1631, 2019.

[40] J. A. Garcıa-Naya, O. Fresnedo, F. J. Vazquez-Araujo, L. Gonzalez-Lopez, M andCastedo, and J. Garcia-Frias, "Experimental Evaluation of Analog Joint Source-Channel Coding in Indoor Environments," *in Proc. IEEE International Conference on Communications (ICC)*, 2011.

[41] J. Zhang, Y. Wang, L. Ding, and N. Zhang, "Bit Error Probability of Spatial Modulation over Measured Indoor Channels," *IEEE Transaction on Wireless Communication*, vol. 13, no. 3, pp. 1380–1387, 2014.

[42] F. Restuccia and T. Melodia, "Deepwierl: Bringing deep reinforcement learning to the internet of self-adaptive things," in *IEEE Conference on Computer Communications (INFOCOM)*, 2020, pp. 844–853.

[43] X. Wang, Y. Zhu, Y. Ha, M. Qiu, and T. Huan, "An fpga-based cloud system for massive ecg data analysis," *IEEE Transactions on Circuits and Systems II: Express Briefs*, vol. 64, no. 3, pp. 309 – 313, 2017.