Sub-Terahertz Devices and Test Metrology

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***Abstract*—As 6G wireless communications push the operation frequency above 110 GHz, it is critical to have low-loss interconnects that can be accurately tested. To this end, D-band (110 GHz to 170 GHz) substrate-integrated waveguides (SIWs) are designed on a 100-µm-thick SiC substrate. The fabricated SIWs are probed on-wafer in a single sweep from 70 kHz to 220 GHz with their input/output transitioned to grounded coplanar waveguides (GCPWs). From CPW-probed scattering parameters, two-tier calibration is used to de-embed the SIW-GCPW transitions and to extract the intrinsic SIW characteristics. In general, the record low loss measured agrees with that obtained from finite-element full-wave electromagnetic simulation. For example, across the D band, the average insertion loss is approximately 0.2 dB/mm, which is several times better than that of coplanar or microstrip transmission lines fabricated on the same substrate. A 3-pole filter exhibits a 1-dB insertion loss at 135 GHz with 20-dB selectivity and 11% bandwidth, which is order-of-magnitude better than typical on-chip filters. These results underscore the potential of using SIWs to interconnect transistors, filters, antennas, and other circuit elements on the same monolithically integrated chip.**

***Index Terms*—Calibration, millimeter wave integrated circuits, semiconductor waveguides, silicon carbide, transmission lines**

I. Introduction

CONVENTIONAL microwave monolithic integrated circuits (MMICs) are based on coplanar or microstrip transmission lines, which, at frequencies above 110 GHz, suffer from high loss, significant crosstalk, and limited power capacity. By contrast, substrate-integrated waveguides (SIWs) [1] have low loss, minimum crosstalk, and high power capacity. However, because the size of SIWs is on the order of the guided wavelength λ, SIWs are usually implemented at the board level for hybrid integration with active devices. Monolithic integration becomes feasible when the operation frequency exceeds 110 GHz, so that $\lambda < 1$ mm in a typical semiconductor such as Si. In the case of high-power GaN-on-SiC MMICs, SIWs are especially attractive because SiC is high in dielectric constant, electrical resistivity, breakdown strength, mechanical toughness, and thermal conductivity, but low in loss tangent [2]–[5]. Table I compares these properties of SiC with those of Si and other substrate materials.

Table II shows that, despite the advantages of SIWs, to date there are few reports of SIWs above 110 GHz [6]–[12], whether on Si or SiC. In this paper, we demonstrate D-band (110–170 GHz) SiC SIWs with an insertion loss of 0.2 ± 0.1 dB/mm. Also fabricated on the same wafer is a 3-pole SIW filter with a 1.0-dB insertion loss at 135 GHz and an 11% 3-dB fractional

TABLE I
PROPERTIES OF COMMON SUBSTRATE MATERIALS

Property	Quartz	Sapphire	Si	GaAs	InP	GaN	AlN	SiC	Diamond
Dielectric Constant	3.8	10	12	13	9.6	8.9	8.5	9.7	5.7
Loss Tangent	10^{-4}	10^{-4}	10^{-4}	10^{-4}	10^{-3}	10^{-4}	10^{-4}	10^{-4}	10^{-4}
Resistivity (Ω·cm)	10^{20}	10^{18}	10^{5}	10^{5}	10^{6}	10^{5}	10^{14}	10^{5}	10^{13}
Breakdown Field (MV/cm)	10	1	0.3	0.5	0.5	3	15	3	10
Thermal Cond. (W/cm°C)	0.05	0.4	1.3	0.5	0.7	2.5	3.4	4.2	100
Thermal Exp. (ppm/°C)	0.6	0.6	2.5	5.7	4.5	3.2	4.5	4.8	1
Fracture Tough. (MPa·m^{½})	0.7	1.3	0.8	0.8	1.2	0.8	4.5	4.6	3.4

TABLE II
SUBSTRATE-INTEGRATED WAVEGUIDES ABOVE 110 GHZ

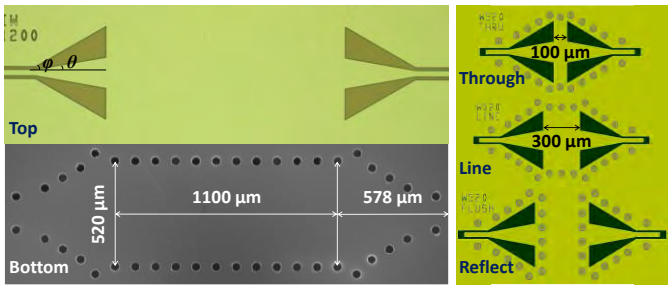
Year	Substrate	Bandwidth (GHz)	Insertion Loss (dB/mm) [a, b]	Return Loss (dB) [a]	Reference
2010	Si	95–200	4–6	>14	[6]
2012	Si	150–210	2–3	>16	[7]
2017	SiC	160–220	0.4–0.7		[8]
2018	Si	110–170	0.4–0.6	>14	[9]
2019	SiC	150–220	0.5–1.2		[10]
2020	Si	243–325	0.4–1.0	>17	[11]
2021	SiC	110–170	0.3±0.1	>17	[12]
2023	SiC	110–170	0.4±0.1[c]	>17	This Work

[a]For the SIW in series with two SIW-GCPW transitions at its input/output
[b]Normalized by the total length of the SIW and two SIW-GCPW transitions
[c] 0.2±0.1 dB/mm after transitions are de-embedded by two-tier calibration.

TABLE III
> 110 GHZ FILERS BASED ON SUBSTRATE-INTEGRATED WAVEGUIDES

Year	Substrate	Freq. (GHz)	Bandwidth	Insertion Loss (dB) [a]	Return Loss (dB) [a]	Reference
2020	Si	279	1%	9	20	[11]
2020	Si	140, 280	1%	3.9, 2.5	17, 11	[13]
2017	SiC	183	5%	~1	18	[8]
2021	SiC	135	11%	1	25	[12]
2023	SiC	195.6	1.5%	5.6	21.8	[14]
2023	SiC	135	11%	1.0	15	This Work

[a] For the SIW plus two GCPW-SIW transitions



(a) (b)

Fig. 1. (a) Front and back micrographs of a 1.1-mm-long D-band SIW in series with two 0.58-mm-long SIW-GCPW transitions at its input/output. (b) Composite layout of SIW calibration structures: "through," "line," and "reflect" [12].

bandwidth. This paper expands on [12] by including details about the SIW design, fabrication, characterization, and analysis. Optimization of the transition design is also discussed.

II. Design, Fabrication, and Characterization

A. Design and Simulation

Using analytical equations [15] and finite-element full-wave electromagnetic simulations (HFSS), D-band SiC SIWs are designed and optimized for the fundamental TE_{10} mode with a cut-off below 100 GHz. Each SIW has two rows of through-substrate vias (TSVs) with diameter d = 40 µm and center-to-center spacing s = 100 µm [Fig. 1(a)]. The two TSV rows are parallel to each other with center-to-center spacing w = 520 µm. The simulated SIW characteristics are plotted together with the measured characteristics in section III.

To facilitate wafer probing, each SIW is transitioned [16], [17] to a grounded coplanar waveguide (GCPW) [18] at both the input and output. Each transition is 578-µm long, including a 175-µm GCPW section, a 353-µm tapered section, and a 50-µm SIW section [Fig. 1(a)]. In the GCPW section, the center electrode is 30-µm wide with a 16-µm gap from the ground electrodes. In the tapered section, the center electrode is linearly widened to 155 µm while the gap is linearly widened to 158 µm, corresponding to $\theta = 10°$ and $\varphi = 30°$ for the inner and outer tapers, respectively, of the gap. Fig. 2 illustrates the effects of θ and φ on the characteristics of a 1.1-mm-long SIW in series with two SIW-GCPW transitions at its input/output. It can be seen that deviations from optimum θ and φ increase the ripples in the reflection and transmission coefficients S_{11} and S_{21}, thereby compromising the return loss while aggravating the insertion loss across the band. Further, the effect of $\Delta\varphi$ is more prominent than that of $\Delta\theta$. Therefore, iterative optimization of θ and φ starts with φ first. Note that with fixed w and φ, the length of the tapered section is approximately $(w/2)\cdot\text{cotan}\,\varphi$.

To extract the intrinsic SIW characteristics from those measured on the GCPW-SIW-GCPW series, through-reflect-line (TRL) calibration structures [19] are laid out [Fig. 1(b)] and fabricated on the same SiC substrate as the SIWs. Composite layouts, overlapping frontside and backside features, are shown in Fig. 1(b) because they reveal more details than separate frontside and backside micrographs as shown in Fig. 1(a).

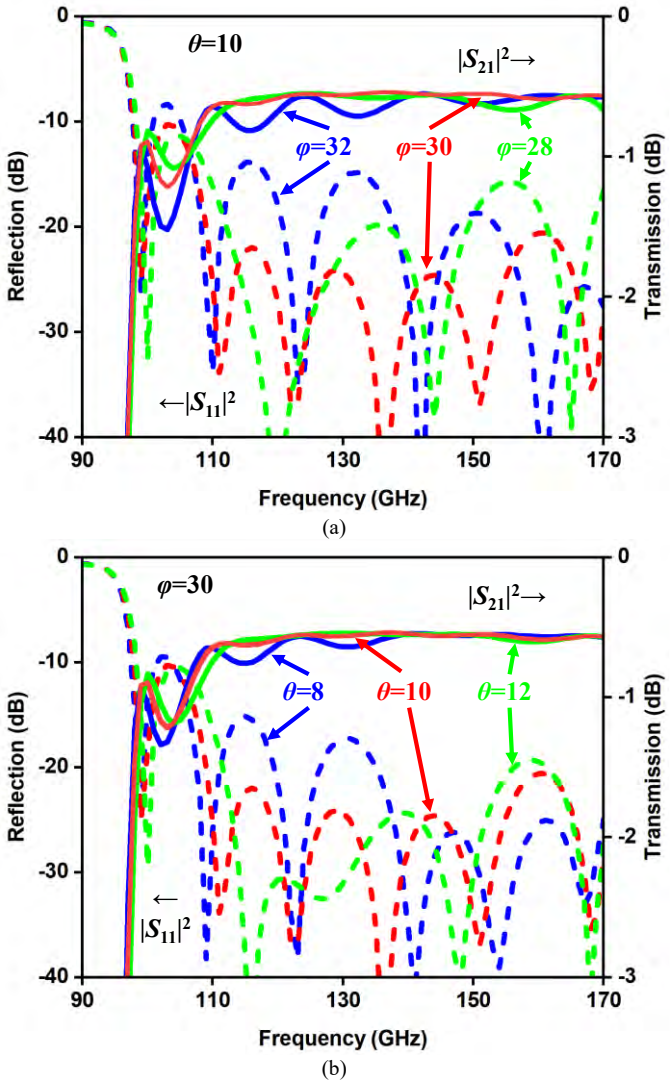


Fig. 2. Simulated effects of (a) the inner taper θ and (b) outer taper φ on S_{11} (dash) and S_{21} (solid) of the GCPW-SIW-GCPW series of Fig. 1(a).

B. Fabrication

Fig. 3 illustrates the SIW fabrication sequence. The fabrication starts with a 100-mm-diameter, 100-µm-thick high-purity 4H-SiC substrate having > 10^6 Ω·cm resistivity. For frontside processing, the Si face of the substrate is patterned with 100-nm-thick Ni and 700-nm-thick Al, both electron-beam evaporated. The total metal thickness is three times the skin depth at 140 GHz. For backside processing, the substrate is flip-mounted on a sapphire carrier using a thermal bond. A 100-nm-thick Ni seed layer is sputter-deposited, then patterned with a 7-µm-thick photoresist layer before a 5-µm-thick Ni layer is electroplated. This electroplated Ni layer serves as the mask for TSV etching. Before TSV etching, the photoresist layer is removed by solvents and the Ni seed layer is removed by ion milling. After TSV etching, the Ni mask is wet-etched, and a 100-nm-thick Ni adhesion layer and 2-µm-thick Al layer are sputter-deposited. Finally, the SiC substrate is debonded and cleaned.

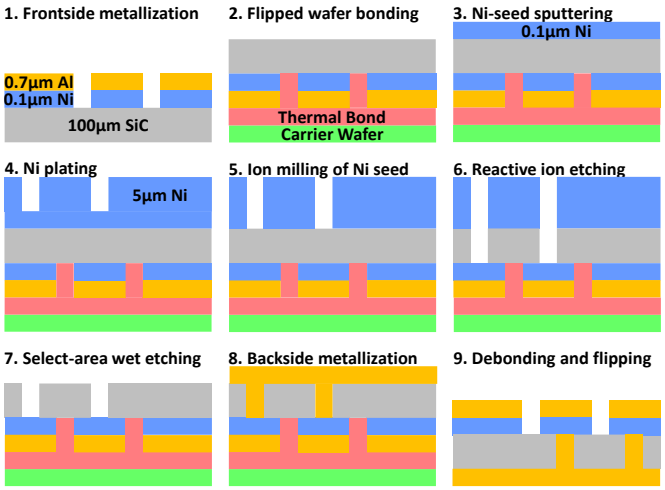
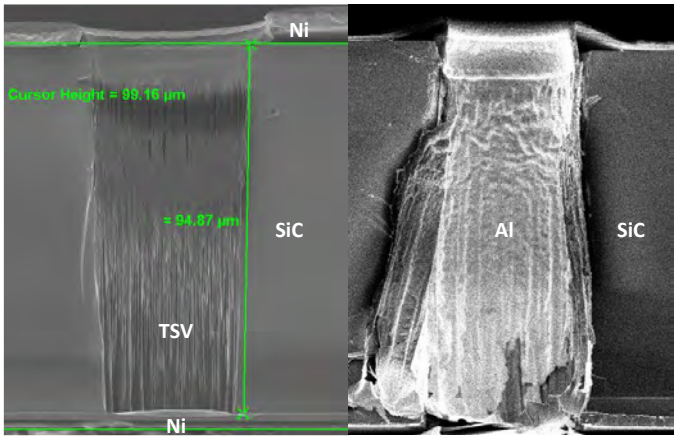


Fig. 3. Schematic illustration of the SIW fabrication sequence.



(a) (b)

Fig. 4. Scanning electron micrograph of a TSV cross-section after (a) etching away 95-µm SiC and (b) complete etching through the SiC and backside metallization.

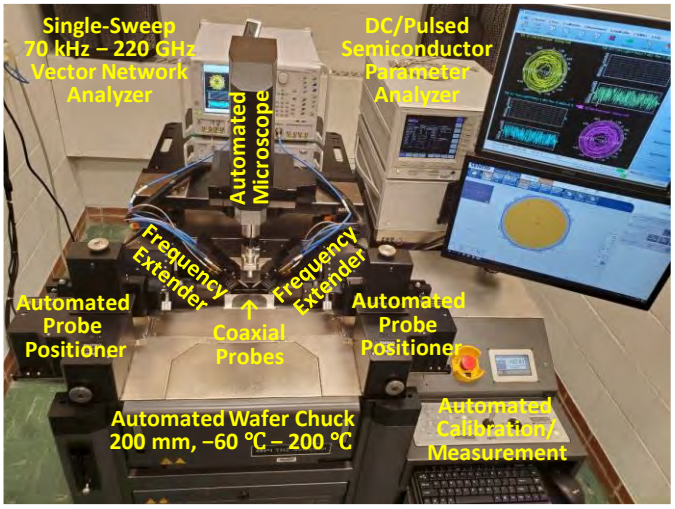


Fig. 5. Measurement setup.

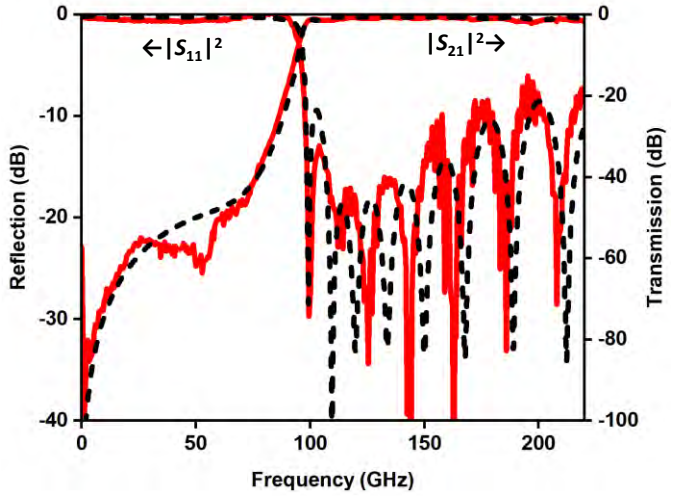


Fig. 6. Measured (solid) vs. simulated (dash) magnitudes of S_{11} and S_{21} of the GCPW-SIW-GCPW series with optimized SIW-GCPW transitions.

TSV etching is the most challenging step in SIW fabrication. TSVs are etched in an Oxford Cobra inductively-coupled-plasma (ICP) reactive-ion etcher (RIE) with 50 sccm SF_6 and 10 sccm O_2 under 10 mTorr vacuum, 2000-W ICP power, and 50-W RIE power. The etch rate of SiC is approximately 15 µm/h with a 50:1 selectivity over Ni. Fig. 4(a) shows a uniform etch front after etching away 95 µm of SiC and just before it reaches the frontside metal. Fig. 4(b) shows the TSV cross-section after completing SiC etching and backside metallization. It can be seen that the TSV sidewall is well covered by Al. The jagged appearance is caused by mechanical cleaving. Macroscopically, it can be seen in Fig. 1(a) that the TSVs are uniform with high yield.

C. Characterization

Fig. 5 shows that the measurement setup comprises an Anritsu ME7838G 70-kHz-to-220-GHz single-sweep VNA, an MPI TS2000-IFE automated probe station, two 220-GHz 0.6-mm-dia coaxial probes with 50-µm pitches. A two-tier calibration is applied sequentially. Tier-1 calibration establishes the reference planes at the probe tips, using the load-reflect-reflect-match (LRRM) method [20] and an MPI TCS-050-100-W impedance standard substrate. Tier-2 calibration shifts the reference planes beyond the SIW-GCPW transitions to the intrinsic SIW section, using the TRL method and the calibration structures shown in Fig. 1(b).

III. Results and Discussion

A. GCPW-SIW-GCPW Series

Fig. 6 compares the measured S_{11} and S_{21} (after tier-1 calibration with the reference planes at the probe tips) of a GCPW-SIW-GCPW series with a total length of 2.26 mm (S_{22} and S_{12} are comparable to S_{11} and S_{21}, respectively, and not shown). It can be seen that the measured and simulated results agree across the entire 220-GHz bandwidth, even when the insertion loss approaches 100 dB. Across the D band, the measured return loss is greater than 17 dB, confirming that both the SIW and the SIW-GCPW transition are broadband. The measured insertion loss of 0.80 ± 0.13 dB corresponds to

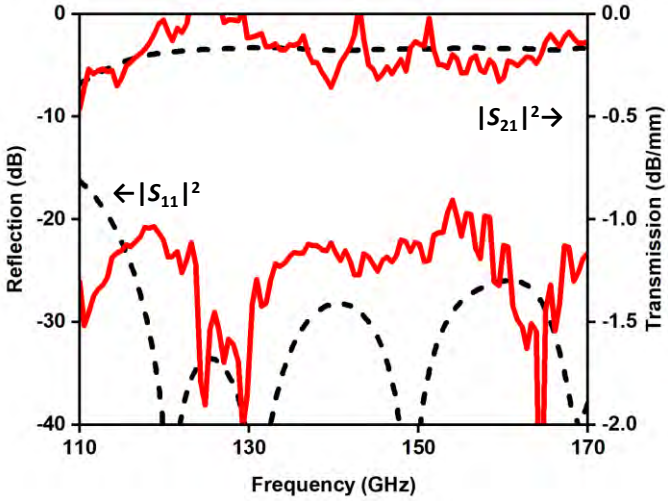


Fig. 7. Measured (solid) vs. simulated (dash) magnitudes of S_{11} and S_{21} of the 1.1-mm-long intrinsic SIW section.

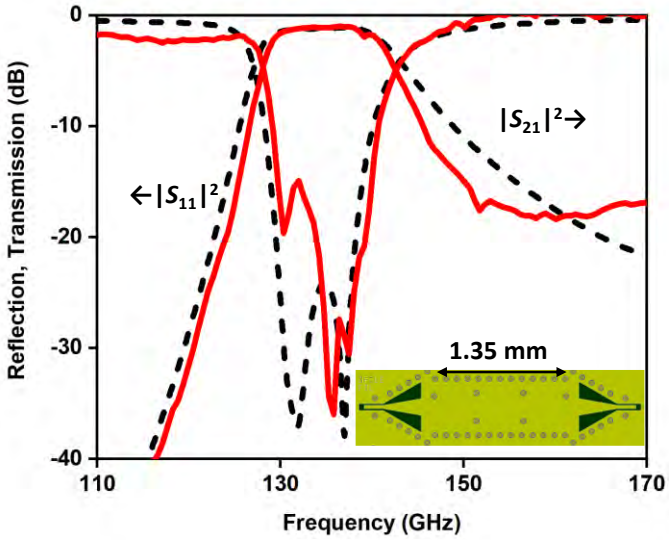


Fig. 8. Measured (solid) vs. simulated (dash) magnitudes of S_{11} and S_{21} for a three-pole SIW filter.

approximately 0.4 ± 0.1 dB/mm when normalized by the total length of the SIW and the two SIW-GCPW transitions. (Table II data, including those of [6]–[12], all include one SIW and two SIW-GCPW transitions in the loss and length). The insertion loss reported here is higher than [12]. This can be attributed to the degradation of the probe pads on the SIW-GCPW transition, as the relatively thin (0.7-µm Al) pads are repeatedly probed (confirmed in the next subsection). Indeed, it is found that the SIW-GCPW transition has 0.3 ± 0.1 dB insertion loss [21], which is 0.1 dB higher than that reported in [12]. Note that in this work we have repeated all measurements on the same SIW die, to avoid any additional uncertainty from die-to-die variation.

B. Intrinsic SIW Section

Fig. 7 compares the measured and simulated S_{11} and S_{21} (after tier-2 calibration and with the reference planes beyond the SIW-GCPW transitions) of the 1.1-mm-long intrinsic SIW section. Across the D band, the return loss is greater than 17 dB and the average insertion loss is approximately 0.2 ± 0.1 dB/mm, much lower than the value with the SIW-GCPW transitions included. For such a low loss, the data is inevitably noisy. Additionally, parasitic modes launched by the CPW probe onto the SIW-GCPW transition may not completely dissipate before reaching the intrinsic SIW section. This can be alleviated by lengthening the GCPW section of the transition beyond 175 µm, with the tradeoff of larger size and higher loss.

C. SIW Filter

Fig. 8 compares the measured and simulated magnitudes of S_{11} and S_{21} for a three-pole filter comprising a 1.35-mm-long SIW and two GCPW-SIW transitions. It can be seen that the measured results agree with that simulated by using a dielectric constant of 10.2 for SiC [22], [23]. The measured insertion and return losses are 1.0 dB and 15 dB, respectively, at the band center of 135 GHz. The 3-dB bandwidth is 15 GHz or 11%. The out-of-band rejection is greater than 40 dB and 20 dB below and above, respectively. These characteristics are consistent with the high-Q resonators and represent the state of the art of SiC SIW filters (Table III) [12]. They are order-of-magnitude better than that of Si on-chip filters. The rejection below band takes advantage of the SIW cut-off characteristics. The rejection above band can be improved by suppressing higher-order modes.

IV. Conclusion

With a broadband, relatively short, and low-loss SIW-GCPW transition, the D-band SiC SIW exhibits a record-low loss of approximately 0.2 dB/mm. The three-pole filter, with an insertion loss of 1.0 dB, represents the state of the art of SiC SIW filters and is order-of-magnitude better than Si on-chip filters. This shows that above 110 GHz, SiC SIWs may be small enough to replace coplanar or microstrip transmission lines as interconnects for high-power MMICs. Additionally, SiC SIW may enable monolithic integration of high-quality filters and edge-firing antennas on the same chip, which has been challenging for MMICs at any frequency. These SIW-based MMICs can in turn form a linear RF frontend array on a single SiC chip with $\lambda_0/2$ pitch, because $\lambda_{TE10} \approx \lambda_0/3$ on SiC and there is little crosstalk between adjacent SIWs.

V. Acknowledgement

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