Design of 145 GHz BPSK SDR on RF-SoC

Kasun Karunanayake, Hasitha Weerasooriya, Gayani Rathnasekera, Arjun Singh, Josep M. Jornet,
Theodore S. Rappaport and Arjuna Madanayake

***Abstract*—Wireless links at sub-THz bands require low-SWaP SDR modems. We report early design experimentation of an SDR operating in the 130-150 GHz band, with ASK/BPSK/QPSK modulation on I/Q channels, at a maximum data rate of 128 Mbps. The design utilizes 110-170 GHz front-ends from Virginia Diodes, and Xilinx RF-SoC ZCU-111 for DSP operations. A 1 GHz baseband example at 145.5 GHz is provided. The experiment uses horn antennas with 21 dB gain. The SNR is about 40 dB without cross correlation gain in the detector which provides an additional 15 dB in link margin. Real-time bit rate of 128 Mbps is achieved. Example applications include vehicle-to-vehicle, vehicle-to-infrastructure, backhaul, device-to-aerostat. This paper provides a platform from which further design work will lead to increased data rate and/or range, and enhance security through encryption. Future designs will facilitate digital interfaces, such as, ethernet, AXI, PCIe and USB-C.**

***Index Terms*—Sub-THz, wireless, SDR, RF-SoC.**

I. Introduction

High-capacity wireless communications in the sub-terahertz (100–300 GHz) bands is promising due to abundant bandwidth [1]. Mobile applications for line of sight (LoS) communications, such as, device-to-aerostat or inter-drone, will typically require at least 100 Mbps over 10 km [1]–[3]. Sub-THz wireless systems using gigabit per second data rates will benefit from power efficient and compact low-SWaP algorithms [4]. As a first step towards supporting wide-ranging research and experimentation at sub-THz communications and sensing, we detail the implementation of end-to-end 130-150 GHz radio-frequency (RF) SDR having baseband bandwidth up to 1 GHz with a field-programmable gate-array (FPGA) platform for digital signal processing (DSP) [5]. The SDR is evaluated using a vector network analyzer (VNA) to obtain performance estimates based on end-to-end measurements. The FPGA is interfaced to the microwave baseband signal across an instantaneous bandwidth of 1 GHz (500 MHz intermediate frequency, double sideband suppressed carrier modulation) using time-interleaved analog-to-digital and digital-to-analog (ADC/DAC) components that are available within the Xilinx RF-SoC chip. While wireless communications systems operating with 1 GHz RF bandwidths at millimeter wave and sub-THz frequencies have been developed and deployed for channel sounding and propagation measurement and modeling studies [6]–[8], this work offers a flexible, SDR for a wide range of applications.

II. Description of the 130-150 GHz SDR

Fig. 1(Top) shows the design of the 130-150 GHz RF front-end and DSP back-end [5]. The RF front-end consists of an up-converter, power amplifier (PA) and down-converter,

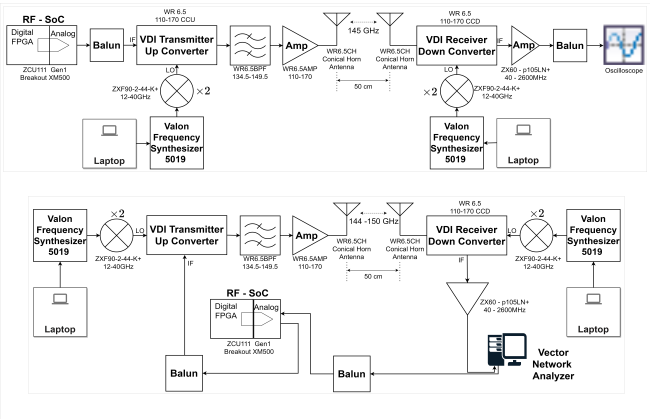

Fig. 1. Top) real-time BPSK/ASK waveforms monitored on oscilloscope, 40 dB SNR and 32 samples/symbol, ADC sample rate 4 GS/s with 8 phases; Bottom) calibrated VNA to measure transfer function in 145-147 GHz band with DAC+Tx+Channel+Rx+ADC+DSP in circuit. A wireless connection requires an RF-SoC at each end.

provided from Virginia Diodes Incorporated (VDI). The digital back-end consists of Xilinx RF-SoC chip (XCZU28DR-2FFVG1517E) hosted on a ZCU-111 board. The up-converter from VDI consists of a small signal amplifier followed by a mixer (conversion loss of 10 dB). This mixer requires a local oscillator (LO) in the 130-150 GHz range, which is derived via a chain of frequency multipliers. The modulated RF carrier within the 130-150 GHz band is bandpass filtered and then applied to the PA which provides 20 dBm at the transmit antenna. This example design has 1 GHz bandwidth (145-146GHz). At the receiver, the horn antenna feeds a down-converter/mixer (conversion loss 10 dB), and the low-pass signal is amplified and provided at the intermediate frequency (IF) output port of the VDI down-converter unit. The VDI up/down converters require LO inputs in the range 32.5-37.5 GHz, which are quadrupled to produce the final LOs. The input LO is doubled using Valon-RF sources, which are configured via user interface software. The Xilinx ZCU-111 contains eight ADCs and eight DAC channels, which supports a ADC/DAC sampling frequencies of 4.096 GS/s at 12-bit quantization. A single ADC/DAC channel is evaluated within baseband of 0-2 GHz (145-147 GHz at RF) [9].

III. Real-Time Experimentation on ZCU-111

An SDR covering the 145-147 GHz band uses two Xilinx RF-SoC ZCU-111 systems at each node for modulating the transmit signal from input source data, and for demodulating the received signal into a received data stream. The end-to-

978-1-7335096-7-1 ©2024 ACES

end channel response, including the frequency dependence of the ADC/DACs, polyphase signal processing units on the RF-SoC (e.g., decimation block, output compensation filters (zero order hold) for instance), as well the frequency dependence of the VDI Tx/Rx units and external PA, were evaluated using the test setup shown in Fig. 1(Bottom) with the National Instruments (NI) sub-8 GHz Vector Network Analyzer (VNA) as a calibrated frequency response measurement system. The test ports of the VNA are calibrated to 50 ohms within the 300 kHz- 8 GHz for SDR baseband measurement. The VNA output power is set at 0 dBm feeding the ADC. DAC output is -16 dBm, within range of the VDI up-converter (WR 6.5 110-170 CCU). We measured the S_{12} between VNA ports 1 and 2 with the cascade of radio and RF-SoC as the device under test. The LO was set to produce an RF carrier at 146 GHz. The received signal from the VDI down-converter (WR 6.5 CCD 110-170GHz) is amplified using an LNA (MiniCircuits ZX60-p105LN+ 40-26000MHz) and applied to the ADC of the ZCU-111 (sampled at 4 GS/s and then decimated by factor 2). The sampled digital received signal, in 8 phases inside the RF-SoC's FPGA fabric, is fed to the DAC after up-sampling by factor 2, to yield the 4 GS/s output signal that is connected to port-2 of the VNA. The VDI PA and VDI receiver are both connected to horn antennas (110-170 GHz range of operation, gain 21 dB). The distance between Tx and Rx antennas is about 50 cm. Fig. 2(Left) shows the measured channel response within the 145-147 GHz band, shown at baseband as a single sided low-pass response. The channel is flat within $\pm 3dB$ within 900 MHz. The equivalent IQ baseband is 1.8 GHz. The SNR was measured at about 40 dB. We used binary phase shift key (BPSK) modulation with 32 samples per symbol for IF at 500 MHz, DAC sampling rate of 4 GS/s [10]. The FPGA uses 16 phases where each DAC phase is clocked at 250 MHz. We chose 50% duty cycle in a periodically modulated amplitude shift key (ASK) and BPSK waveforms for evaluation. Fig. 3 shows time-domain baseband Tx signal from the DAC and Rx signal from the VDI down-converter. BPSK modulation is equivalent to quadrature phase shift key (QPSK) modulation for IQ basebands, and allows for constant envelope operation at high PA efficiency because the peak to average power ratio (PAPR) is 0 dB. The BPSK-bitrate is 125 Mbps; this optimally requires correlation detection (CD), which can improve raw 40 dB SNR by another 15 dB. CD necessitates digital downconvertion (DC) followed by low-pass filtering via a cyclic integrate and comb (CIC) [11] or integrate-and-dump filter (I channel in Fig. 2(Right)).

IV. Conclusion

Hardware for 145-147 GHz band SDR was designed and experimentally evaluated for frequency response (VNA) and BPSK waveforms. The system uses RF-SoC ZCU-111 paired to VDI 110-170 GHz RF system. Future work includes replacing inbuilt VDI antennas (21 dB) with LHA-HG-WR06 (38 dB) and correlation detection (15 dB) that potentially adds 49 dB to the link budget, likely increasing the range to 140m. We will also extend to M-nary phase shift key (M-PSK), frequency shift key (FSK), and differential quadrature phase shift key (DQPSK) modulation.

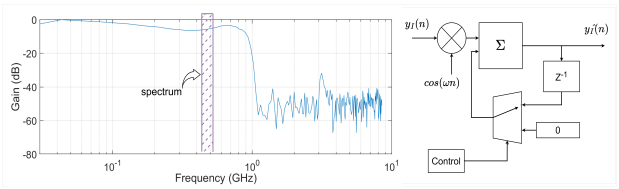

Fig. 2. Left) VNA measured 145-147 GHz (2 GHz) band: S_{1s} of DAC+Tx+Channel+Rx+ADC sampled at 4 GS/s and 8/16 ADC/DAC clock phases; Right) architecture for integrate and dump cross-correlator.

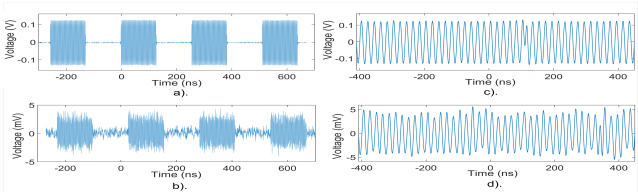

Fig. 3. Time domain modulated signals; data ...-1-0-1-0-1.... IF at 500 MHz, a) Tx ASK, b) Rx ASK, c) Tx BPSK (zoomed), and d) Rx BPSK (zoomed).

References

[1] T. S. Rappaport, Y. Xing, O. Kanhere, S. Ju, A. Madanayake, S. Mandal, A. Alkhateeb, and G. C. Trichopoulos, "Wireless communications and applications above 100 GHz: Opportunities and challenges for 6G and beyond," *IEEE Access*, vol. 7, pp. 78 729–78 757, 2019.

[2] H. Abdellatif, V. Ariyarathna, S. Petrushkevich, A. Madanayake, and J. M. Jornet, "A real-time ultra-broadband software-defined radio platform for terahertz communications," in *IEEE INFOCOM 2022 - IEEE Conference on Computer Communications Workshops (INFOCOM WKSHPS)*, 2022, pp. 1–2.

[3] P. Sen, J. V. Siles, N. Thawdar, and J. M. Jornet, "Multi-kilometre and multi-gigabit-per-second sub-terahertz communications for wireless backhaul applications," *Nature Electronics*, vol. 6, no. 2, pp. 164–175, 2023.

[4] A. Singh, I. V. Reddy, D. Bodet, and J. M. Jornet, "Bessel beams for 6G - A performance analysis," in *2022 56th Asilomar Conference on Signals, Systems, and Computers*, 2022, pp. 658–664.

[5] V. Ariyarathna, A. Madanayake, and J. M. Jornet, "Toward real-time software-defined radios for ultrabroadband communication above 100 GHz [application notes]," *IEEE Microwave Magazine*, vol. 24, no. 8, pp. 50–59, 2023.

[6] G. R. MacCartney and T. S. Rappaport, "A flexible millimeter-wave channel sounder with absolute timing," *IEEE Journal on Selected Areas in Communications*, vol. 35, no. 6, pp. 1402–1418, 2017.

[7] Y. Xing and T. S. Rappaport, "Millimeter wave and terahertz urban microcell propagation measurements and models," *IEEE Communications Letters*, vol. 25, no. 12, pp. 3755–3759, 2021.

[8] ——, "Terahertz wireless communications: Co-sharing for terrestrial and satellite systems above 100 GHz," *IEEE Communications Letters*, vol. 25, no. 10, pp. 3156–3160, 2021.

[9] C. Liu, M. E. Jones, and A. C. Taylor, "Characterizing the performance of high-speed data converters for RFSoC-based radio astronomy receivers," *Monthly Notices of the Royal Astronomical Society*, vol. 501, no. 4, p. 5096–5104, 2020. [Online]. Available: http://dx.doi.org/10.1093/mnras/staa3895

[10] C. T. Parisi, S. Badran, P. Sen, V. Petrov, and J. M. Jornet, "Modulations for terahertz band communications: Joint analysis of phase noise impact and papr effects," *IEEE Open Journal of the Communications Society*, vol. 5, pp. 412–429, 2024.

[11] E. Hogenauer, "An economical class of digital filters for decimation and interpolation," *IEEE Transactions on Acoustics, Speech, and Signal Processing*, vol. 29, no. 2, pp. 155–162, 1981.