Evaluation of the Bonding Strength of Die Attachment Techniques for Gallium Oxide Power Devices

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***Abstract*— The integration of gallium oxide (Ga_2O_3) in electronic packaging has gained significant attention in recent research due to its promising properties. Despite this growing interest, the technology remains predominantly at the academic research stage, largely due to a lack of comprehensive data on the packaging process. Die attachment is a crucial factor for establishing functional and reliable semiconductor packages. This study sheds light on various factors that can affect the bonding strength of Ga_2O_3 chips on conventional direct bonded copper (DBC). Several samples were prepared by attaching Ga_2O_3 and Si chips onto gold-plated DBCs using various die attachment materials and methods. The bonding strength of each sample was evaluated through shear testing. The results indicated that surface roughness, die attachment method, die attachment material, metallization, and chip size significantly influenced the bonding strength.**

Keywords*— Chip size, die attachment method, die attachment material, DBC, Ga_2O_3 chip, metallization, Si chip, shear test, surface roughness.

I. Introduction

The ultra-wide bandgap energy (4.8-4.9 eV) of gallium oxide (Ga_2O_3) makes it a potential next-generation power semiconductor device promising high breakdown electrical strength (~8MV/cm), low intrinsic carrier concentration, and high operation temperatures [1]. In order to fully exploit the advantages of Ga_2O_3, the thermal and mechanical packaging challenges are required to be investigated. Numerous studies have used Ga_2O_3 to address higher breakdown voltage, surge current, lower thermal resistance, and subthreshold swing requirements [2-5]. The materials inside the package assemblies are expected to withstand high temperatures as well as function reliably. The electrical performance, thermal management, and reliability highly depend on the die attachment material connecting the chip with the substrate and the method of the attachment. The advanced die attachment methods involve attaching one terminal of the chip to the substrate by lead or lead-free solder alloys or electrically conductive adhesives, and the other terminals are connected by gold (Au) or aluminum wire bonding technology.

The mechanical bond between the die and substrate acts as a shield that protects the delicate die from shock and physical strain. Furthermore, the connecting layer serves as a thermal bridge facilitating efficient heat transfer from the die to the substrate. Therefore, the study of the potential factors that might have a substantial impact on the bonding strength of Ga_2O_3 is pivotal. The bonding strength of the die attachment predominately depends on the surface roughness of the wafer, chip size, metallization, die attachment technique, die attachment material, and surface cleanliness. Tseng et. al. showed in their work that surface roughness greatly impacts the bonding strength of Si wafers with Pyrex glass [6]. Their experimental results reveal that at 2 MPa contact pressure, the bonding strength decreases linearly with the surface roughness. The authors in [7] demonstrated that the area of the chip has a significant impact on the coefficient of thermal expansion (CTE) mismatch that affects the bonding strength.

Attaching SiC die and the substrate with silver (Ag) nanoparticles, the authors of [8] demonstrated that thermal aging affects the bonding strength. Their experimental results show that during thermal aging at 350ºC, the sintering joint exhibits good shear strength (e.g., 100 N/cm^2) till 72 hours of aging. After 96 hours the shear strength comes down to 16 N/cm^2 due to the silver oxide formation. The authors of [9] showed in their investigation that the apparent porosity and the thickness of the Ag sintered layer hold a linear relationship with the bonding strength. They also showed that bonding strength has a nonlinear relationship with the drying time, sintering pressure, and temperature. The effect of metallization is illustrated in one of the experiments in [10]. They attached Ag metallized SiC Schottky diode with Au / Ag plated DBC utilizing Ag sintering. Their experimental results demonstrated that Ag-plated DBCs show superior bonding strength over Au-plated DBCs.

Several heterostructures are proposed in some studies to efficiently address the self-heating property of β-Ga_2O_3. The authors of [11] attached β-Ga_2O_3 with Si substrate using O_2-plasma activation at room temperature. They showed that higher annealing temperatures lead to a higher bonding strength of 6.3 MPa as it helps to convert weak van-der-walls bonds to direct bonds. However, over-activation time intends to weaken the bond because of oxidation. In a similar manner, β-Ga_2O_3 was bonded with diamond in [12]. Their experimental results show that bonding strength can be promoted to 14 MPa from 0.5 MPa by annealing at 250ºC for 24 hours. More heterostructures, e.g., β-Ga_2O_3/4H-SiC, Ga_2O_3-SiC formation can be found in [4,13,14] but measuring bonding strength with shear test was out of the scope for the works.

In this paper, the factors influencing the bonding strength of Ga_2O_3 chips are investigated. While existing literature extensively covers the bonding of β-Ga_2O_3 with diamond substrates, β-Ga_2O_3/4H-SiC, or other heterostructures for thermal management, the direct die attachment of unprocessed Ga_2O_3 chips to traditional DBC substrates has not been thoroughly explored. The purpose of this work is to

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clarify several aspects that may influence the Ga_2O_3 wafer's bonding strength on conventional DBC substrate. The rest of the paper is organized as follows. Section II gives the theoretical aspects of different factors that affect the bonding strength. Section III shows the experimental setup. The experimental results are shown in section IV. Finally, section V draws the conclusion based on the experimental results.

II. Different Factors Affecting Bonding Strength

The major factors that affect the bonding strength of the die and DBC are, surface roughness, die attachment methods, die attachment temperature and pressure, die attachment materials, metallization, dimension of the chip, surface cleanliness, and so on.

A. Surface Roughness

Surface roughness encounters an essential function in defining the strength of the bonds that form between materials. The complex interplay between the topographical features of two surfaces during bonding has a significant impact on the bonding strength. The bonding strength is primarily affected by surface roughness, which also impacts the contact area and the distribution of stresses across the interface. The number of atomic or molecular connection platforms decreases as surface roughness increases because the precise contact region between the bonding surfaces gets reduced. This reduction in contact area leads to fewer bonds forming between the surfaces, which in turn results in poor adhesion. Furthermore, stress concentration regions are created at the interface by roughness characteristics like peaks and valleys. These stress concentration regions are more prone to distortion and failure under applied stresses, which lowers the bond's overall strength.

B. Die Attachment Techniques

A die can be attached to the substrate through different methods, for instance, Ag sintering die attach, lead/ lead-free die attach, eutectic die attach, epoxy die attach, flip chip, wire bonding, and ultraviolet die attach. However, Ag sintering has gained significant attention in the packaging industry due to its electrical and thermal properties [9]. Ag sintering involves two methods namely, pressured and pressure-less Ag sintering. Pressured Ag sintering is expected to give superior bonding strength because it increases the interparticle contact and facilitates dense and uniform bond formation. In addition, the external pressure helps to minimize the void formation by expelling trapped air and volatiles from the interface.

C. Die Attachment Materials

Eutectic compounds, conductive adhesives, and solder alloys are often utilized materials for die attachment, sometimes referred to as die bonders. These materials are selected based on a number of criteria, including their electrical and thermal conductivity, mechanical strength, and compatibility with substrate and die materials The electrical device's efficiency and reliability can be significantly impacted by the die attach material adopted for packaging [15]. Metal alloys are preferred for their promising thermal and electrical properties. For example, one of the most utilized metal alloys for die attachment is gold-tin (AuSn) which offers a high thermal conductivity of 58 W/mK and a melting point of 280°C. Owing to these properties, it is a great option for high-power systems where effective heat dissipation is essential. However, this method is less appealing in low-cost appliances because of the high cost of Au. Lead-tin and lead-free solder alloys are currently extensively utilized for connections between devices and packages. However, Compatibility between Au metallization and solder alloys containing tin (Sn) must be taken into account. Due to the larger surface energy of nanoscale silver [16, 17], it can be sintered under low processing temperatures (~250ºC). Therefore, nanoscale Ag can be a potential high-performance die-attach for packaging electronic devices.

D. Metallization

The proper choice of solder material greatly depends on the metallization. For example, silver sintering is suitable for titanium (Ti)/Au metallization. However, solder paste requires an additional Nikel (Ni) layer between Ti and Au because Au gets dissolved quickly in solder due to the Sn content [18]. The thickness of the Au, the reflow duration and temperature at liquidus, and the concentration of Sn in the solder combinely affect how much Au will be dissolved. Over scavenging of Au leads to the production of an Au/Sn intermetallic, which can embrittle the joint if the amount is considerable. When the assembly is subjected to thermal cycling, this kind of embrittlement may result in joint failure and cracking. Therefore, with the Ti/Au metallization, solder paste consumes Au and does not stick to Ti. Ni layer works as an adhesive layer in this case. Furthermore, which surface is being metallized also affects the bonding strength.

E. Dimension of the Chip

The area of the chip has a significant impact on the CTE mismatch that affects the bonding strength [7]. During the bond formation at higher temperatures, larger chips are more exposed to stress from CTE mismatch because the difference in contraction and expansion is intensified over a larger area. This results in a considerable temperature gradient and higher stress concentration, specifically at the edge of the chip, where localized strain can initialize cracks. These cracks propagate from the corner to the center of the chip reducing the effective bonding area. On the other hand, smaller chips encounter more uniform temperature distribution and reduced stress due to differential expansion. The relationship between bonding strength and chip dimension can be expressed by equation (1)

$$P = F/A \quad (1)$$

Where P is the bonding strength, F is the force applied to the chip and A is the area of the chip. If the applied force is kept constant, smaller chips will encounter higher bonding strength and larger chips will exhibit lower bonding strength.

III. Experimental Setup

For the experiments, samples are prepared by attaching Si chip or Ga_2O_3 chip over the aluminum nitride (AlN) DBC substrate. The copper of the DBC was Au-plated. The dimension of the Ga_2O_3 chip was 6.3 × 4.5 × 0.65mm. The measurement of the Si chip was 10 × 10 × 0.525mm. In order to maintain a similar setup for the experiments, the Si

Fig. 1: Diener electronic PICO 5

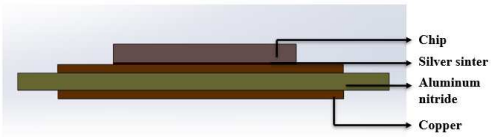


Fig. 2: Model of the sample

chips were diced with diamond tips. It is noteworthy that Si chips are fragile. Therefore, cutting them with a diamond saw might cause severe damage to the chip. One side of the Si chip was gold metallized, and the other side was chromium metallized. Similarly, the Ga_2O_3 chip had Au and no metallization on the other side. The surface cleanliness of the DBC was ensured by oxygen and argon cleaning using Diener electronic PICO 5 as shown in Fig.1. The oxygen cleaning removes the organic particles, and the argon cleaning removes the oxides from the DBC surface. Isopropyl alcohol was also used during the fabrication process. A 50µm thick silver paste or solder paste was applied to the DBC using precisely cut kaptan mask. The structure of the sample is shown in Fig. 2. The pressured and pressure-less silver sintered samples were fabricated using the hotplate controlling the pressure with ES 20 as shown in Fig. 4(a). Fig. 3 demonstrates the temperature

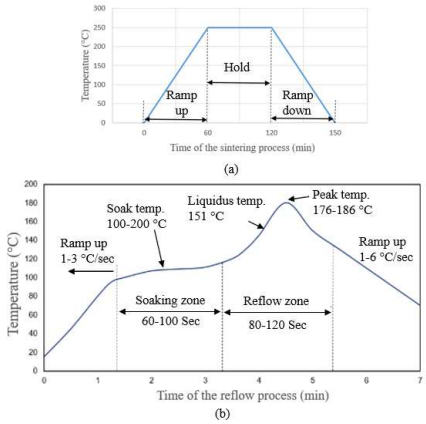


Fig. 3: Thermal profiles (a) UNIMEC H9890-6A silver paste, (b) Kester NP-510-LT solder [19]

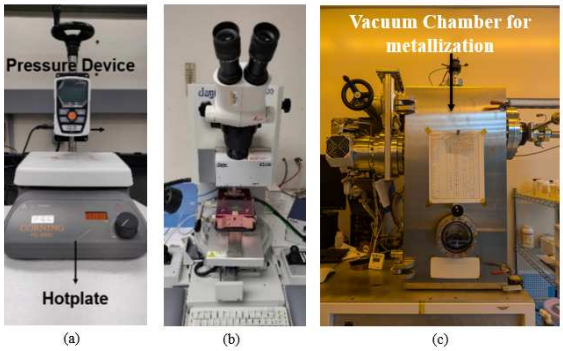


Fig. 4: Experimental setup (a) Hotplate and ES 20 for fabrication, (b) Dage DS 100 model used for shear test (c) Specialty Vacuum PVD-1 E-beam evaporator used for metallization

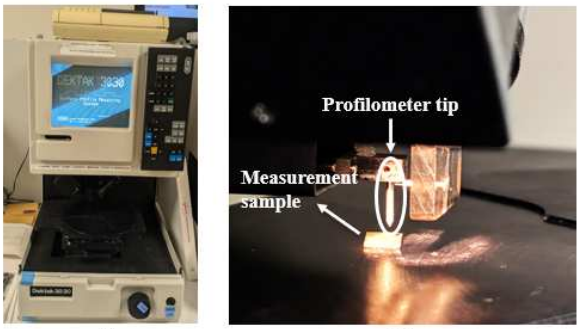


Fig. 5: Surface roughness measurement setup (a) Dektak 3030 profilometer (b) Profilometer tip used for surface roughness measurement of a sample

profile of the bonding materials used for different experiments. The samples with silver sintering were ramped up to 250ºC for 60 minutes. Then it was held for an hour and then cooled down for 30 minutes. Samples with solder paste are prepared using a reflow oven. Appropriate temperature profile was selected, and a weight was placed over the die to expel void from the bonding layer. The bonding strength was measured by shear test with Dage DS 100 (Fig. 4(b)). The Dage tip length was selected to be at least 80% of the chip length. In addition, shear height was selected based on the thickness of the bonding material. 100/100 nm Ti/Au metallization was done by Specialty Vacuum PVD-1 E-beam evaporator (Fig. 4(c)). The surface roughness of the chips was measured with Dektak 3030 profilometer equipment and tip as shown in Fig. 5(a) and 5(b) respectively.

IV. Results and Discussion

Several experiments were conducted by attaching Ga_2O_3 wafer or Si chip with DBC. The Si chip Au-plated side had a glossy polished surface (roughness ~ 1.9 nm) whereas the Ga_2O_3 wafer had comparatively rough surface (roughness ~ 300.9 nm). Fig. 6(a) and 6(b) introduce the chips that have been used. A light was incident on the samples to visualize the surface roughness. In case of a rough surface, the light reflects mostly from the higher peak areas of the chip as demonstrated in Fig. 6(c) (Ga_2O_3 wafer) whereas a smoother polished surface reflects the light more uniformly as shown in Fig. 6(d) (Si chip). The results of the surface roughness test are illustrated in Fig. 7. Initial experiments were done by doing pressured silver sintering on the diced Si chip and Ga_2O_3 wafer Au-plated surface. Table I shows 5.2 MPa (Fig. 8(a)) and 1.1 MPa shear strength for the Si chip and Ga_2O_3 chip respectively.

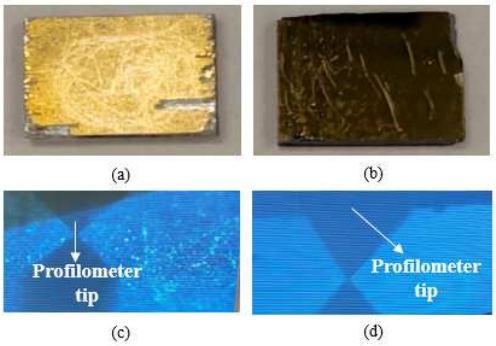


Fig. 6: Chips used for fabrication (a) Ga_2O_3 wafer (b) Si chip (c) surface roughness of Ga_2O_3 wafer (d) surface roughness of Si chip

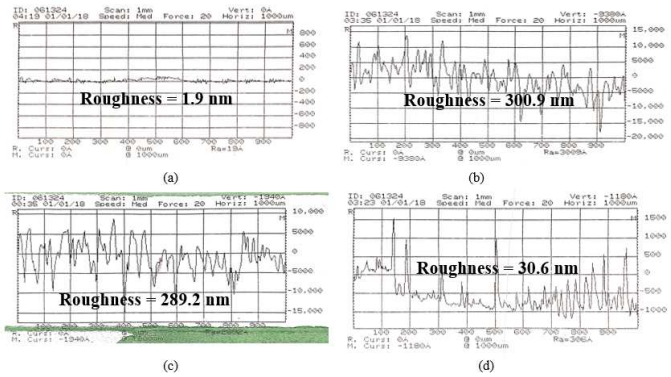


Fig. 7: Surface roughness (a) Si chip, (b) Ga_2O_3 wafer (c) reused Ga_2O_3 wafer (d) after metallization on Ga_2O_3 wafer unmetallized side

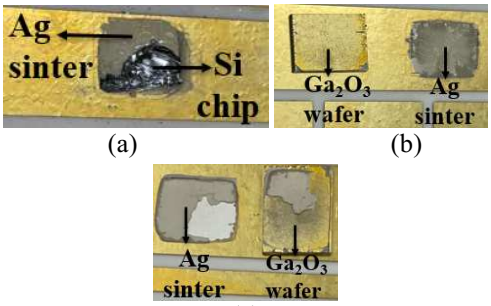


Fig. 8: Shear test results for surface roughness (a) diced Si dummy chip, (b) Ga_2O_3 wafer (c) reused Ga_2O_3 wafer

TABLE I. BONDING STRENGTH FOR DIFFERENT SURFACE ROUGHNESS

Die material	*Die attach material and method*	*Bonding strength (MPa)*
Si	Pressured silver paste	5.2
Si	Pressure-less silver paste	6.31
Ga_2O_3	Pressured silver paste	1.1
Ga_2O_3 (reused)	Pressure-less silver paste	7.09

The bonding strength decreases as surface roughness increases because the exact contact zone between the bonding surfaces gets smaller. Fig. 8(b) shows that almost no bond was created because most of the bonding material went to the valley area of the Ga_2O_3 wafer due to the external pressure in pressured Ag sintering. We reused the same Ga_2O_3 wafer for pressure-less silver sintering. Since some of the valley area was filled with bonding material after the previous experiment, it allowed more bonding material to stay in the contact region. By this time the surface roughness was reduced to 289.2 nm and the bonding strength was 7.09 MPa (Fig. 8(c)). Pressured silver sintering was expected to show higher bonding strength but due to the surface roughness, the results for Ga_2O_3 was showing higher bonding strength for pressure-less Ag sintering. However, Si chips also show a little discrepancy because the 10 × 10 mm^2 Si chips were diced with diamond tips which resulted in internal fracture during pressured Ag sintering process. Owing to this reason, the die fractured leaving a small portion of the chip on the substrate as shown in Fig. 8 (a). The bonding strength for pressured and pressure-less Ag sintering on the Si chip was 5.2 MPa and 6.31 MPa

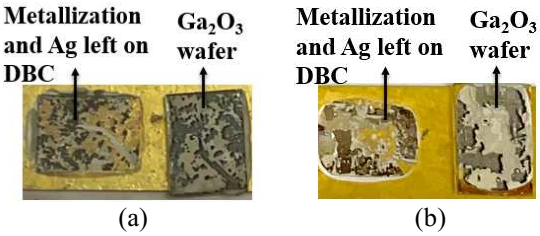


Fig. 9: Shear test results for different die attachment method on Ga_2O_3 wafer after 100/100 nm Ti/Au metallization (a) Pressured silver sintering, (b) Pressure-less silver sintering

TABLE II. BONDING STRENGTH FOR DIFFERENT DIE ATTACHMENT METHODS

Die material	*Die attach material and method*	*Bonding strength (MPa)*
Ga_2O_3	Pressured silver paste	3.44
Ga_2O_3	Pressure-less silver paste	2.24

respectively. A further experiment was conducted by metallizing the Ga_2O_3 chip with 100/100 nm Ti/Au. The surface that has been metallized, didn't have prior metallization. The surface roughness was measured to be 30.6nm after metallization which is 10% of the Au-plated surface used in the previous experiment. The bonding strength of pressured and pressure-less silver sintering were investigated as shown in Fig. 9. Since the external pressure helps to minimize the void formation by expelling trapped air on the interface, Table II shows that the bonding strength for pressured silver sintering was superior to the pressure-less silver sintering. However, some portion of the metallized layer was sticking with the DBC (Fig. 9(a,b)) because of poor metallization with e-beam evaporator and the surface roughness of the Ga_2O_3 surface. The metallization was more precise in the peak areas, but the metal atoms in the valley areas did not make a proper bond with the Ga_2O_3 surface. That weak metallization parts came out with the sinter layer during the shear test.

Furthermore, which surface is being metallized also affects the bonding strength. In one of the experiments, the Chromium (Cr) side of the Si dummy chip was metallized with 100/100nm Ti/Au and was attached to the DBC through pressured silver sintering. From Fig. 10, it can be observed that all the metallized layer is sticking to the DBC which indicates poor bonding of Ti with Cr surface.

Thereafter, the bonding strength using two different die attachment materials (Ag paste and solder paste) on Si chips was investigated. Experimental results in Table III demonstrate that bonding with pressure-less silver paste offers ~12% higher adhesive strength than the pressure-less solder paste. The reason is the intermetallic compound formation of solder paste during the reflow process weakens the bonding between the solder and chip. Due to the internal fracture during dicing, the Si chip was broken during the

TABLE III. BONDING STRENGTH FOR DIFFERENT DIE ATTACHMENT MATERIAL

Die material	*Die attach material and method*	*Bonding strength (MPa)*
Si	Pressure-less silver paste	6.31
Si	Pressure-less solder paste	5.62

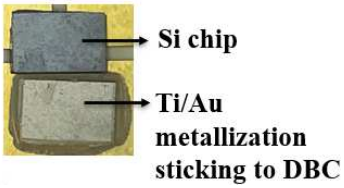
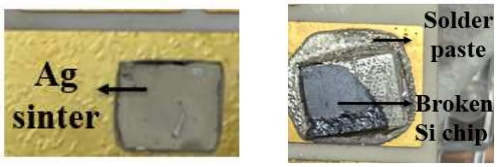


Fig. 10: Poor metallization on the Cr surface of the Si chip



(a) (b)

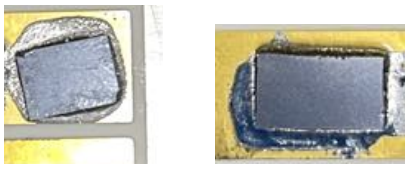
Fig. 11: Shear test results for different die attachment material (a) Pressure-less silver paste, (b) Pressure-less solder paste

shear test and couldn't be retrieved as shown in Fig. 11(a). This experiment was not conducted with Ga_2O_3 wafer because of the limited resources.

Finally, the impact of different chip sizes on bonding strength using pressure-less die attachment method with solder paste was investigated as shown in Fig. 12. Experimental results in Table IV show that for a 7.73mm^2 increase in the chip area, the bonding strength decreases by 27.58%. Larger chips are more vulnerable to stress from CTE mismatch during the bond formation at higher temperatures which results in distinct temperature gradient and increased stress concentration and results in lower bonding strength.

V. Conclusion

In this paper, different factors that can have significant impact on the bonding strength have been explored. According to the experimental results, surface roughness plays the most important role in strengthening the bond between the chip and DBC substrate. Pressured silver sintering with controlled temperature and pressure is found to be more promising than pressure-less silver sintering. Metallization and choice of die attachment material are interdependent. And larger chip size reduces the overall bonding strength due to the CTE mismatch. The current experimental results of Ga_2O_3 chips are not comparable to Si chips as they hold very different levels of surface roughness. The future work includes comparing the bonding strength of Ga_2O_3 wafer with SiC and Si wafer holding similar surface roughness levels. The effect of oxygen plasma activation and annealing will also be observed in addition to the factors discussed in this work.



(a) (b)

Fig. 12: Shear test results for different Si chip size (a) 6.3x4.5 mm^2, (b) 8.2x4.4 mm^2

TABLE IV. Bonding Strength for Different Chip Size

Die material	*Chip dimension (mm^2)*	*Bonding strength (MPa)*
Si	6.3 × 4.5	5.62
Si	8.2 × 4.4	4.07

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