Ramirez-Salgado, A., & Antonenko, P. (2024, October). Developing an Equity-Centered Hands-On Curriculum to Support Hardware Engineering Learning. Presented at the *2024 AECT International Convention, Kansas City, MO*.

Description:

Given the digital electronics industry's workforce shortage, fostering interest in hardware computing becomes imperative. Our NSF IUSE-funded project aims to address this by offering an inclusive, hands-on curriculum that involves FPGAs, IoT boards, and collaborative projects. Employing a DBR methodology, we systematically refine it through iterative analysis, design, development, and implementation. We have conducted three implementations, each informing the improvement of the curriculum with empirical evidence.

Developing an Equity-Centered Hands-On Curriculum to Support Hardware Engineering Learning

The semiconductor and digital electronics industry is rapidly evolving, impacting both industries and device capabilities. Despite hardware engineers' crucial role, shortages exist as students opt for software careers due to limited exposure to hardware.

To address this issue, our project, funded by the NSF Improving Undergraduate STEM Education (IUSE) program, aims to cultivate an early interest in hardware engineering. We are developing a hands-on, gamified curriculum that simplifies core hardware concepts by leveraging affordable educational tools like Field Programmable Gate Arrays (FPGA) and Internet of Things (IoT) boards.

Our project employs a Design-Based Research (DBR) methodology to improve the curriculum through iterative analysis, design, development, and implementation (Brown, 1992). In our presentation, we will discuss its evolution across a pilot test, a summer program with high schoolers, and an elective course for undergraduates.

Conceptual framework

Our curriculum's conceptual framework, outlined in Figure 1, prioritizes equity, experiential (Kolb, 2014), inquiry-based learning (Ismail et al., 2006), collaboration, reflection, and gamified experiences (Ndlovu & Mhlongo, 2020). Equity spotlights, including Universal Design for Learning (UDL) (CAST, 2018) and Culturally Sustaining Pedagogies (CSP) (Paris, 2012) principles, are integrated into each lesson. Informed by the TPACK framework (Niess, 2011), teacher implementation materials support lesson delivery. Rooted in engineering identity (Chemers et al., 2011) and persistence theories, the framework fosters situational interest (Hidi & Renninger, 2006) and self-efficacy (Bandura, 2010).

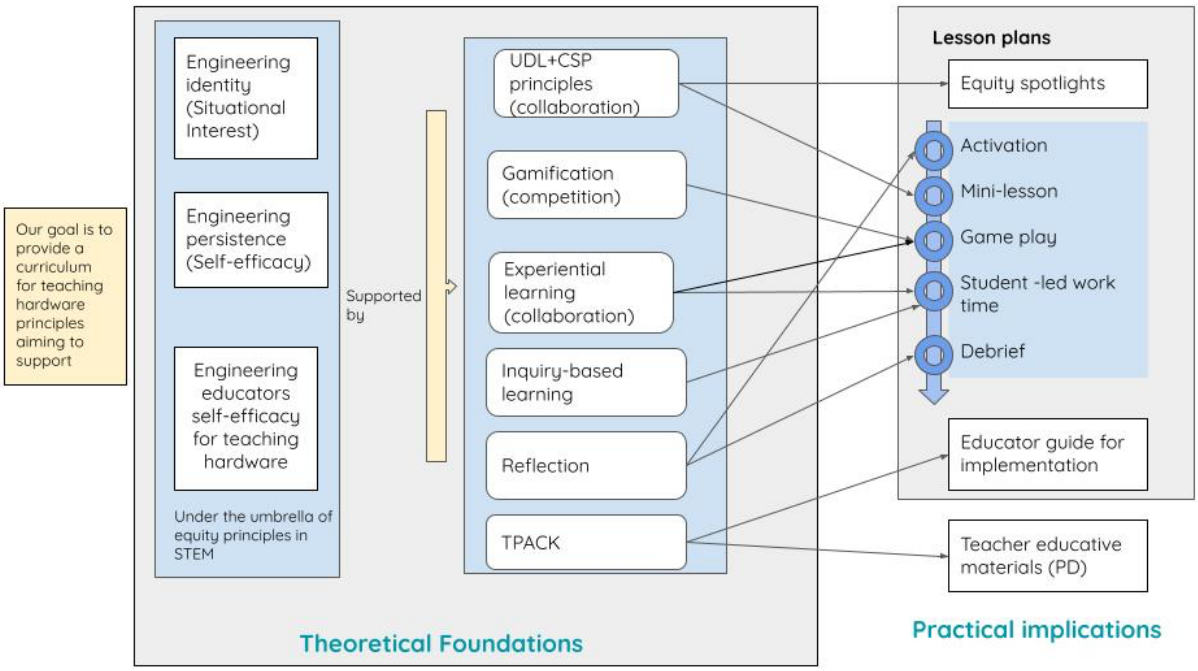

Figure 1. Curriculum conceptual framework

Method

Our DBR approach employs a range of mixed and relevant methods, such as phenomenological interviews, focus groups, and pre-posttest analyses, to gain diverse insights. Data from each research cycle guides curriculum development, ensuring ongoing refinement based on empirical evidence, as depicted in Figure 2.

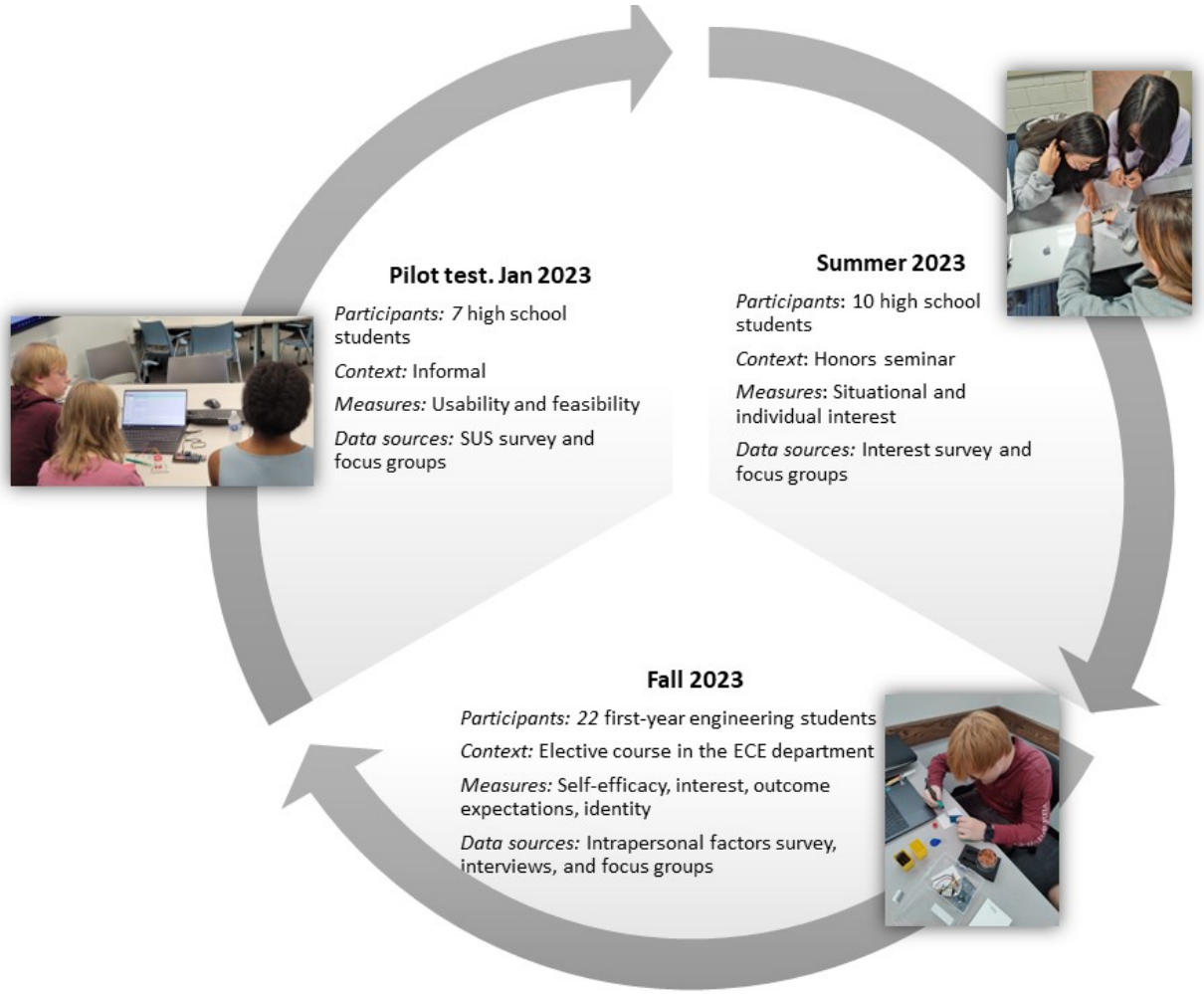

Figure 2. Cycles of implementation

Pilot test

Participants

Six girls and one boy from grades ten and eleven participated in usability and feasibility testing as part of an after-school activity.

Instructional approach

Our project aims to develop games and activities reinforcing computer hardware concepts. In this pilot, participants played the first two instructional games using an FPGA (Figure 3). The approach fostered both competition and collaboration among students.

Measures and data sources

After playing the games, students completed a Systems Usability Score SUS survey (Brooke, 1996) with additional open-ended questions. An observation protocol validated behavioral, cognitive, and emotional engagement, and a focus group gathered perceptions of the games.

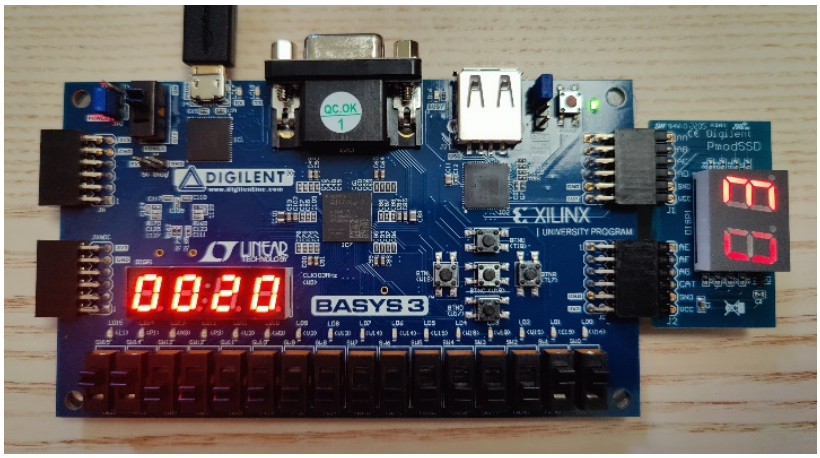

Figure 3. FPGA

Results

With an average SUS score of 61, falling below the typical threshold of 68, we analyzed the open-ended responses, observations, and focus group data. This analysis revealed several key insights to enhance the design of the curriculum's activities:

1. Reduce external components connected to the FPGA.
2. Fine-tune collaboration while maintaining competitiveness.
3. Integrate more real-life applications to enhance concept complexity.
4. Involve students in circuit design.

Summer program

Participants
We offered the curriculum in a summer honors seminar at a large R1 institution in the southeastern US. The seminar met twice a week for six weeks, with sessions lasting 1.5 hours. Ten high school seniors participated, with six granting consent, including two girls and four boys.

Instructional approach
The seminar's activities aimed to balance simulations, circuit design, FPGA-based applications, and collaboration to develop FPGA-based projects to address real-world challenges. Students also interacted with guest speakers acting as role models in hardware engineering.

Measures and data sources
Before and after the seminar, students completed Romine et al.'s (2014) Student Interest in Technology and Science (SITS) survey. Additionally, they participated in a focus group at the end of the seminar. The focus group protocol was designed to explore their perceptions of the activities and whether they sparked interest in hardware computing.

Results

Survey results revealed heightened individual interest following the six-week seminar. Additionally, focus group findings indicated a shift from initially sparked situational interest to a sustained level. These insights informed the following design considerations for the curriculum's activities:

1. Allow students to explore more advanced applications like Artificial Intelligence IoT (AIoT) and Edge AI.
2. Introduce students to hardware design, enabling them to manipulate both hardware and software for FPGA programming.
3. Increase the use of simulations to streamline the setup process for hardware boards.

Elective course

Participants

During the Fall semester of 2023, we implemented our curriculum as an undergraduate course at a large R1 institution in the southeastern US. Twenty-two first-year engineering students enrolled, with seventeen providing consent—four women and thirteen men. Students completed pre and post-surveys and engaged in focus groups and interviews.

Instructional approach

In this phase, we enhanced the curriculum by integrating sensor-based IoT boards (Figure 4). Students explored diverse sensors (motion, weather, heart rate, ultrasonic, light) to gather environmental data. They used machine learning (ML) algorithms to predict conditions, covering AIoT and EdgeAI topics, and participated in collaborative projects to devise real-world solutions.

Measures and data sources

Students completed a pre and post-survey on intrapersonal factors to gauge changes in self-efficacy, interest, outcome expectations, and identity. This survey was adapted from Neiderhauser and Perkmen (2008) Intrapersonal Technology Integration Scale (ITIS). Additionally, students participated in focus groups and interviews after the semester.

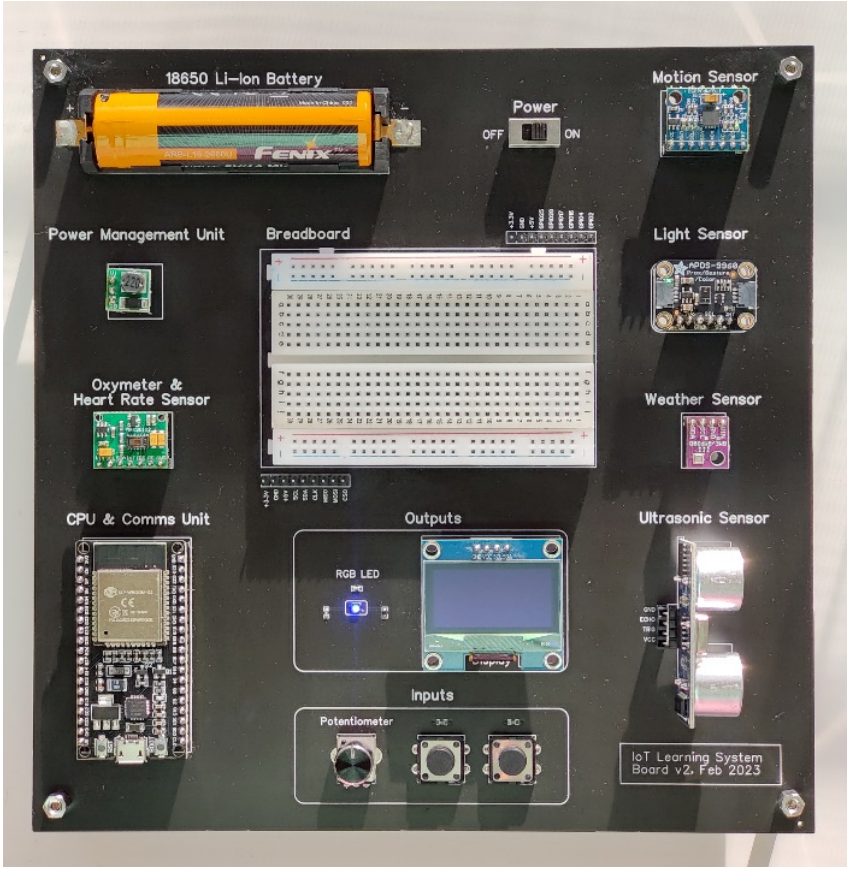

Figure 4. IoT learning board

Results

Findings from the survey indicated significant improvements in students' interest after the course ($t16 = 2.56$, $p < .02$), students' self-efficacy ($t16 = 3.97$, $p < .001$), students' engineering identity ($t16 = 4.78$, $p < .001$), and students' outcome expectations ($t16 = -2.27$, $p<.05$). Results are promising, indicating the curriculum promotes hardware engineering career intentions, aligning with our project's main goal. The qualitative analysis of the focus groups and interviews is ongoing, and the results will be discussed in the presentation.

Future implications

Data from Fall 2023 curriculum implementation underscores the importance of analyzing gender and racial differences. Targeted supports can then be developed to address the needs of underrepresented groups, promoting equity and diversity in hardware engineering. Furthermore, it is crucial to engage high school teachers in refining and testing the curriculum to ensure it meets diverse student needs and aligns with educational standards. Additionally, providing comprehensive implementation guides is essential for broad adoption and maximizing impact.