Active Switched-Inductor High-Gain Step-up DC-DC Converter with Reduced Voltage Stress

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***Abstract*—This paper introduces a high-gain step-up DC-DC converter with an active switched-inductor and a voltage multiplier cell. The proposed converter has a simple structure with the replacement of a diode in the switched-inductor cell with an active switch to reduce the voltage stress on power switches and improve efficiency. In addition, an inductor is used in the output side of the voltage multiplier cell to mitigate electromagnetic interference (EMI) issues and to reduce reverse recovery loss. A comprehensive comparison study with the conventional switched-inductor converter is also presented to confirm the effectiveness of the proposed converter. To verify its feasibility, a 200 W prototype of the proposed converter is built.**

Keywords—High step-up, DC-DC converter, Switched-capacitor, Single-switch, Renewable Energies

I. Introduction

Renewable sources will have a significant impact on the future of power generation. Compared to other renewable sources, solar photovoltaics have become one of the major trends due to their accessibility, modularity, and low cost [1]. The output voltage of a solar panel varies depending on changing environmental conditions. Therefore, DC–DC boost converters are required to provide constant DC bus voltage. Traditionally, conventional boost converters can increase the low solar panel voltage to the required high DC-bus voltage by controlling the duty cycle of the active switch. However, these converters cannot satisfy the voltage ratio requirement of the practical applications and need to work at a high-duty cycle to achieve a high voltage conversion, resulting in issues such as reduced efficiency, high voltage stress on power switching devices, and high reverse recovery loss. Therefore, high-gain boost DC-DC converters have been derived to overcome the limitations associated with the conventional boost converter [2]. When considering the isolation issue, high-gain step-up DC-DC converters can be divided into isolated and non-isolated structures. For the isolated structure, while the output voltage can be further boosted by the high-frequency transformers [3]. Such transformers can increase the converter cost and size. Likewise, the method with coupled-inductor also contains critical issues related to high voltage spikes on semiconductor devices caused by the leakage component of the coupled-inductor [4]. By contrast, a non-isolated structure is considered a potential solution for high efficiency and low cost of the converter system in distributed generation systems. Switched capacitor (SC) structures have become good candidates for their high-power density, extendibility, and high efficiency at low-power

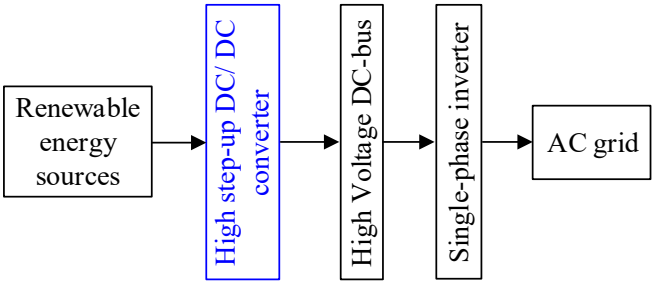


Fig. 1. Typical block diagram of renewable energy conversions.

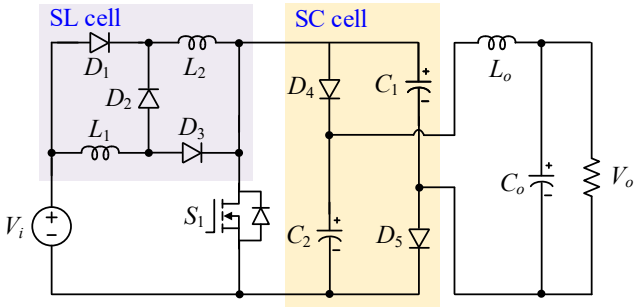


Fig. 2. Conventional SL DC-DC converter.

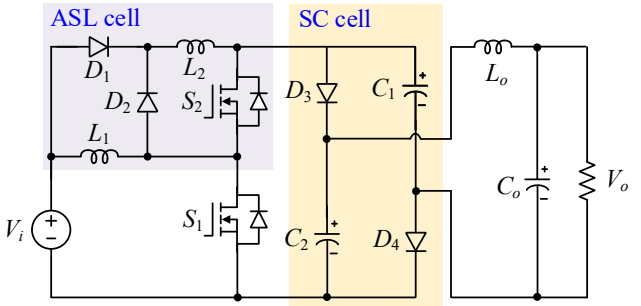


Fig. 3. Proposed ASL DC-DC converter.

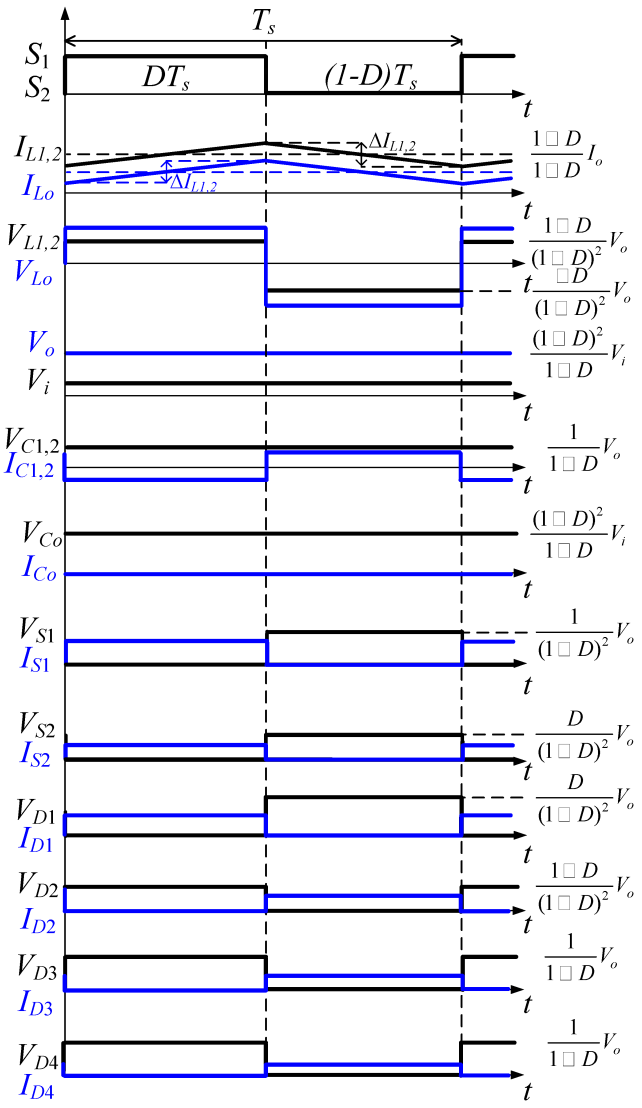


Fig. 4. Key waveforms of the proposed ASL DC-DC converter.

applications. In these structures, the voltage ratio is obtained by storing or restoring capacitors' energy in parallel or in series then discharging the charge to the load. Similarly, the switched-inductor (SL) structures also provide a high voltage ratio by charging inductors in parallel and discharging them in series. Some of the recent solutions of SL/SC structures and hybrid SL/SC structures were reported in [5]-[7].

In addition, converters like Buck, Ćuk, and Zeta use an inductor connected to the output side to provide continuous output currents. The concept of using an output inductor to replace the diode at the output side of the voltage multiplier in a high-gain boost DC-DC converter was discussed in [8]-[10]. The replacement of the output diode by an inductor can be considered as the output low-pass filter for high step-up DC-DC converters, which provides a continuous output current, reduces the output electrolytic capacitance, and improves the reliability of the power converter. However, this replacement reduces the voltage gain of the converters. So, the SL and SC structures can be added to these converters to improve the voltage gain. Fig. 1 presents the topology of the conventional SL DC-DC converter, in which the output diode is replaced with an inductor. The SL circuit is applied on the input side to

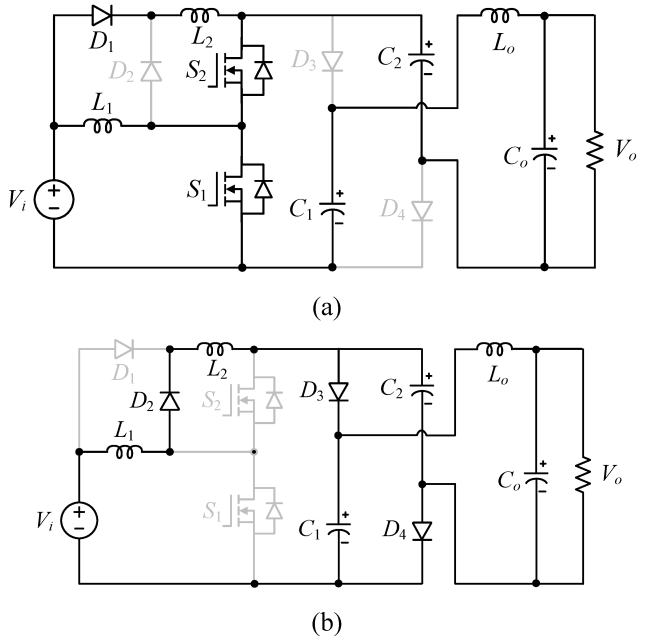


Fig. 5. Operation modes of the proposed ASL converter. (a) Mode 1, (b) Mode 2.

improve the voltage ratio compared with the conventional boost converter. Moreover, a voltage multiplier circuit is used on the output side to provide twice the voltage ratio and reduces voltage stress of the component. However, the voltage stress of switching devices is still high. Hence, the derivation of the SL circuit on the input side is proposed in this paper. The diode in the SL circuit is replaced by an active power switch, and the total number of components is kept the same. The proposed active-switched inductor (ASL) converter reduces the voltage rating of switching devices and offers high step-up capability.

II. Proposed ASL DC-DC Converter

1. *Operating Principle*

The proposed ASL converter is derived from the conventional SL converter by replacing the diode in the SL cell with an active switch, as shown in Fig. 2. On the output side, the voltage multiplier cell with an output inductor is employed. The total number of components in the proposed ASL converter equals the conventional SL converter. In the pulse-width modulation (PWM) control method, switches S1 and S2 are turned on and off simultaneously. The proposed ASL converter is considered in the continuous conduction mode to simplify the circuit analyses.

Mode 1: In this mode, the two switches *S*1 and *S*2 are turned on. During this mode, only diode *D*1 is turned on, and the other three diodes *D*2, *D*3, and *D*4 are turned off. The analysis circuit of the proposed ASL converter is described in Fig. 5(a). The corresponding equations are expressed as follows

$$\begin{cases} v_{L1(\text{Mode 1})} = v_{L2(\text{Mode 1})} = V_i \\ V_{C1} + V_{C2} = v_{Lo(\text{Mode 1})} + V_o \\ I_{Lo} = I_o \\ i_{C1(\text{Mode 1})} = i_{C2(\text{Mode 1})} = - I_o, \end{cases} \tag{1}$$

Mode 2: In this mode, the two switches S1 and S2 are turned off. In this mode, diodes D_2, D_3, and D_4 are turned on while diode D_1 is turned off. The analysis circuit of the proposed ASL converter is described in Fig. 5(b). The relevant equations are expressed as follows

$$\begin{cases} v_{L1(\text{Mode 2})} + v_{L2(\text{Mode 2})} + V_{C1} = V_i \\ v_{Lo(\text{Mode 2})} + v_o - V_{C1} = 0 \\ V_{C1} = V_{C2} \\ I_{L1} = I_{L2} = i_{C1(\text{Mode 2})} + i_{C2(\text{Mode 2})} + I_{Lo}, \end{cases} \tag{2}$$

Using the average value equation of the inductor voltage

$$\langle v_{L1} \rangle_{T_S} = \langle v_{L2} \rangle_{T_S} = 0, \tag{3}$$

From (1) to (3), the voltage gain of the proposed ASL converter can be calculated as

$$\frac{V_o}{V_i} = \frac{(1+D)^2}{1-D} V_i, \tag{4}$$

Where D is the duty cycle.

Besides that, the voltage stress on capacitors C_1, C_2 and inductors L_1, L_2 and L_o can be derived as

$$\begin{cases} V_{C1} = V_{C2} = \dfrac{1}{1+D} V_o \\ V_{L1(\text{Mode 1})} = V_{L2(\text{Mode 1})} = \dfrac{1-D}{(1+D)^2} V_o \\ V_{L1(\text{Mode 2})} = V_{L2(\text{Mode 2})} = \dfrac{-D}{(1+D)^2} V_o \\ V_{Lo(\text{Mode 1})} = \dfrac{1-D}{1+D} V_o \\ V_{Lo(\text{Mode 2})} = \dfrac{-D}{1+D} V_o, \end{cases} \tag{5}$$

Using the average value equation of the capacitor, we got the equation as follows

$$\langle i_{C1} \rangle_{T_S} = \langle i_{C2} \rangle_{T_S} = \langle i_{Co} \rangle_{T_S} = 0, \tag{6}$$

From equations (1), (2), and (6), the current through capacitors, and inductors can be calculated as follows

$$\begin{cases} I_{C1(\text{Mode 1})} = I_{C2(\text{Mode 1})} = -I_o \\ I_{C1(\text{Mode 2})} = I_{C2(\text{Mode 2})} = \dfrac{D}{1-D} I_o \\ I_{Lo} = I_o \\ I_{L1} = I_{L2} = \dfrac{1+D}{1-D} I_o, \end{cases} \tag{7}$$

III. Design Guideline

1. *Inductance values of* L_1, L_2, and L_o

The inductance values in the proposed ASL converter are selected according to their current ripple. The equations can be shown as

TABLE 1
COMPARISON OF CONVENTIONAL SL AND PROPOSED ASL CONVERTERS

Converter	Conventional SL converter	Proposed ASL converter
Voltage gain	$\frac{(1+D)^2}{1-D}$	$\frac{(1+D)^2}{1-D}$
Total device	12	12
Normalized switching device voltage	$\frac{4+4D}{1-D} V_i$	$\frac{4+3D}{1-D} V_i$
Common-ground feature	Yes	Yes
Cost (US$)	59.29	56.12
Measured efficiency	93.9 %	94.8 %

TABLE 2. SIMULATION PARAMETERS

Parameter	Values
V_i	40 V
V_o	200 V
P_o	200 W
f_s	20 kHz
Inductors (L_1, L_2, L_o)	500 µH
Capacitors (C_1, C_2, C_o)	200 µF

TABLE 3. SIMULATED COMPARISON

Converter	Conventional SL converter	Proposed ASL converter
Voltage gain	5	5
Total device	12	12
Semiconductors voltage stress	518.1 V	477.4 V
Semiconductors current stress	22.4 A	23.2 A
Total semiconductor device rating (TSDR)	11.605 kVA	11.075 kVA

$$\begin{cases} v_{L1} = L_1 \dfrac{di_{L1}}{dt} \\ v_{L2} = L_2 \dfrac{di_{L2}}{dt} \\ v_{Lo} = L_o \dfrac{di_{Lo}}{dt}, \end{cases} \tag{8}$$

The equations (8) can be derived

$$\begin{aligned} V_{L1} &= L_1 \frac{\mathrm{D}i_{L1}}{\mathrm{D}t} \\ V_{L2} &= L_2 \frac{\mathrm{D}i_{L2}}{\mathrm{D}t} \\ V_{Lo} &= L_o \frac{\mathrm{D}i_{Lo}}{\mathrm{D}t}, \end{aligned} \tag{9}$$

The inductor current ripple can be calculated as

$$\begin{aligned} \mathrm{V}i_{L1} = \mathrm{V}i_{L2} &= i\%.I_L = \frac{(1-D)V_o}{(1+D)^2} DT_s \\ \mathrm{V}i_{Lo} &= i\%.I_{Lo} = \frac{(1-D)V_o}{1+D} DT_s, \end{aligned} \tag{10}$$

Using equations (7) and (10), the inductances of L_1 and L_2 are found as

$$\begin{aligned} L_1 = L_2 &= \frac{RD(1-D)^2}{i\% f_s (1+D)^3} \\ L_o &= \frac{RD(1-D)}{i\% f_s (1+D)}, \end{aligned} \tag{11}$$

where $i\%$ is the percent of current ripple on inductors L_1, L_2 and L_o.

2. *Capacitance Values of C_1, C_2 and C_o*

Similar to inductance selection, the capacitance values are also selected based on their current ripple. The equation can be expressed as

$$\begin{aligned} I_{C1} &= C_1 \frac{\mathrm{D}v_{C1}}{\mathrm{D}t} \\ I_{C2} &= C_2 \frac{\mathrm{D}v_{C2}}{\mathrm{D}t} \\ \mathrm{D}Q_{Co} &= C_o \mathrm{D}v_{Co} = \frac{\mathrm{D}i_{Lo}}{8f_s}, \end{aligned} \tag{12}$$

The capacitors are designed by the ripple voltage, charging current, and rated voltages. Utilizing equations (7), (10) and (12), the below equation is obtained

$$\begin{aligned} C_1 \frac{\mathrm{D}V_{C1}}{DT_s} &= I_o \\ C_2 \frac{\mathrm{D}V_{C2}}{DT_s} &= I_o \\ C_o \mathrm{D}v_{Co} &= \frac{\mathrm{D}i_{Lo}}{8f_s}, \end{aligned} \tag{13}$$

The capacitances of capacitors C_1, C_2, and C_o, can be derived as

$$\begin{aligned} C_1 = C_2 &= \frac{D(1+D)}{c\% R f_s} \\ C_o &= \frac{D(1-D)}{8c\% f_s^2 (1+D)^2}, \end{aligned} \tag{14}$$

where c% represents the percentage of voltage ripple of C_1, C_2, and C_o.

3. *Semiconductor Devices Selection*

Semiconductor devices in this topology are chosen by their current and voltage rating. From equation (5) and referring to Fig. 5, the voltage stress of all semiconductor devices can be written as

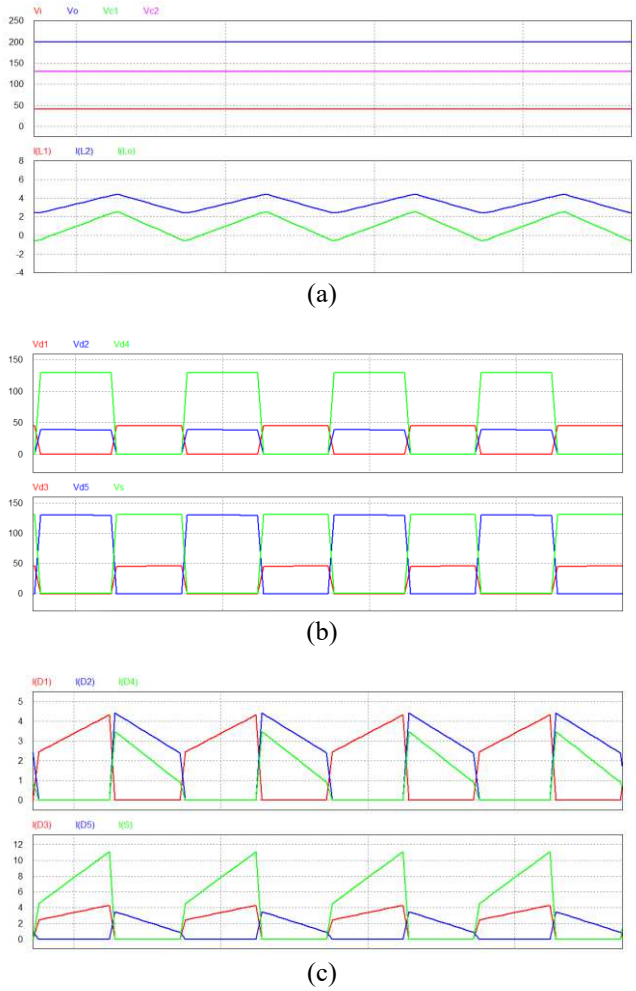
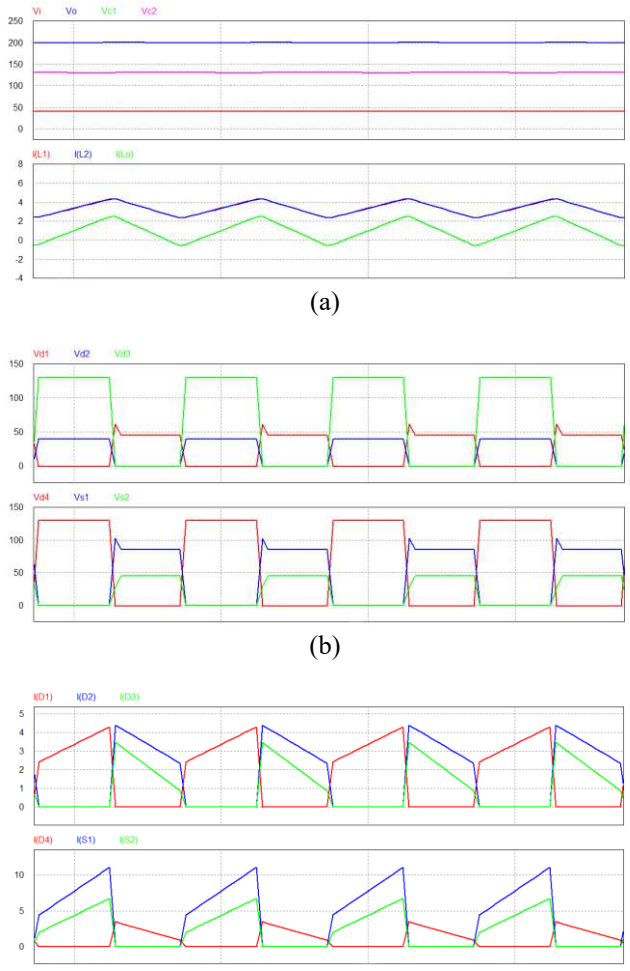


Fig. 6. Simulation results of the conventional SL converter. (a) Voltage gain, voltage stress on capacitors and inductors current (b) Voltage stress on diode D_1, D_2, D_3, D_4, D_5 and switch S (c) Current stress through diode D_1, D_2, D_3, D_4, D_5 and switch S.

$$\begin{aligned} V_{S1} &= \frac{1}{(1+D)^2} V_o \\ V_{S2} &= \frac{D}{(1+D)^2} V_o \\ V_{D1} &= \frac{D}{(1+D)^2} V_o \\ V_{D2} &= \frac{1-D}{(1+D)^2} V_o \\ V_{D3} = V_{D4} &= \frac{1}{1+D} V_o, \end{aligned} \tag{15}$$

From the (7) equation, all semiconductors current can be written by the following expression

$$\begin{aligned} I_{S1} &= \frac{3+D}{1-D} I_o \\ I_{S2} &= \frac{2}{1-D} I_o \\ I_{D1} = I_{D2} &= \frac{1+D}{1-D} I_o \\ I_{D3} = I_{D4} &= \frac{1}{1-D} I_o, \end{aligned} \tag{16}$$



(a) (b) (c)

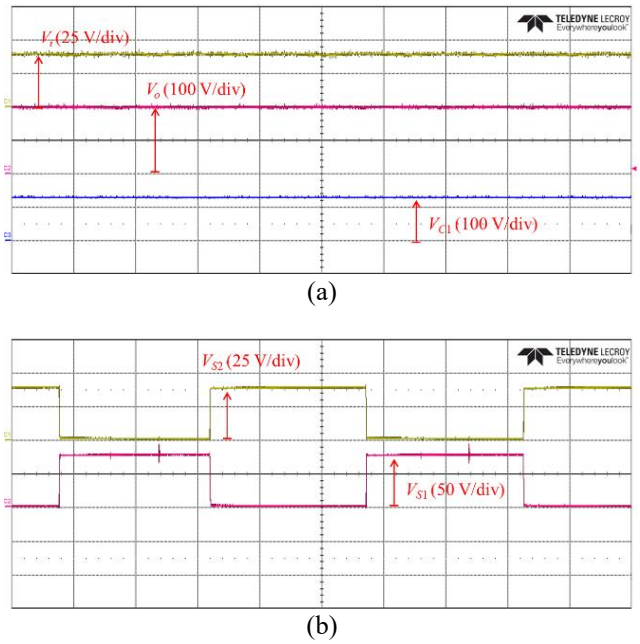
Fig. 7. Simulation results of the proposed ASL converter. (a) Voltage gain, voltage stress on capacitors and inductors current (b) Voltage stress on diode D_1, D_2, D_3, D_4, switch S_1 and S_2 (c) Current stress through diode D_1, D_2, D_3, D_4, switch S_1 and S_2.

From equation (16) and referring to Fig. 5, the current RMS of all semiconductors can be calculated as follows

$$\begin{aligned} I_{S1,RMS} &= \frac{(3+D)\sqrt{D}}{1-D} I_o \\ I_{S2,RMS} &= \frac{2\sqrt{D}}{1-D} I_o \\ I_{D1,RMS} &= \frac{(1+D)\sqrt{D}}{1-D} I_o \\ I_{D2,RMS} &= \frac{1+D}{\sqrt{1-D}} I_o \\ I_{D3,RMS} &= I_{D4,RMS} = \frac{1}{\sqrt{1-D}} I_o, \end{aligned} \tag{17}$$

IV. Comparative Study

To present the improvement of the proposed ASL converter with the conventional SL converter, a comparison is shown in Table 1. The conventional SL and the proposed ASL converters have the same number of components. The total voltage stress of the proposed ASL converter is lower than that of the conventional SL converter. In addition,



(a) (b)

Fig. 8. Experimental results of the proposed ASL converter. (a) Input voltage, capacitor voltage, output voltage. (b) Switches S_1 and S_2 waveforms.

compared with the conventional SL converter, the measured efficiency of the proposed ASL converter is improved and its cost is reduced. This is because the voltage rating of semiconductor devices in the proposed ASL converter is less than that of the conventional SL converter.

V. Simulation And Experimental Results

To verify the performance of the proposed ASL converter, a simulation is built in PSIM software. Table 2 shows that the simulation parameters are identical for both the conventional SL and proposed ASL converters. The 40 V input voltage and the 0.6 duty cycle generate a 200 V output voltage. The 200 Ω resistive load is connected to the output side to provide 200 W output power. Figs. 6-7 shows the simulation of the output voltage, current through inductors L_1 and L_2, voltage through capacitors C_1 and C_2, current through all semiconductors, and voltage stresses of the conventional SL converter and the proposed ASL converter. It is clear from the simulation results that the capacitor voltages for C_1 and C_2 are 99.8 V and the output capacitor V_{Co} equals the output voltage around 200 V. The simulated data in Table 3 compares the conventional SL and proposed ASL converters. The proposed ASL converter is more advantageous than the conventional SL converter because the ASL converter demonstrates a lower semiconductor voltage. Also, because of the proposed ASL converter's lower total semiconductor device rating, it has a 0.9% increase in efficiency compared to the conventional SL converter.

A 200 W prototype was built to verify the performance of the proposed ASL converter. The switches S1 and S2 were controlled with a 20 kHz switching frequency. We also selected two 0.5 mH SL and 0.1 mH output. The 40V input voltage and the 0.6 duty cycle of S_1 and S_2 produces an output voltage of 200 V. Fig. 8(a) shows the experimental results of the input voltage, capacitor voltage, and output. Fig. 8(b) shows the voltage stresses of switches S_1 and S_2. The voltage

stress of switch S_1 is significantly reduced compared with that of the conventional SL converter.

VI. Conclusion and Future Works

This paper proposes a new ASL converter based on the conventional SL converter. The proposed ASL converter reduces EMI and reverse recovery issues, as well as the required output capacitance. Compared with the conventional SL converter, the proposed ASL converter requires a lower total semiconductor voltage rating. Thus, the efficiency and cost of the proposed ASL converter can be improved. Additionally, the theory and experimental verification have been provided. For future work, the power density of the proposed ASL converter can be increased by applying a coupled inductor for the SL inductors and an output inductor.

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References

[1] M. Forouzesh, Y. P. Siwakoti, S. A. Gorji, F. Blaabjerg, and B. Lehman, ‘‘Step-up DC–DC converters: A comprehensive review of voltage-boosting techniques, topologies, and applications,’’ *IEEE Trans. Power Electron*., vol. 32, no. 12, pp. 9143–9178, Dec. 2017.

[2] M. K. Nguyen, T. D. Duong, and L. C. Lim, “Switched-capacitor-based dual-switch high-bost dc-dc converter,” *IEEE Trans. Power Electron*., vol. 33, no. 5, pp. 4181–4189, May 2018.

[3] N. Q. Trong, H.-J. Chiu, Y.-K. Lo, C.-Y. Lin, and M. M. Alam, “Modified current-fed full-bridge isolated power factor correction converter with low-voltage stress,” *IET Power Electron*., vol. 7, no. 4, pp. 861–867, Apr. 2013.

[4] P. Mohseni, S. H. Hosseini, M. Sabahi, and T. Jalilzadeh, “A new high step-up multi-input multi-output DC–DC converter,” *IEEE Trans. Ind. Electron*., vol. 66, no. 7, pp. 5197–5208, Jul. 2019.

[5] T. D. Duong, M. K. Nguyen, Y. C. Lim, J. H. Choi, D. M. Vilathgamuwa, "An active-clamped current-fed half-bridge DC-DC converter with three switches," *in Proc. 2018 International Power Electronics Conference (IPEC-Niigata 2018-ECCE Asia)*, Niigata, Japan, May 2018, pp. 982–986.

[6] Y. Zhao, W. Li, X. He, “Single-phase improved active clamp coupled-inductor based converter with extended voltage doubler cell,” *IEEE Trans. Power Electron*., vol. 27, no. 6, pp. 2869–2878, Jun. 2012.

[7] A. Alzahrani, M. Ferdowsi, and P. Shamsi, “A family of scalable non-isolated interleaved DC-DC boost converters with voltage multiplier cells,” *IEEE Access*, vol. 7, pp. 11707–11721, 2019.

[8] Y. Tang, T. Wang, and D. Fu, “Multicell switched-inductor/switched capacitor combined active-network converters,” *IEEE Trans. Power Electron*., vol. 30, no. 4, pp. 2063–2072, Apr. 2015.

[9] B. Faridpak, M. Bayat, M. Nasiri, R. Samanbakhsh, and M. Farrokhifar, “Improved hybrid switched inductor/switched capacitor DC–DC converters,” *IEEE Trans. Power Electron*., vol. 36, no. 3, pp. 3053–3062, Mar. 2021.

[10] Y. Zeng, H. Li, W. Wang, B. Zang, and T. Q. Zheng, ‘‘High-efficient high voltage-gain capacitor clamped DC–DC converters and their construction method,’’ *IEEE Trans. Ind. Electron*., vol. 68, no. 5, pp. 3992–4003, May 2021.

[11] G. G. Kumar, K. Sundaramoorthy, V. Karthikeyan, and E. Babaei, “Switched capacitor–inductor network based ultra-gain DC–DC converter using single switch,” *IEEE Trans. Ind. Electron*., vol. 67, no. 12, pp. 10274–10283, Dec. 2020.

[12] A. Kumar, Y. Wang, X. Pan, M. Raghuram, S. K. Singh, X. Xiong, A. K. Tripathi, “Switched-LC based high gain converter with lower component count,” *IEEE Trans. Ind. Appl.,* vol. 56, no. 3, pp. 2816–2827, May/Jun. 2020.

[13] B. Axelrod, Y. Berkovich, and A. Ioinovici, “Switched capacitor/switched-inductor structures for getting transformerless hybrid DC–DC PWM converters,” *IEEE Trans. Circuits Syst. I: Regular Papers*, vol. 55, no. 2, pp. 687–696, Mar. 2008.

[14] A. M. S. S. Andrade and M. L. d. S. Martins, “Study and Analysis of Pulsating and Non pulsating Input and Output Current of Ultrahigh Voltage Gain Hybrid DC–DC Converters,” *IEEE Trans. on Ind. Electron.*, vol. 67, no. 5, pp. 3776–3787, 2020.

[15] S. Habibi, R. Rahimi, M. Ferdowsi, and P. Shamsi, ‘‘A General Method for Analyzing Single-Switch Step-Up DC-DC Converters with Switched Capacitor Cells and an Output Inductor,’’ *IEEE J. Emerg. Sel. Topics Ind. Electron*., *Early Access*, 2023.