A 22nm CMOS 15-25GHz Dual-Differential Driver for RF Silicon Photonic Front-End

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***Abstract*— An RF photonic front-end using dual-differential driving scheme is reported with a 22nm CMOS FD-SOI driver co-integrated with a silicon traveling-wave Mach-Zehnder modulator. A compact design of power splitter and output routing network are implemented on dual-differential driver. An LC input matching network co-designed with bond wire inductance is implemented on a photonic chip to complete the output matching network. The proposed driver is verified with S-parameter and two-tone measurements, achieving 15-25GHz bandwidth with peak 3dBm IIP3 and consumes 448mW. The link performance is demonstrated 12.1% EVM of 16-QAM modulation with 2Gbd at 20GHz carrier frequency.**

***Keywords*— Mach-Zehnder Modulator, Microwave Photonics, Radio-over-Fiber System, Silicon Photonics**

I. Introduction

Radio-over-Fiber (RoF) links represent a promising solution for modern wireless communication systems by converting RF signals into the optical domain for efficient transmission through a fiber network [1]. This approach simplifies the deployment of RF receivers and central units that perform demanding base-band signal processing. The Traveling-Wave Mach-Zehnder modulator (TW-MZM) is a strong candidate in such a system because of its high frequency and high speed performance. To improve the minimum detectable signal level, an electrical driver is often adopted as the front-end circuit of the receiver. The front-end circuit must exhibit high linearity, low noise, and considerable gain to offset the inherent loss of high-speed MZM. The advanced driving scheme can benefit the system at the cost of integration complexity. A differential driving architecture, as shown in Fig. 1, is preferred over conventional single-drive configurations due to its inherent ability to eliminate second-order harmonic distortion. The dual-differential driving scheme, in particular, offers advantages by effectively doubling the modulating drive voltage without impacting the linearity of the driver [2]. This configuration theoretically increases an additional linear RF gain of 6dB in the system. Furthermore, the dual-differential driver design can be derived naturally from the architecture of a two-way power amplifier, while avoiding the need for a lossy power combiner at the output stage.

To the best of the authors' knowledge, this work reports the first wideband silicon-based RoF front-end employing a dual-differential driving configuration. The proposed front-end integrates a 22nm CMOS fully depleted silicon-on-insulator (FDSOI) driver with a silicon photonic TW-MZM fabricated in a 220nm SOI technology. The dedicated TW-MZM is designed to support the bandwidth and present a wideband impedance

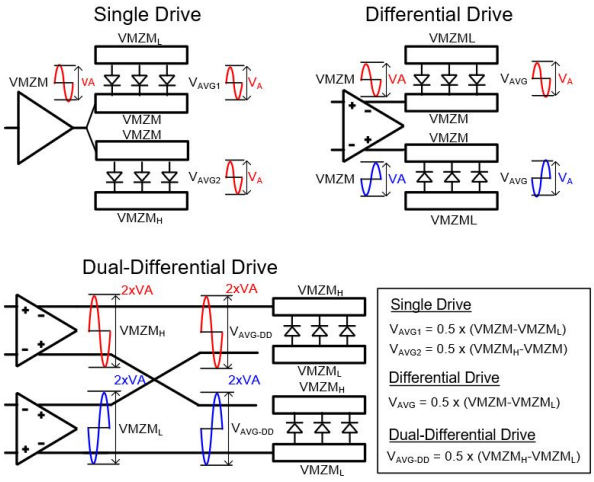
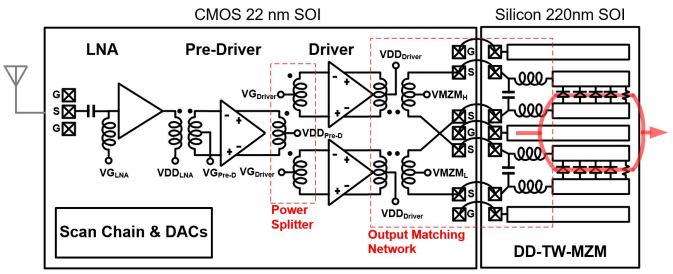


Fig. 1. Different driving topology of modulator.

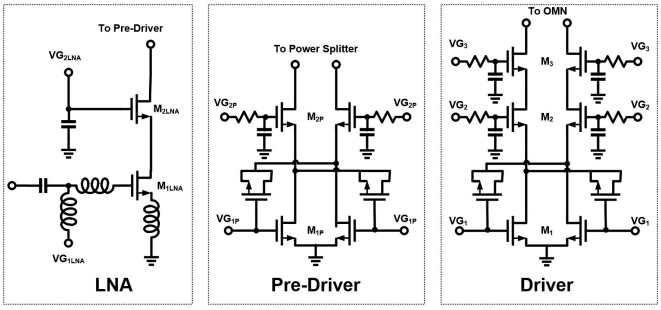
to the driver. An impedance matching circuit is implemented directly on the silicon photonic integrated circuit (Si-PIC) and is co-designed with the bondwires used at the interface between the two chips. The proposed driver is measured with 20dB gain for each arm with peak 3dBm of input 3rd order intercept point (IIP3) and consumes 448mW. The input return loss is below 9dB in the operating frequency range. The system operates in a wide frequency range of 15–25GHz and demonstrates an EVM of 12.1% for 16-QAM modulation at 20GHz carrier frequency.

II. Dual-Differential Driver Architecture

The block diagram of the proposed dual-differential MZM driver and traveling-wave Mach-Zehnder modulator (TW-MZM) is shown in Fig. 2(a). The active driver design is derived from [3]. To realize the dual-differential driving scheme, a compact power splitter and balanced output routing are incorporated. The received wireless signal is initially amplified by an input low-noise amplifier (LNA) and subsequently converted into a differential signal by a balun. This differential signal is then further amplified by a pre-driver stage before being split into two paths by a power splitter. Finally, three-stack FET output drivers modulate each arm of the TW-MZM in the dual-differential configuration. Fig. 2(b) depicts the transistor-level schematic of the LNA, pre-driver and driver circuits, respectively. The LNA is a single-stage cascode structure for its high isolation and high



(a)



(b)

Fig. 2. (a) Dual-differential receiver font-end architecture and (b) schematic of dual-differential driver.

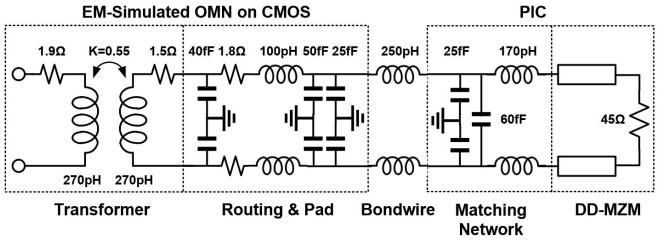


Fig. 3. Completed equivalent circuit of the output matching network.

gain performance. The following balun also serve as the inter-stage matching network and provide supply VDD to the LNA. Pre-driver and driver utilize stack-FET technique to overcome low supply voltage constraint in advanced CMOS technology. The input impedance of the electrode of dual-differential MZM needs to be designed twice higher compare to differential version, while still matching the group velocity to optical signal.

As shown in Fig. 2, a vertically-coupled power splitter is adopted to divide the signal between the two arms of the TW-MZM [4]. Consistent with other inter-stage matching components, this fully-differential power splitter leverages on the magnetically-coupled resonator (MCR) technique, incorporating parallel capacitors to achieve a wideband response [5]. The DC gate bias voltage of driver and supply voltage of pre-driver are connected at the center tap of the transformers. A cross connection is necessary at the one arm of the output to accomplish the correct polarity of the dual-differential driving scheme. An output matching network (OMN) is designed to ensure optimal loading impedance for

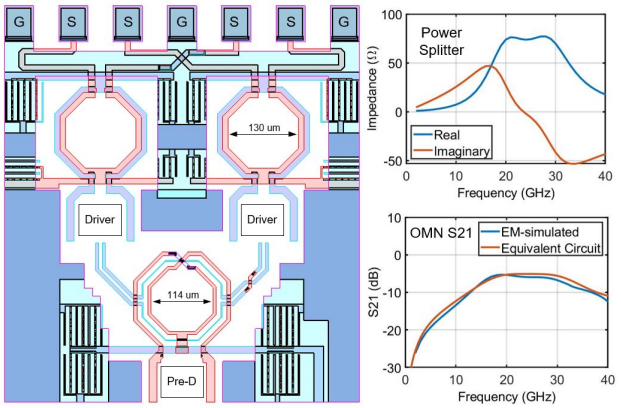
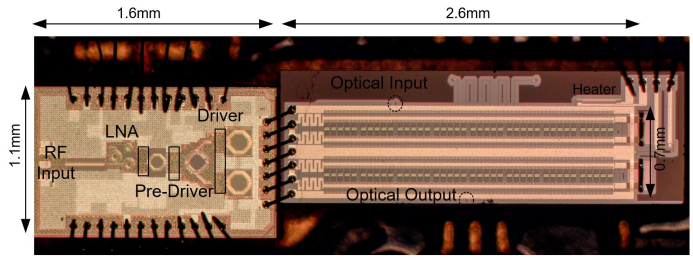


Fig. 4. Layout and EM-simulation of power splitter and output matching network to implement dual-differential drive.

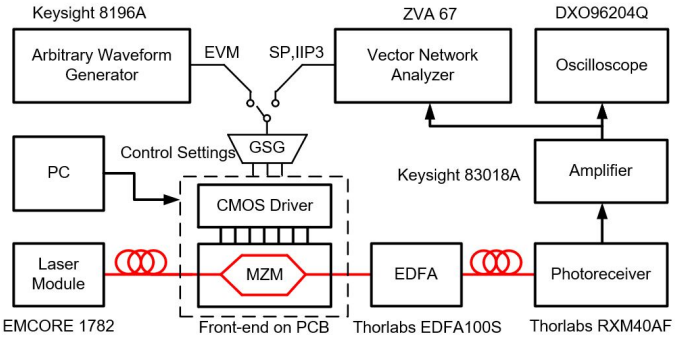
the driver circuits while maintaining a low-loss transition across the entire operating frequency range for both drivers. The equivalent circuit of the OMN is described in Fig. 3 which involves, pad capacitance, bond-wire and dedicated matching circuit on Si-PIC. The output transformer is modeled by inductor with series resistor for finite quality factor and coupling coefficient k labeled in the figure. A π-model is adopted to model the routing at the output. Pad parasitic capacitor and bondwire are also included in the OMN. A simple LC matching network is implemented using two metal layers on the PIC to build 170pH inductors and 60fF capacitor. Lastly, characteristic impedance of electrode of TW-MZM and termination are added to complete the equivalent circuit. The layout of the power splitter and the OMN on the CMOS chip is illustrated in Fig. 4. To avoid gain penalty, it is critical to maintain phase matching at cross-routing at the output. DC biasing is also carefully implemented, with the MZM reversed-bias voltage provided via the center tap of the passive transformer layout to prevent high-voltage breakdown in the 22nm CMOS devices. A huge ground shielding is implemented using top aluminum layer to avoid coupling and provide a low-resistance ground. Fig. 4 shows the electromagnetic (EM) simulation results, including the input impedance of the power splitter and the S21 of the OMN. The compact power splitter and output matching network combined with MCR technique can provide wideband frequency response and agree to the equivalent circuit simulation.

III. Experimental Results

Fig. 5(a) presents the micrograph of the co-integrated CMOS driver and dual-differential traveling-wave Mach-Zehnder modulator (DD-TW-MZM) on Si-PIC. The output of the CMOS driver is interfaced with the input of DD-TW-MZM using bond-wires configured in GSSGSSG. To minimize bond-wire inductance, both the CMOS and Si-PIC chips are designed with approximately the same height and are mounted in close proximity on an FR-4 PCB. The DD-TW-MZM on Si-PIC is using slow-wave transmission line design for the electrode with 45Ω on-chip termination resistor.



(a)



(b)

Fig. 5. Proposed RF photonic front-end (a) micrograph and (b) measurement setup.

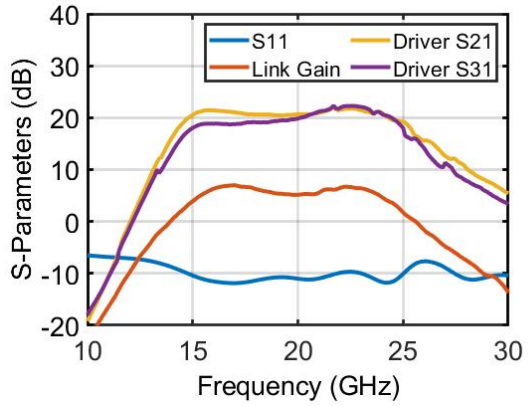
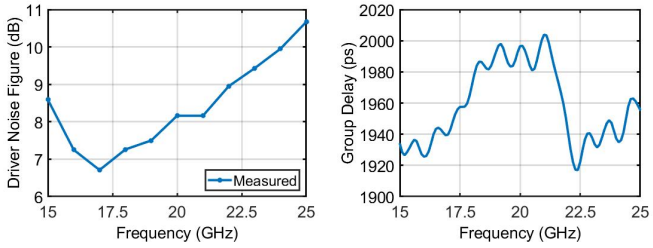


Fig. 6. Measured RF silicon photonic front-end frequency response.

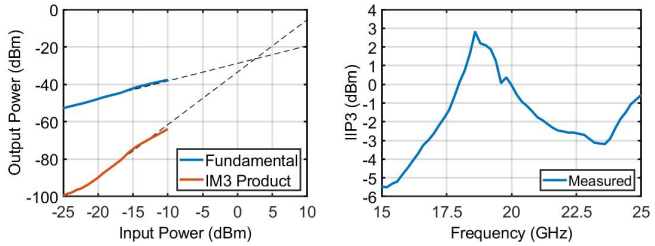


(a) (b)

Fig. 7. Measured driver (a) noise figure and (b) group delay.

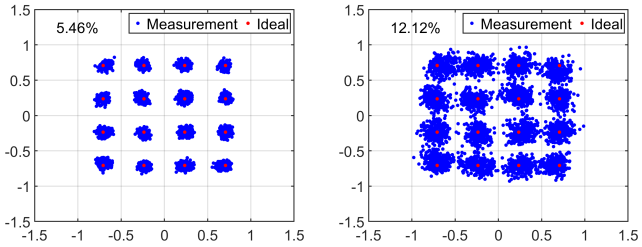
A phase recovery loop is implemented on the waveguide to match the velocity of electrical signal. Grating couplers each with 8dB loss are implemented to receive the CW-laser and output modulated optical signal for the prototype testing. This design is simulated to achieve 28GHz 3-dB bandwidth and $V\pi$, DC of 9.6V. The experimental measurement setup for the link is shown in Fig. 5(b). A high-power continuous-wave laser source (EMCORE 1782) is coupled to the TW-MZM via a grating coupler. The modulated optical output signal is then fed into a photoreceiver module (Thorlabs RXM40AF) followed by a broadband amplifier (Keysight 83050A). A vector network analyzer (Rohde & Schwarz ZVA67) is employed to characterize the link performance, including the frequency response and two-tone measurement.

The standalone driver measurement is performed with



(a) (b)

Fig. 8. Measured (a) input RF power sweep at 20GHz and (b) IIP3 over frequency of driver design.



(a) (b)

Fig. 9. Measured EVM with (a) 100MBd and (b) 2GBd 16-QAM signal at 20GHz carrier frequency.

Table 1. Performance Comparison

Reference	[6]	[7]	[8]	[3]	This Work
Frequency (GHz)	2-30	0.5-20	20-35	16-32	15-25
Process	LiNbO3	Si-SiGe	CMOS	CMOS	CMOS
P_{DC} (mW)	N/A	1700	180	209	448
Modulation Voltage (Vpp)	N/A	2	2.5	2.5	5
IIP3 (dBm)	6.2	22	4.8	1	3
NF (dB)	N/A	14-20*	22	38.1$^{\triangle}$	35.1$^{\triangle}$
NF (dB·Hz$^{2/3}$)	85-111	109-120*	99	86-89$^{\triangle}$	85-92$^{\triangle}$

* Edge Coupler
$^{\triangle}$ Grating Coupler

on-chip 4-side probing. An GSG and customized GSSGSSG probe are used as input and output. Two 12-pin DC probe are used for the DC supply and sending digital controlling bits. Fig. 6 illustrates the frequency response of the driver and the RoF link, demonstrating an operational bandwidth of 15–25GHz with return loss (S11) better than -9dB across the band. The link gain (S21) achieves a maximum of 6dB excluding the losses introduced by the grating couplers. Compare to driver bandwidth, overall link 3-dB bandwidth is reduced to 15-24.3GHz. The noise figure measurement is shown in Fig. 7(a) ranging from 6.5dB to 11dB. Since it is only one-stage LNA design with following high power driver, the noise performance is not comparable to the state-of-the-art. The group delay of the link is depicted in the Fig. 7(b). The maximum variation is below 85ps in the targeting frequency. To evaluate linearity, two-tone measurements are conducted, as shown in Fig. 8. Power sweep of the two-tone measurement at 20GHz are shown in the Fig. 8(a), showing approximate 2dBm of input third-order intercept point (IIP3) by extrapolation. Similar procedure is carried out through all the frequency, the IIP3 performance over the frequency is plotted in Fig. 8(b). The IIP3 of the driver is observed to range from -6dBm to 3dBm over the operational bandwidth. The error vector magnitude (EVM) measurement is done by using arbitrary waveform generator (Keysight M8196A) and high-speed oscilliscope (DSOX96204Q). As shown in Fig. 9, an EVM of 5.5% and 12.1% is measured for 100MBd and 2GBd 16-QAM at 20GHz carrier frequency which validate the operation of the RoF link. The performance is mainly limited by the signal-to-noise ratio (SNR) caused by the significant optical loss of the grating couplers, even with EDFA compensating the signal power afterward. Either increase the optical power or using more advanced edge coupler type could improve the EVM performance. The performance is compared with other works in Table. I. dual-differential driving scheme double the modulation depth while keeping the similar chip area which will benefit the SNR performance.

IV. Conclusion

This work presents an integrated RoF receiver front-end leveraging an advanced dual-differential driving scheme to achieve a 5dB improvement in overall link gain compared to conventional differential driving schemes. Compact power splitter and output matching network are implemented to complete the driving scheme. A stack-FET driver scheme along with MCR technique are applied in the driver design to improve the linearity and wideband performance. The interface between the CMOS chip and Si-PIC is co-designed with bond-wire inductance and an LC matching network on PIC to optimize impedance matching. Measurement results show the driver achieves 15–25GHz bandwidth with a peak IIP3 of 3dBm and consumes 448mW. The RoF link is validated with 16-QAM EVM measurement at 20GHz carrier frequency, 12.1% EVM can be achieved with 2GBd with two lossy grating couplers on the silicon DD-TW-MZM.

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