High-Speed CMOS Silicon Photonic PAM4 Transceiver Front-End Circuits

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***Abstract*—Growing interconnect bandwidth demand in large datacenters requires energy-efficient optical transceivers that operate with four-level pulse amplitude modulation (PAM4) to enable high per-wavelength data rates. Further increases in bandwidth density is possible by leveraging wavelength-division multiplexing (WDM), which optical link architectures based on silicon photonic microring modulators (MRMs) and drop filters inherently enable. This paper presents high-speed PAM4 transmitter and receiver front-ends implemented in a 28nm CMOS process that are co-designed with these silicon photonic optical devices to enable energy-efficient operation. The transmitter utilizes an optical digital-to-analog converter (DAC) approach with two PAM2 AC-coupled pulsed-cascode high-swing voltage-mode output stages to drive the MRM MSB/LSB segments. A 3.42V_{ppd} output swing is achieved when operating at 80Gb/s PAM4 with an energy efficiency of 3.66pJ/bit. The receiver front-end interfaces with a silicon-germanium avalanche photodiode (APD) and utilizes a low-bandwidth input transimpedance amplifier followed by continuous-time linear equalizer and variable-gain amplifier stages. Biasing the APD to realize a gain of 2 allows for -7dBm optical modulation amplitude (OMA) sensitivity at 56Gb/s PAM4 with a BER=10^{-4} and an energy efficiency of 1.61pJ/bit. Experimental verification of the full PAM4 transceiver at 50Gb/s operation shows -4.66dBm OMA sensitivity at a BER~$4x10^{-4}$.**

***Keywords*—Avalanche photodiode, heterogeneous integration, microring modulator, optical transceiver, PAM4, silicon photonics.**

I. Introduction

Modern datacenters are now being architected to handle large artificial intelligence workloads. This involves both scaling up with more xPUs in compute clusters and scaling out to larger clusters with higher per-lane data rates in the interconnect network. Flatter network topologies with higher-radix switches also offer improved performance but require more longer-distance data communication [1]. This motives an increased amount of optical transceiver links within server racks that can achieve very high bandwidth density in an energy-efficient manner.

Increased per-wavelength data rates are possible with transceivers that support four-level pulse amplitude modulation (PAM4). In addition, leveraging wavelength-division multiplexing (WDM) allows for further increases in bandwidth density. Optical link architectures based on silicon photonic microring modulators (MRMs) and drop filters offer an attractive solution due to their inherent WDM capability [2, 3]. However, several challenges exist in achieving robust operation of microring-based optical transceivers. MRM transmitters require high voltage swing at high data rates and compensation of both static and dynamic non-linearities. While at the receive side, the higher signal-to-noise ratio (SNR) requirements of PAM4 operation require techniques to improve front-end gain and sensitivity.

This work presents high-speed PAM4 transmitter and receiver front-ends implemented in a 28nm CMOS process that are co-designed with silicon photonic optical devices to address these issues and enable energy-efficient operation. Efficient PAM4 transmission is achieved with an optical digital-to-analog converter (DAC) approach with the MRM device segmented into MSB and LSB phase shifters that are driven by two PAM2 AC-coupled pulsed-cascode high-swing voltage-mode output stages. This 80Gb/s PAM4 transmitter includes individual MSB/LSB swing control to compensate for MRM static non-linearities and both edge-rate control and a 2-tap non-linear feed-forward equalizer (FFE) to compensate for dynamic non-linearities. Improved 56Gb/s PAM4 receiver sensitivity is achieved by utilizing a silicon-germanium (Si-Ge) avalanche photodiode (APD) interfacing with an analog front-end that has a low-bandwidth transmimpedance amplifier (TIA) input followed by continuous-time linear equalizer (CTLE) and variable-gain amplifier (VGA) stages.

II. PAM4 Microring Modulator Transmitter

PAM4 modulation is efficiently achieved with an optical DAC approach that requires only PAM2 drivers. Fig. 1(a) shows the depletion-mode microring modulator that has both longer MSB and shorter LSB phase shifter segments. These phase shifter segments have a Z-shaped profile with four different carrier implantation that enhances the interaction between the junction depletion region and the optical mode, resulting in a combined resonant shift of 28pm/V [4]. This two-segment device acts as an optical DAC, combining the two PAM2 electrical data streams into a single PAM4 optical output. Designing the two-segment carrier-depletion microring modulator with an MSB:LSB length ratio of 2:1 allows for nominally uniform PAM4 level spacing with the laser wavelength slightly offset from the resonant frequency, as illustrated in the Fig. 1(b) transmission curves. Further fine tuning of the PAM4 output power levels is achieved by varying the MSB and LSB drivers' output voltage swing.

Fig. 2(a) shows the PAM4 transmitter block diagram with two PAM2 output stages that drive the MRM device's phase shifters [5]. A PRBS generator outputs 16 parallel bits at one-eighth rate, with the eight odd/even bits respectfully representing the MSB/LSB data streams that are separately serialized in two stages. An initial 8:4 serializer stage, which is switched with two one-eighth rate clock phases, provides quarter-rate data to the final three parallel 4:1 serializers that are switched with four quadrature-spaced clock phases from an injection-locked oscillator (ILO) clock generator. These three serializers are utilized to implement a 2-tap non-linear feed-forward equalizer (FFE) in the segmented output driver (Fig. 2(b)), with the TAP0 data driving the main cursor segments and the TAP1R/F respectively driving the first post-

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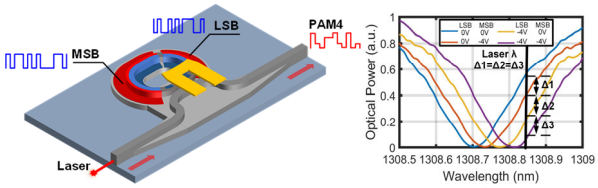
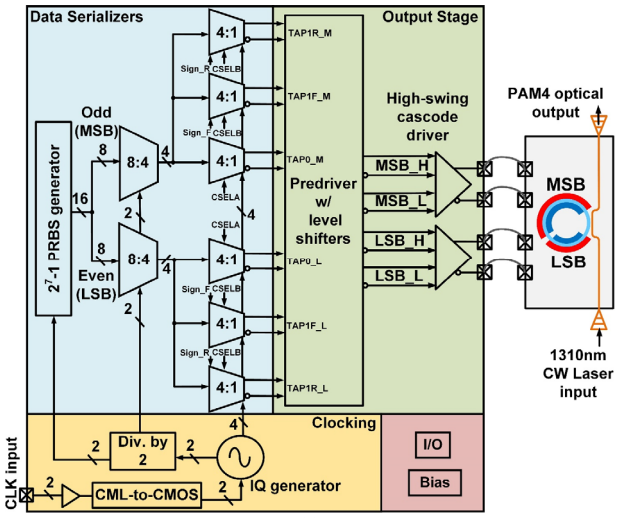
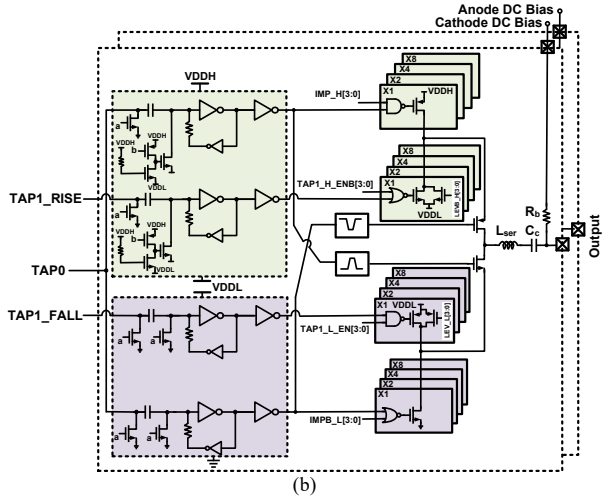


(a) (b)

Fig. 1. (a) Microring modulator device with MSB and LSB phase shifters for optical DAC-based PAM4 generation. (b) Transmission curves with resonance shift configured for equal PAM4 output levels.



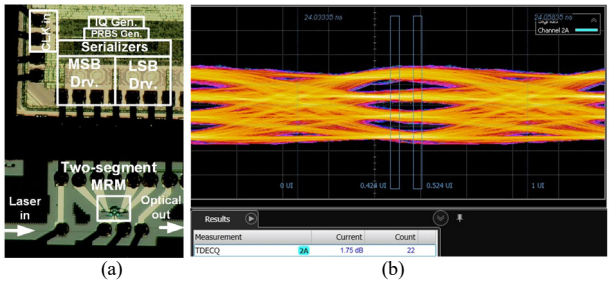
(a)



(b)

Fig. 2. (a) PAM4 optical transmitter block diagram. (b) High-swing differential pulsed-cascode output driver with output swing and edge-rate control and 2-tap nonlinear FFE.

cursor rising- and falling-edge segments. High-swing differential pulsed-cascode output drivers are utilized to reliably achieve an output swing close to 4X the nominal CMOS supply on the MRM device. The primary pull-down path consists of the bottom NMOS segments, which are switched with nominal CMOS logic levels, in series with a shared NMOS cascode transistor whose gate is pulsed during a falling transition by level-shifted logic operating between VDD and 2*VDD. Parallel PMOS segments in the pull-down path are statically configured for output swing control and dynamically switched to implement the falling-edge post-cursor FFE tap. In a similar manner, the primary pull-up path consists of the top PMOS segments, which are switched with level-shifted CMOS logic levels, in series with a shared



(a) (b)

Fig. 3. (a) Optical transmitter prototype assembly. (b) 80Gb/s PAM4 optical eye diagram.

PMOS cascode transistor whose gate is pulsed during a rising transition by logic operating at the nominal CMOS supply. Parallel NMOS segments in the pull-up path are statically configured for output swing control and dynamically switched to implement the rising-edge post-cursor FFE tap. Segmenting the main bottom NMOS and top PMOS transistors provides edge-rate control that is utilized for fine-tuning the relative delay between the MSB and LSB drivers to optimize the output optical PAM4 signal. At the driver output, series inductive peaking is utilized to provide bandwidth extension and AC-coupling with a simple resistive bias tee allows for proper reverse-bias MRM operation.

The transmitter prototype was fabricated in a 28nm CMOS process and the two-segment MRM device is fabricated in a 130nm SOI process. Fig. 3(a) shows the hybrid-integration approach with the two chips adjacently placed and short wirebonds connecting the MSB and LSB drivers' outputs to the two-segment MRM device. Grating couplers are utilized to bring the continuous-wave light in from the left and output the modulated signal to the right. An on-die resistive heater provides MRM resonance wavelength control. Fig. 3(b) shows the measured 80Gb/s PAM4 eye diagram with a 3.42V_{ppd} output swing and the 2-tap non-linear FFE enabled. A >5dB dynamic extinction ratio and a transmitter and dispersion eye closure quaternary (TDECQ) metric of 1.75dB is achieved. The transmitter consumes 293mW (3.66pJ/bit) and achieves a FOM of 1.07pJ/(bit*V).

III. Avalanche Photodiode Receiver

Fig. 4 shows a block diagram of the PAM4 optical receiver [6]. An avalanche photodiode provides photocurrent to a CMOS all-inverter-based analog front-end (AFE) that consists of an input transimpedance amplifier (TIA) that is followed by continuous-time linear equalizer (CTLE) and variable-gain amplifier (VGA) stages. This AFE drives four parallel PAM4 slicer banks that are clocked with quadrate-spaced clocks from an ILO clock generation block. The four parallel thermometer-encoded slice outputs then pass through a 4:8 demultiplexer stage, undergo thermometer-to-binary conversion, and then final 8:16 demultiplexing.

Further AFE details are shown in Fig. 5(a). High bandwidth is achieved with series inductive peaking, utilized both at the input and between the TIA and CTLE, that distributes the capacitance between these blocks. Reduced input-referred noise is also achieved by intentionally designing the input TIA with a low 7GHz bandwidth and 400Ω feedback resistor. Fig. 5(b) shows the subsequent CTLE stage that provides frequency peaking to partially recover the AFE bandwidth after the low-bandwidth input TIA. This CTLE block works with low-frequency input signals experiencing a subtraction between the lower and upper signal

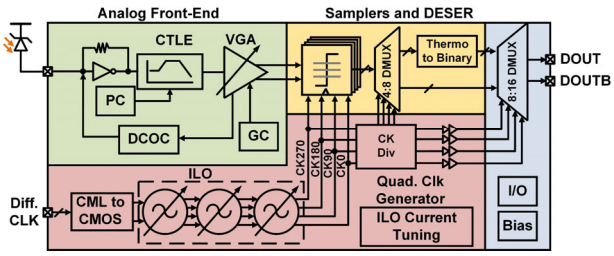
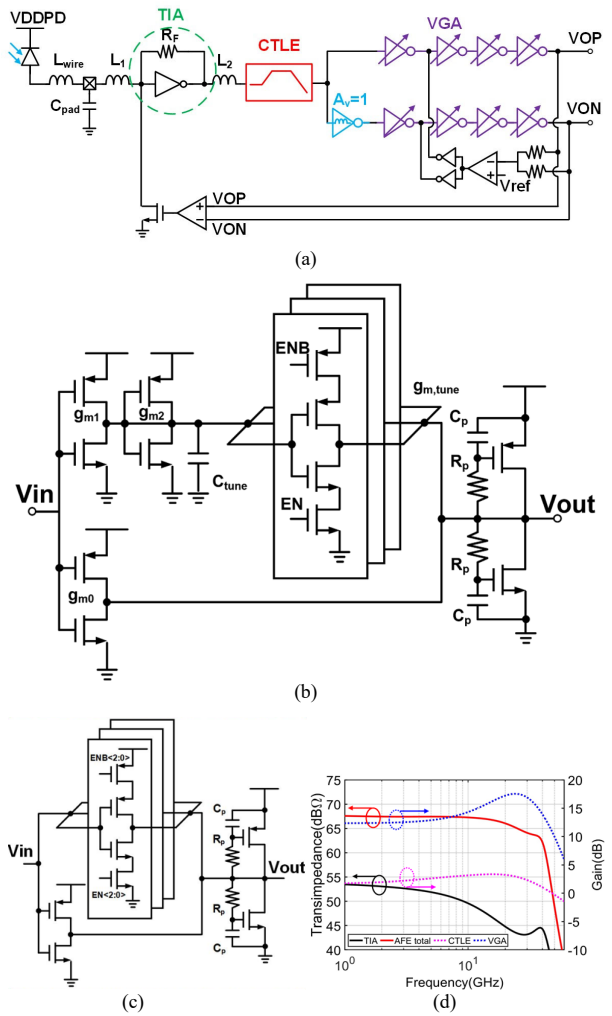


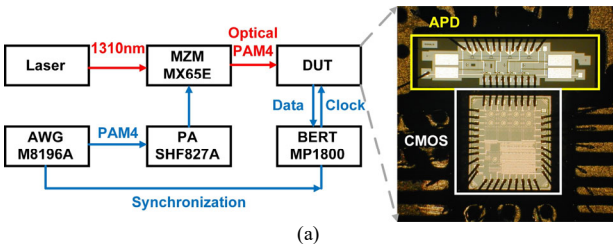
Fig. 4. PAM4 optical receiver block diagram.



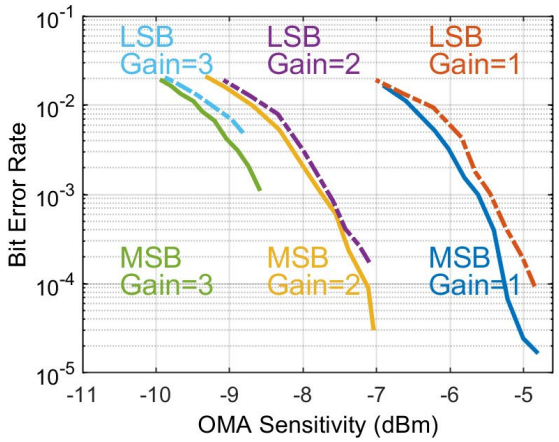
(a) (b) (c) (d)

Fig. 5. (a) Optical receiver analog front-end with low-bandwidth input TIA. (b) Inverter-based CTLE and (c) VGA stages. (d) Analog front-end frequency response.

paths at the output diode-connected load, while the shunt C_{tune} capacitor shorts out the high-frequency components of the upper signal path to provide frequency peaking. Segmentation of the upper-path final $g_{m,tune}$ stage provides 5dB peaking tuning range with 8 settings. Fig. 5(c) shows the final VGA block that consists of cascaded stages of tunable inverter-based transconductance segments that drive a diode-connected load to provide close to 3dB gain tuning. Both the diode-connected loads of the CTLE and VGA stages include additional resistors in series with the transistor gates to implement active-inductor shunt peaking for bandwidth extension. As shown in Fig. 5(d), these techniques allow for a simulated 67.5dBΩ gain and 38GHz bandwidth.



(a)



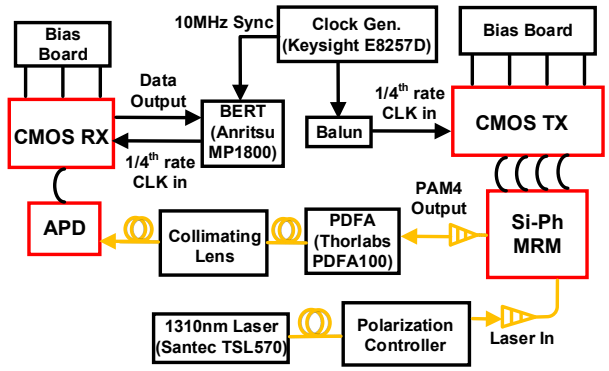
(b)

Fig. 6. (a) Optical receiver measurement setup and prototype assembly. (b) Measured 56Gb/s PAM4 bit error rate vs OMA sensitivity.

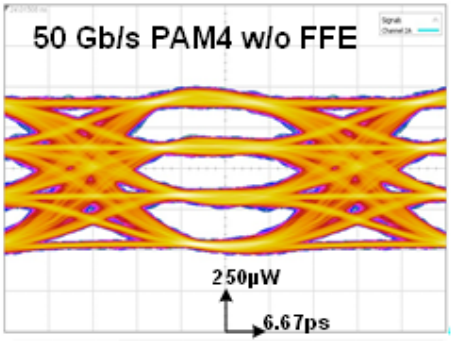
After the AFE, the PAM4 symbols are resolved with four parallel segments that perform a 2b flash ADC operation. Each segment has three regenerative latches operating on single clock phase that consist of a two-stage PMOS dynamic amplifier with a regeneration stage in parallel with the second stage [7]. Each slicer has offset correction and threshold generation implemented with a parallel differential input pair that is driven with a voltage DAC.

A four-channel receiver prototype was fabricated in a 28nm CMOS process and tested with silicon-germanium (Si-Ge) avalanche photodiodes at the drop ports of microring drop filters. The APD devices employ a graded doping in the Ge layer that creates a quasi-electric field, which improves carrier transport by reducing hole transit time while maintaining nearly the same electron transit time. This results in a higher APD speed and an extended 3-dB bandwidth [8].

Fig. 6(a) shows the optical receiver measurement setup and the hybrid-integration approach with the two chips adjacently placed and short wirebonds connecting the APDs' outputs to the CMOS optical receiver channels. 56Gb/s PAM4 data from an arbitrary waveform generator is passed through a power amplifier to drive a Mach-Zehnder modulator (MZM) with a 1310nm continuous wave input. A grating coupler is then utilized to bring the MZM's modulated light into the photonic integrated circuit from the left and a microring drop filter is tuned with on-die resistive heaters to drop the signal onto the APD at the channel of interest. The optical receiver's deserialized data is then multiplexed out of the chip for BER testing. Fig. 6(b) shows the measured 56Gb/s PAM4 OMA sensitivity with varying APD gain. A BER=10^{-4} is achieved at -4.6dBm optical modulation amplitude (OMA) sensitivity with APD gain of one. The sensitivity improves to -7dBm at a BER=10^{-4} as the APD gain increases to two. However, further increases in the APD gain result in limited bandwidth



(a)



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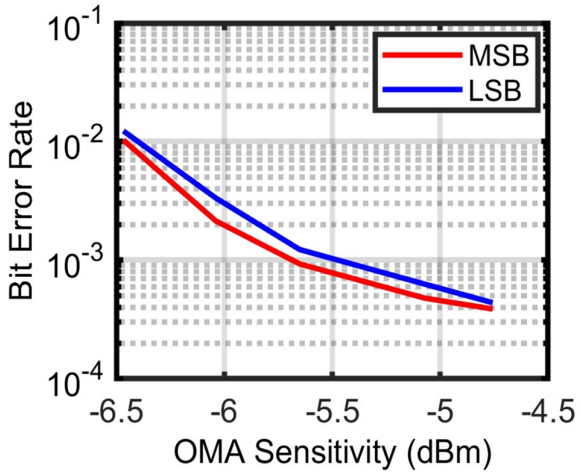

(c)

Fig. 7. (a) Optical transceiver measurement setup. 50Gb/s PAM4 (b) transmitter output eye diagram and (c) receiver BER vs OMA sensitivity.

and BER degradation. The receiver consumes 90.2mW (1.61pJ/bit) from a 1V supply.

IV. Full Link Experimental Results

Experimental verification of a complete PAM4 transceiver link is performed with the Fig. 7(a) setup. A signal generator provides a differential quarter-rate input clock to the CMOS transmitter IC to generate the required serialization clock signals of the MSB and LSB drivers that are attached to the optical DAC MRM device on the silicon photonic chip via short wirebonds. The 1310nm continuous wave light input originates from a laser source and passes through a polarization controller before being coupled into the MRM chip. In order to compensate for link losses, which are primarily due to the grating couplers, the modulated output light then passes through a praseodymium-doped fiber amplifier (PDFA) and a collimated lens to couple to a commercial APD (Albis APD20D1) that uses a -15.5V bias. This APD is connected to the CMOS receiver IC via short wirebonds. A bit error rate tester, synchronized with the transmitter clock source, provides the required quarter-rate clocks to the receiver IC and verifies the BER of the deserialized data.

Fig. 7(b) shows that a wide-open 50Gb/s PAM4 eye diagram is achieved with the optical DAC MRM transmitter. Applying this signal to the receiver with the APD biased at a gain of 2 results in an OMA sensitivity of -4.66dBm at a BER~$4X10^{-4}$ (Fig. 7(c)). Note that the OMA sensitivity performance degradation relative to the stand-alone receiver characterization is primarily due to noise introduced by the PDFA. Reducing grating coupler loss would allow for potential elimination of the PDFA and overall improved performance.

V. Conclusion

This paper presented high-speed PAM4 transmitter and receiver front-ends implemented in a 28nm CMOS process that are co-designed with silicon photonic optical devices to enable energy-efficient operation. The transmitter utilizes an optical DAC approach with two PAM2 AC-coupled pulsed-cascode high-swing voltage-mode output stages to drive the MRM MSB/LSB segments. Individual MSB/LSB swing control compensates for MRM static non-linearities and both edge-rate control and a 2-tap non-linear feed-forward equalizer (FFE) compensates for dynamic non-linearities. Improved PAM4 receiver sensitivity is achieved by utilizing a Si-Ge APD interfacing with an analog front-end that has a low-bandwidth TIA input followed by CTLE and VGA stages.

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