Quantification of Contact-Doping Effect in Ultrathin In_2O_3 Transistors

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***Abstract*—In this work, we quantify the contact-doping effect (CDE) by extracting the contact-doping length (ΔL) in ultrathin In_2O_3 transistors based on a modified transfer length measurement (TLM) model. The extracted ΔL values range from 0.55 to 0.30 µm, which are consistent with the channel length (L_{ch}) where threshold voltage (V_T) roll-off happens in In_2O_3 devices. The above observations suggest that CDE might be one of the reasons for the V_T roll-off in In_2O_3 transistors.**

I. Introduction

Oxide semiconductor (OS) field-effect transistors (FETs) have drawn significant attention for their promising use as back-end-of-line (BEOL) compatible transistors in monolithic 3D integration [1-5]. Among various OS FETs, atomic-layer-deposited (ALD) In_2O_3 FETs stand out due to their exceptional conformality and uniformity on 3D structures achieved through ALD process [2], high electron mobility of 152 $cm^2/(V\cdot s)$ versus other OS materials [3], ultrahigh on-current of nearly 20 mA/µm in gate-all-around structure [4], and remarkable reliability [5]. In this work, for the first time, we quantify the contact-doping effect (CDE) by extracting the contact-doping length (ΔL) in In_2O_3 transistors using a modified transfer length measurement (TLM) model. The extracted ΔL values are consistent with the channel length (L_{ch}) where the threshold voltage (V_T) roll-off starts to happen, which implies that CDE might be the one of the reasons behind the V_T roll-off of In_2O_3 FETs.

II. Experiments

Fig. 1 (a) shows the schematic device structure of a back-gated In_2O_3 FET with the fabrication process shown in **Fig. 1 (b)**. Regarding the gate stack, 6 nm Al_2O_3 (by atomic layer deposition (ALD) at 175 °C), 60 nm Ni (by e-beam evaporation), 4 nm HfO_2 (by ALD at 200 °C), and In_2O_3 (by ALD at 225 °C), are used as gate metal adhesion layer, gate metal, gate dielectric, and channel material, respectively. 60 nm Ni was then e-beam evaporated as the source and drain (S/D) metals. Finally, BCl_3/Ar dry etching was used to isolate the devices and define the channel width.

III. Results and Discussions

Fig. 2 (a) illustrates the $I_D – V_{GS}$ curves of In_2O_3 transistors with channel thickness (T_{ch}) of 1.2 nm and L_{ch} from 1 µm to 60 nm. An obvious negative shift of V_T can be observed when the L_{ch} reduces from 1 to 0.6 µm. Similar V_T roll-off behavior can also be seen in In_2O_3 FETs with thicker T_{ch} of 2.0 nm when L_{ch} scales down to 0.2 µm (**Fig. 2 (b)**). Based on the natural length theory [6, 9], the natural length (λ) of SOI (silicon-on-insulator, which has similar device structure to our back-gated devices) transistors can be defined as

$$\lambda = \sqrt{\varepsilon_{ch}/\varepsilon_{ox} \cdot T_{ch} \cdot T_{ox}} \quad (1)$$

where ε_{ch} is the dielectric constant of the channel material (In_2O_3 with ε_{ch} = 8.9 [7]), ε_{ox} is the dielectric constant of the gate oxide (HfO_2 with ε_{ox} ~ 9.0 [8]), T_{ch} is the thickness of the channel material (T_{ch} = 1.2 to 2.0 nm), and T_{ox} is the thickness of the gate oxide (T_{ox} = 4.0 nm). For our In_2O_3 devices, λ = 2 – 3 nm can be calculated using (1). Based on natural length theory [9], when $L_{ch} > 5\lambda$ = 10 – 15 nm, the In_2O_3 transistors studied here should not be affected by the short channel effect (SCE) since the channel control from gate is stronger than the control from S/D. As a result, the V_T roll-off happening at long L_{ch} of 0.6 – 0.2 µm shown in **Fig. 2** is probably not caused by the ordinary SCE but by other mechanisms, such as CDE introduced by S/D contacts. CDE makes the carrier density inside the In_2O_3 channel non-uniform with the channel near the S/D contacts having higher carrier concentration, like the n^+ doping region in traditional Si MOSFETs. The above idea of non-uniform channel is visualized in **Fig. 3**. **Fig. 3 (b)** illustrates the schematic carrier density profile in long L_{ch} (>= 0.8 µm) In_2O_3 transistors with n^+ (high carrier density) regions near the S/D and n (medium carrier density) region in the channel center. Here we define ΔL as the portion of channel that is n^+ region with ΔL/2 contributed from source and ΔL/2 contributed from drain. When the L_{ch} is short enough (<= 60 nm), the n^+ regions from S/D will merge as presented in **Fig. 3 (a)**. Based on **Fig. 3**, a modified TLM model is developed to extract the ΔL which can quantify the CDE (**Fig. 4**). From the long L_{ch} part in the TLM analysis, we can extract the sheet resistance of n region ($R_{sh,n}$), as shown in **Fig. 4 (b)**. On the other hand, from the short L_{ch} part, the sheet resistance of n^+ region ($R_{sh,+}$) can be extracted (**Fig. 4 (a)**). Combining the $R_{sh,n}$ and $R_{sh,+}$, ΔL can be calculated based on the equation in **Fig. 4 (b)**. **Fig. 5** and **Fig. 6** present the TLM results of In_2O_3 FETs with T_{ch} of 1.2 nm and 2.0 nm, respectively. In each TLM result, linear fitting was adopted in short L_{ch} (**Fig. 5 (a)** and **Fig. 6 (a)**) and long L_{ch} regions (**Fig. 5 (b)** and **Fig. 6 (b)**) to extract $R_{sh,n}$, $R_{sh,+}$, and ΔL. **Fig. 7** exhibits the extracted $R_{sh,n}$ and $R_{sh,+}$ as a function of V_{GS}. The clear difference between $R_{sh,n}$ and $R_{sh,+}$ corroborates the existence of n^+ regions resulting from CDE and the n region at the channel center. **Fig. 8 (a)** demonstrates the extracted ΔL from In_2O_3 FETs with T_{ch} of 1.2 nm and 2.0 nm as a function of V_{GS}. When $V_{GS} \sim V_T$, the ΔL is 0.55 µm for T_{ch} = 1.2 nm and 0.30 µm for T_{ch} = 2.0 nm. The large ΔL values explain why the V_T roll-off happens even when the L_{ch} is still far from the natural length (5λ = 10 – 15 nm) of the transistors. For example, while L_{ch} > ΔL, the reduction of L_{ch} has small impact on V_T since the carrier density at the channel center is not yet affected by the n^+ region extending from S/D. However, when L_{ch} <= ΔL, the n^+ regions from S/D start to merge and increase the carrier density at the channel center, which causes the negative shift of V_T and the abnormal V_T roll-off. The reason why we call this "abnormal" V_T roll-off is based on our understanding of SCE derived from natural length theory. **Fig. 8 (b)** shows the $V_T – L_{ch}$ relation with L_{ch} = ΔL highlighted. One can observe that the L_{ch} where In_2O_3 FETs start to have V_T roll-off are consistent with our ΔL extracted, which supports our explanation that CDE might be one of the reasons for the abnormal V_T roll-off in In_2O_3 FETs.

Acknowledgment: This work is supported by NSF, SRC and Samsung Electronics.

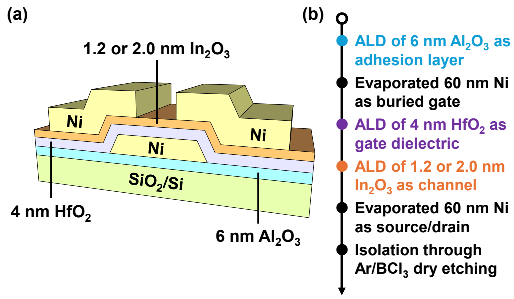

Fig. 1. (a) Device schematic of a buried-gated In_2O_3 transistor. **(b)** Fabrication process flow of buried-gated In_2O_3 transistors.

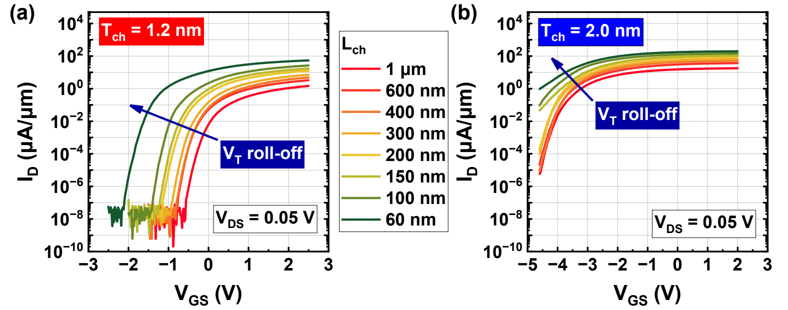

Fig. 2. Transfer characteristics of In_2O_3 transistors with channel length (L_{ch}) = 1 um – 60 nm at different In_2O_3 channel thicknesses (T_{ch}) of **(a)** 1.2 nm and **(b)** 2.0 nm.

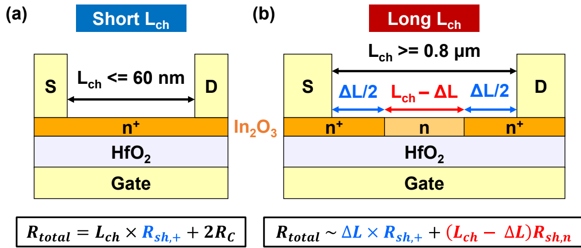

Fig. 3. Cross-section of In_2O_3 transistors with schematic carrier density profiles along the In_2O_3 channel for **(a)** short L_{ch} (<= 60 nm) case and **(b)** long L_{ch} (>= 0.8 μm) case. "n^+" represents the high carrier concentration region while "n" stands for the medium carrier concentration region. The total channel resistance (R_{total}) equations for each case are also written. $R_{sh,+}$ is the sheet resistance of n^+ region. $R_{sh,n}$ is the sheet resistance of n region.

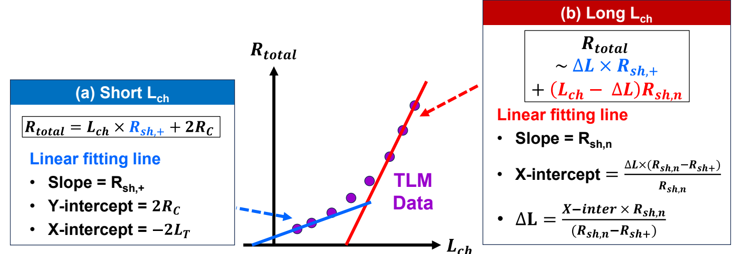

Fig. 4. Proposed TLM model for the analysis of $R_{total} - L_{ch}$ if transistors have non-uniform carrier density profiles along the channel. The $R_{total} - L_{ch}$ relation can be split into two parts: **(a)** short L_{ch} region, corresponding to the case of **Fig. 3 (a)**; **(b)** long L_{ch} region, corresponding to the case of **Fig. 3 (b)**. Combining the TLM analysis from short and long L_{ch} devices, the contact doping length (ΔL) can be extracted.

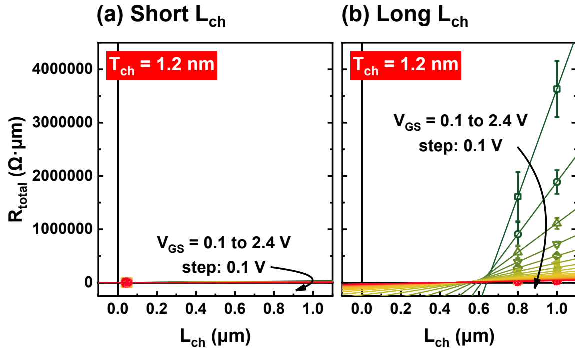

Fig. 5. (a) Short L_{ch} (<= 60 nm) and **(b)** long L_{ch} (>= 0.8 μm) TLM analysis on In_2O_3 FETs with T_{ch} of 1.2 nm.

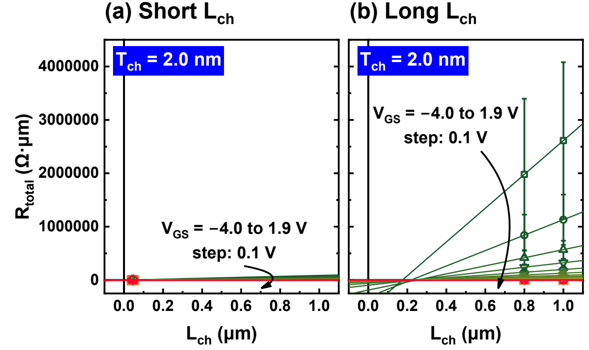

Fig. 6. (a) Short L_{ch} (<= 60 nm) and **(b)** long L_{ch} (>= 0.8 μm) TLM analysis on In_2O_3 FETs with T_{ch} of 2.0 nm.

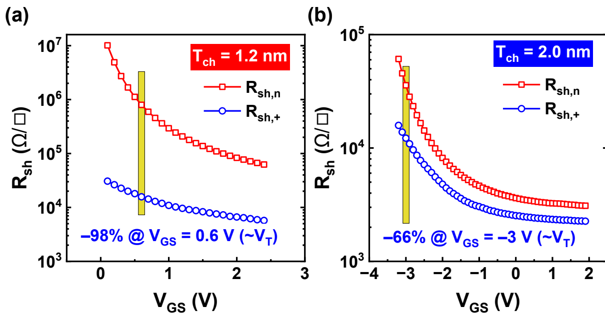

Fig. 7. Extracted $R_{sh,n}$ and $R_{sh,+}$ from the In_2O_3 FETs with T_{ch} of **(a)** 1.2 nm and **(b)** 2.0 nm as a function of V_{GS}. The $R_{sh,n}$ and $R_{sh,+}$ near $V_{GS} \sim V_T$ are highlighted.

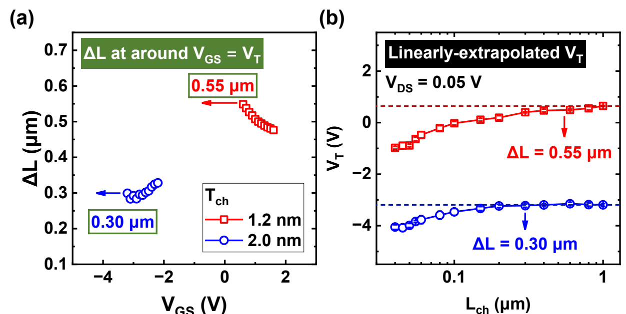

Fig. 8. (a) Extracted ΔL as a function of V_{GS} with T_{ch} of 1.2 and 2.0 nm. ΔL values at $V_{GS} \sim V_T$ are highlighted. **(b)** Linearly extrapolated V_T as a function of L_{ch}. The extracted ΔL values are consistent well with the L_{ch} where the V_T roll-off starts.

Reference:

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