

**Synchronous switched circuits for enhanced energy extraction from
triboelectric kinetic energy harvesters**

by

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DEDICATION

To all my teachers

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ABSTRACT

Internet of Things (IoT) sensors are finding increasing usage in today's 'smart' City/Building/Factory/Agriculture/Healthcare settings. A challenge with remote-monitoring IoT sensors lies in their battery-powered operation that requires human intervention to periodically replace batteries, increasing maintenance cost. Harvesting ubiquitous background kinetic energy is an attractive *green* solution to self-power the IoTs. In this context, Triboelectric Nanogenerators (TENGs), a class of ambient kinetic energy harvesters with their material and design versatility, have emerged as a promising cost-effective solution to self-power the IoTs in the past decade.

This research fundamentally investigates the TENG's cyclic transduction operation and proposes novel synchronous-switched Energy Extraction Circuits (EECs) that *actively* condition the TENG charge (equivalently voltage) in sync with TENG operation to enhance the TENG's per-cycle transduced energy. The overall objective is developing an EEC interfacing the AC TENG source with the IoT's on-board DC storage (battery/ capacitor) that (a) provides rectification, (b) maximizes TENG's energy output, and (c) maintains the energy optimality even as the external mechanical input condition (accordingly the TENG parameters) changes. In that context, this dissertation reports the design, simulation, mathematical modeling, optimization, and comparison of the following *seven* circuit architectures as TENG EEC candidates,

- Standard Full Wave Rectifier circuit (FWR) (*reference circuit for comparison*)
- Synchronous Switched Harvesting on Inductor (SSHI) class of circuits:
 - Parallel-SSHI
 - Series-SSHI
- Synchronous Charge Extraction (SCE) class of circuits:
 - Standard SCE
 - Pre-biased SCE (pSCE)
 - Self-propelled Pre-biased SCE (spSCE)
 - Multi-Shot SCE (MS-SCE)

Barring the Standard FWR and Standard SCE, the rest of the architectures have been proposed as TENG EEC for the first time in this work.

In the first set of works, detailed analytical circuit models for FWR, P-SSHI, and the SSHI circuits are developed to derive their per-cycle energy output, optimal load (as in MPP: Maximum Power Point), and upper bound on load. The analytical results are validated against the simulated and those measured by testing using a custom-made experimental TENG. SSHI circuits showed up to $8.5\times$ experimental gain over the Standard FWR; however, their optimal load operation over varying ambient input conditions requires a second-stage DC/DC converter with closed-loop MPP Tracker, increasing the overhead power consumption and, thus, reducing the net output.

Next, we study the SCE circuit with the desirable trait of providing a constant level of transduced energy, regardless of the load voltage, i.e., MPPT-free operation and also one that exceeds the reference FWR circuit's optimal energy output. Building on the SCE circuit architecture, we propose a pre-biased SCE (pSCE) circuit that is analytically shown to provide a further boost beyond the SCE output through its synchronous pre-biasing (pre-charging) technique. Measured results with the discrete component implementation of pSCE on PCB provide validation with its up to $2.1\times$ gain over the SCE circuit. A drawback with pSCE lies in its complex control that requires TENG-specific manual tuning. The next proposed architecture, Self-propelled pre-biased SCE (spSCE), addressed this challenge by offering plug-and-play self-tuned pSCE action, i.e., applicable for any TENG and under any operating ambient input condition, thus, meeting the set EEC design goals.

To achieve compact and low-loss EEC, we move from discrete component to on-chip design with our novel on-chip compatible Multi-shot SCE (MS-SCE) architecture that extracts energy from TENG in multiple short bursts to maintain operating voltage just below the technology's breakdown limit. The MS-SCE is mathematically shown to be MPPT-free and universally-optimal, as in extracting energy higher than the optimal FWR for any given TENG under any operating conditions. The implementation and simulation in TSMC $0.18\mu\text{m}$ 70V BCD process provide validation, showing $>1.91\times$ net gain over the optimal FWR.

CHAPTER 1. GENERAL INTRODUCTION

The Internet of Things (IoT) sensors and subsequent data-driven decision making is one of the primary driving forces of the ongoing Industry 4.0 transformation. The global market for IoT sensors was valued at \$10.9 billion in 2021 and is expected to grow at a CAGR of 27.4% to reach \$36.6 billion by 2026 [1]. One major application for IoT sensors is remote asset monitoring and ensuing predictive maintenance to avoid costly failures and unplanned downtime. For example, out of more than 617 thousand bridges in the US, nearly 46 thousand or 7.5% are structurally deficient and can benefit from IoT-based Structural Health Monitoring (SHM) [2]. At the same time, IoT-based Machine Health Monitoring (MHM) is estimated to reduce factory equipment downtime by up to 50% and reduce maintenance costs by up to 40% [3]. IoT in the human-health setting is another area witnessing large interest and growth [4]. Examples include wearables for remote patient monitoring [5], worker safety monitoring [6], and ‘smart’ cardiovascular, dental, and orthopedic implants for real-time monitoring of disease progression and post-surgery recovery [7]. Overall, IoT sensors find usage across varied application segments and form the backbone of today’s ‘smart’ City/Ag/Building/Factories/Healthcare revolution.

1.1 Motivation for ambient micropower energy harvesting

One challenge with the wide adoption of remote monitoring IoT sensors is their limited battery life, requiring human intervention for periodic battery replacement, some of which could be in hazardous areas. This challenge is brought forth in [8] as: “*The cost of getting to a remote sensor to change a battery is often higher than the cost of the battery itself*”. Further, as the IoT devices scale in number, with a single factory floor having hundreds of sensors, the maintenance cost of tracking their battery status and replacing the spent batteries shall continue to grow with the involved frequent manual effort weakening the core value of wireless sensing. It is predicted

that the world will reach a trillion IoT devices by 2035 [9], amounting to a cumulative 274 million battery replacements every single day even with an optimistic 10-year battery lifetime [10]; clearly, an unsustainable scenario. With a majority of these spent batteries (predominantly lithium-ion) ending up in landfills (current recycling ratio is $\sim 5\%$ [11]), their chemicals shall also flare up the environmental pollution issue. The severity of limited battery life is even higher in the case of biomedical implants, as the battery replacement requires invasive and costly medical surgery. In [12], it is noted that cardiac defibrillator implants have an average lifetime of 59 months, plus 8% of these implants witness a premature battery depletion within 36 months. Even for wearables, a need for frequent battery charging reduces their ease of use and can cause loss of critical data in case of an unexpected battery outage. Thus, it is imperative to extend the battery life of IoT sensors, or better, to make them battery-free.

A possible solution lies in integrating a miniaturized energy harvester that scavenges ambient energy for sustainable self-powered operation of the IoT sensor. In this context, energy harvesters that transduce from light, thermal, kinetic (mechanical), and electromagnetic (RF) energy have been developed [13]. The typical values of power density harvested from these ambient energy sources are listed in Table 1.1 [14], which suggest that a mesoscale integrated energy harvester can self-power an IoT sensor with 0.1-1 mW power requirement. Also, advances in the electronics technology for the IoT system's sensors/microprocessors/radio, etc. continue to lower the overall required power, thereby improving the feasibility of using ambient energy harvesters to self-power the IoTs. For example, a recently reported temperature sensing self-powered IoT system transmitting data via BLE (Bluetooth Low Energy) every 5 minutes consumes average power of only $7.61\mu\text{W}$ [15]. In another low-power demonstration, a System on Chip (SoC) for continuous health monitoring of an electrical machine by tracking temperature, relative humidity, vibration, and magnetic field reported consumption of only $89.1\mu\text{W}$ and is compatible with multiple energy harvesting modalities [16]. Further examples of energy-harvester-powered IoTs from both academia and industry can be found in reviews such as [13], [14], and [17].

Table 1.1 Ambient energy sources and corresponding typical harvested power density [14]

Source		Harvested power density
Light	Indoor	$10 \mu\text{W}/\text{cm}^2$
	Outdoor	$10 \text{mW}/\text{cm}^2$
Kinetic	Human	$4 \mu\text{W}/\text{cm}^2$
	Industrial	$100 \mu\text{W}/\text{cm}^2$
Thermal	Human	$30 \mu\text{W}/\text{cm}^2$
	Industrial	$1\text{-}10 \text{mW}/\text{cm}^2$
RF	Cellular	$0.1 \mu\text{W}/\text{cm}^2$

This research focuses on kinetic energy harvesters that have a universal appeal owing to the ready availability of motion energy in a wide variety of ambient environments, such as in the form of wind/water flow, machine/structure vibration, human body motion, etc. [17, 18, 19, 20] Kinetic harvester integrated self-powered IoT sensing is feasible in multiple applications of industrial interest such as Structural Health Monitoring (SHM) of bridges/ wind-turbines/ airplane-wings, etc., factory floor or agricultural Machine Health Monitoring (MHM), and environmental sensing. Amidst the choice of various mechanical to electrical energy transducers such as piezoelectric, electromagnetic, electrostatic, electrochemical, and triboelectric [21, 22, 23, 24, 25], the latter offers a new opportunity by its versatility of material choices, fabrication methods, and designs [26, 27] as elaborated in Sec. 1.2.2.

1.2 Triboelectric Nanogenerator (TENG) as a kinetic energy harvester

The Triboelectric effect refers to the generation of static surface charge on frictional contact between any two dissimilar materials. It is a day-to-day effect that is undesirable in most cases, for example, electronics failure by high-voltage static discharge. However, this effect was proposed for use in energy harvesting by conjugation with the electrostatic induction in 2012 to device Triboelectric Nanogenerator or TENG in short [28]. Since then, it has received a huge academic interest as a solution to self-power electronics and is now at the brink of commercial adoption

[29]. Next, the working principle of the TENG is briefly explained, and its key advantages over other mechanical to electrical energy transducers are listed.

1.2.1 Working Principle

An operation cycle of the generic contact-separation type TENG generating AC output is shown in Fig. 1.1(a). A contact-separation type TENG is essentially a parallel plate capacitor with layers of two different materials used to generate static opposite surface charge by repeated contact (triboelectrification). The relative motion (contact and separation) of the layers with the triboelectric charge induces emf between the two surrounding electrodes (electrostatic induction), which can be tapped to harness electric energy. Thus, conjugation of triboelectrification with electrostatic induction is the working principle of TENG [28]. Note that barring the triboelectric origin of the static surface charge, the working principle of TENG is similar to the electret (pre-charged dielectric) based electrostatic kinetic energy harvester demonstrated and studied earlier in [30], [31], [32], etc.

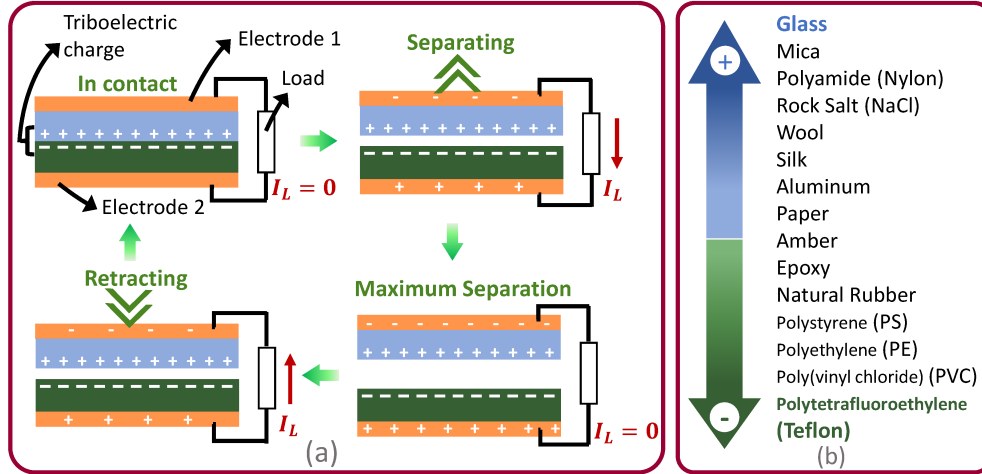


Figure 1.1 (a) Schematic showing operation cycle of a contact-separation TENG. (b) A subset of triboelectric series as per [33].

1.2.1.1 Triboelectric series

All materials, natural or synthetic, can be arranged in a triboelectric series based on their relative tendency to get positively or negatively charged on frictional contact. The magnitude of the triboelectric charge density depends on how far the two materials are located on the triboelectric series. A short example series is shown in Fig. 1.1(b). A comprehensive quantified triboelectric series can be found at [34].

1.2.2 Salient Features

The key advantage of TENG is the vast material choice since all materials are triboelectric in nature, and a combination can be selected to suit the application constraints/requirements. TENGs based on low-cost materials such as paper, recycled materials; environmentally degradable materials; flexible/stretchable polymers for wearable applications such as polydimethylsiloxane (PDMS), nylon, and advanced materials such as graphene and carbon nanotube (CNT) are some of the many examples, demonstrating the versatility of TENG [25, 35, 36, 37, 38].

TENG can also be operated in multiple modes other than the vertical contact-separation mode (one shown in Fig. 1.1(a)) such as lateral sliding, single electrode, and freestanding triboelectric-layer mode [25]. By choosing suitable material and mode, TENG can capture kinetic energy from different forms of motions such as lateral, rotary, bending, and stretching, thereby making them suitable for harnessing energy from a wide range of sources such as machine/structure vibration, sound (acoustic energy), human-body motion (as wearables), and wind/water flow [25, 39, 40]. TENGs have been demonstrated in ultra-low-power setting of in-vivo cardiac motion generating $\sim 0.55 \mu\text{W}$ [41] to large-scale water-wave energy harvesting producing upwards of 10s of mW [42], again showing TENG's wide applicability.

In kinetic energy harvesting, compared to the commonly chosen piezoelectric energy harvester (PEH), which requires specific expensive materials with piezoelectric properties, TENGs can be built with low-cost materials. For example, [43] compared PEH with TENG over the same impact-driven external excitation and found that while TENG's peak-power density is low

(0.5 mW/cm³ vs. PEH's 4.6 mW/cm³); it provides a significantly higher power density per unit cost (346.0 μ W/cm³ per USD vs. PEH's 16.7 μ W/cm³ per USD). This low-cost advantage of TENG translates to good potential for upscaling, i.e., building cost-effective larger-sized energy harvesters; for example, [44] built a spherical TENG buoy with 6 cm diameter using commonly available materials (plastic shell and Al/Nylon/Kapton tapes) harvesting water-wave energy and providing a peak-power of 10 mW. In summary, with its versatile material and design choice, TENG has a promising potential for wide application in kinetic energy harvesting [26, 27]. Next, the circuit model for the TENG is presented to bring forward its unique time-varying internal impedance nature and motivate the challenges associated with the end goal of efficient energy transfer from TENG to the IoT device's onboard storage (battery/capacitor).

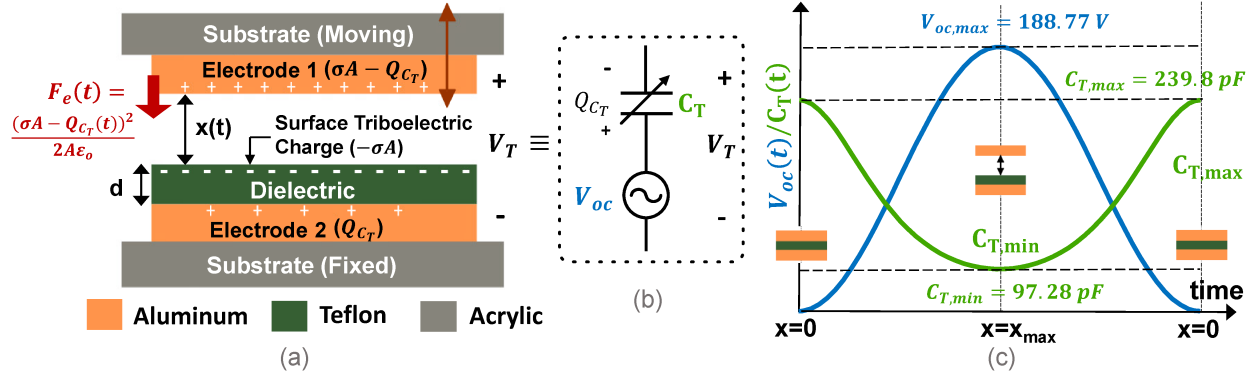


Figure 1.2 (a) Cross section schematic of a contact-separation TENG, $\pm\sigma A$ denotes the triboelectric surface charge on the dielectric and electrode 1 (that also acts as the positive triboelectric layer), Q_{CT} is the external charge drawn on the electrodes, and F_e is the electrostatic force of attraction between the moving upper and fixed lower TENG plates; (b) Lumped-element circuit model of TENG; (c) Variation of TENG electrical parameters: Open circuit voltage (V_{oc}) and Capacitance (C_T) over one operation cycle. Implementation and the marked TENG parameter values as in [45].

1.2.3 Circuit Model

The TENG circuit model is summarized here using an example of contact-separation TENG implemented in our work [45] (presented in chapter 2), and its schematic is shown here in

Fig. 1.2(a). It consists of an upper moving Aluminum electrode plate together with a dielectric (Teflon) tape atop an Aluminum electrode to form the bottom fixed plate (both with a cross-sectional area A). The external periodic mechanical excitation drives the upper plate in a vertical reciprocating motion relative to the stationary bottom plate. The repeated contact of the two plates generates equal and opposite triboelectric surface charge, $\pm\sigma A$. Due to Aluminium vs. Teflon's triboelectric properties, the top plate is positively charged while the bottom plate is negatively charged. Note, the top Aluminum plate here acts both as an electrode and positive triboelectric layer. The generated static (triboelectric) surface charge induces open circuit voltage, V_{oc} , between the two electrodes that is linearly proportional to their separation:

$$V_{oc}(t) = \frac{\sigma x(t)}{\epsilon_0}. \quad (1.1)$$

Here, ϵ_0 is the electrical permittivity of air, and $x(t)$ is the distance between the two plates (air gap) that varies periodically between zero and a certain maximum value termed x_{max} . Further, the TENG forms a variable parallel plate capacitor with an air gap $x(t)$ along with a dielectric of thickness d between the two electrodes. Letting ϵ_d denote the relative permittivity of the dielectric layer, the capacitance $C_T(t)$ is given by:

$$C_T(t) = \frac{\epsilon_0 A}{x(t) + \frac{d}{\epsilon_d}}. \quad (1.2)$$

When connected with an external electrical load, the electrodes draw equal and opposite conduction charges, $\pm Q_{C_T}(t)$ (distinct from the fixed triboelectric $\pm\sigma A$ charge) to generate additional voltage $V_{C_T}(t)$ across those. Accordingly, the overall TENG voltage $V_T(t)$ is given by the superposition of the two voltages:

$$V_T(t) = V_{oc}(t) - V_{C_T}(t) = \frac{\sigma x(t)}{\epsilon_0} - \frac{Q_{C_T}(t)}{C_T(t)}. \quad (1.3)$$

The above TENG operating equation leads to the 1st-order lumped circuit model of a time-varying voltage source in series with a varying capacitor [46] as shown in Fig. 1.2(b). One cycle of TENG operation commences with the two plates in contact, i.e., $x = 0$, and rises to reach the maximum separation of $x = x_{max}$ to complete the first half-cycle, followed by return to the

initial position $x = 0$ in the second half-cycle. The two TENG electrical parameters V_{oc} and C_T are functions of the air-gap, $x(t)$ and vary over a periodic cycle as plotted in Fig. 1.2(c). Thus, TENGs are an AC source with typically high maximum open circuit voltage (188.77 V in the considered example with $x_{max}=1.2$ mm) and a high non-linearly-varying internal capacitive impedance (varying between 97.28 pF and 239.80 pF for the considered TENG with $A=113.8$ cm²; refer Fig. 1.2(c)).

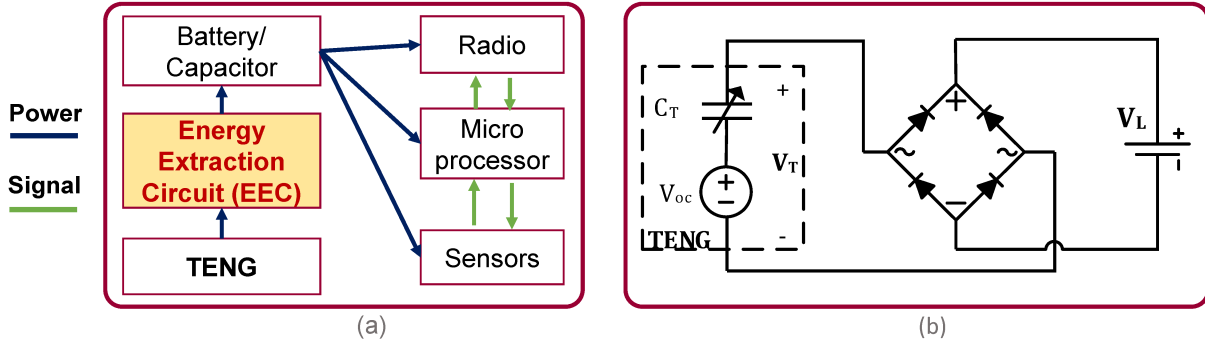


Figure 1.3 (a) Schematic block diagram of a TENG integrated IoT sensor node. (b) Circuit diagram of Full Wave Rectifier (FWR) as the standard EEC for TENG.

1.2.4 Roles of an Energy Extraction Circuit (EEC)

In practice, an Energy Extraction Circuit (EEC) is required to integrate the TENG with an IoT as schematized in Fig. 1.3(a). Firstly, the output of TENG harnessing energy from the environment is AC, and the interfacing EEC provides the rectification to charge the onboard DC load (battery or capacitor). In that sense, the Full Wave Rectifier (FWR) circuit shown in Fig. 1.3(b) is the basic solution and serves as the standard EEC.

Beyond rectification, during the cyclic operation of TENG, the EEC architecture/operation, together with load-voltage, affect the charge drawn on the TENG electrodes (marked $Q_{C_T}(t)$ in Fig. 1.2 (a) and (b)), influencing the electrostatic force of attraction between the two TENG plates ($F_e(t)$ in Fig. 1.2(a), a function of $Q_{C_T}(t)$). The work done by the ambient mechanical force against this electrostatic damping force is the transduced electrical energy, and so effectively,

the choice of EEC and load-voltage determine the transduced energy or, equivalently, the average output power (per-cycle transduced energy times the average source frequency). This indicates that by appropriately adjusting the TENG capacitor charge, Q_{CT} through an intelligently designed EEC action, TENG's transduced energy can be boosted beyond that by the standard FWR circuit and the development of such circuit techniques is the central objective of this research.

Finally, the EEC should transfer the extracted energy to the end-load in the desired form and with minimal intermediate parasitic energy losses. To summarize, EEC for TENG provides rectification, sets the per-cycle transduced energy, and transfers the extracted energy to the load; hence, the design of an optimal EEC is an important aspect of TENG-based energy harvesting.

1.3 Research Objectives

A large attention of the TENG community is on approaches to enhance TENG's energy output by proposing device-specific changes such as increasing the triboelectric surface charge density by using different materials and surface modifications or structures to increase the effective area [26]. However, this work takes a generalized non-device-specific improvement approach of developing advanced synchronous switched (interface) energy extraction circuits that use the switching action to adjust the charge drawn on the TENG electrodes in sync with the TENG operation, setting the electrostatic damping so as to enhance the net work done against it by the mechanical source in the form of transduced electrical energy beyond that achieved through the standard-FWR circuit.

In this context, the objectives of this research are enumerated below,

1. The primary goal is the design of optimal Energy Extraction Circuits (EECs) that maximize the energy extracted from any given TENG.
2. Develop mathematical models of different EEC candidates in a common analytical platform to bring forward their pros versus cons over each other under different input and load conditions.

3. From the engineering point of view, the aim is to generate design guidelines for a universally-optimal EEC as in a plug-and-play solution that is compatible with any given TENG and self-tunes to maintain optimal energy output under varying (input) ambient environmental conditions.

1.4 Dissertation Overview and Structure

Having motivated the motion energy harvesting using TENG and stating the requirement of an Energy Extraction Circuit (EEC) for interfacing TENG with an IoT system to charge its onboard storage, here the structure and an upper-level overview of the dissertation are provided.

This dissertation compiles the following journal publications as chapter 2 through chapter 5, and in that order,

- [J1] **M. Pathak** & R. Kumar, “Synchronous Inductor Switched Energy Extraction Circuits for Triboelectric Nanogenerator”, *IEEE Access*, Vol. 9, 2021.
- [J2] **M. Pathak** & R. Kumar, “Synchronous Pre-biasing of Triboelectric Nanogenerator for Enhanced Energy Extraction”, *IEEE Transactions on Power Electronics*, Vol. 37, Issue 10, 2022.
- [J3] **M. Pathak** & R. Kumar, “Self-propelled Pre-biased Synchronous Charge Extraction Circuit for Triboelectric Nanogenerator”, *IEEE Journal of Emerging and Selected Topics in Power Electronics*, Early Access, 2022.
- [J4] **M. Pathak**, S. Xie, C. Huang, & R. Kumar, “High-Voltage Triboelectric Energy Harvesting using Multi-Shot Energy Extraction in 70V BCD Process”, *IEEE Transactions on Circuits and Systems II: Express Briefs*, Vol. 69, Issue 5, 2022.

This dissertation introduces, studies, and compares multiple novel circuit architectures as an EEC candidate for TENG. The shared idea among all the newly introduced EEC architectures here is the use of *synchronous switched inductor/s* for manipulating/conditioning the charge on

the TENG capacitor and subsequently boosting the per-cycle transduced energy. Here, the synchronous operation refers to enabling (switching) the inductor at the TENG operation extremes (TENG plates in contact vs. fully separated) and additionally at (if any) set intermediate safety triggers to avoid circuit components' voltage-breakdown.

Chapter 2 presents the first set of EEC candidates, namely Parallel and Series Synchronous Switched Harvesting on Inductor (P-SSHI and S-SSHI) circuits from our work [45]/[J1], that is an extended version of our earlier work [47] that introduced the use of SSHI circuits as TENG EEC for the first time in literature. First, the mathematical models of P-SSHI and S-SSHI circuits with general TENG electrical parameters and first-order circuit non-idealities are developed to derive the closed-form equation for the energy delivered to the battery load and compare it with the standard FWR (a 3rd circuit) in a common analytical framework. Further, the per-cycle energy output of all the three considered circuits are found to be quadratic functions of the load voltage and their corresponding optimal value of battery load at which output is maximized (also referred to as MPP: Maximum Power Point) and the upper bound beyond which charging is not feasible are derived as a function of the TENG electrical parameters for each of the circuits. Next, the derived analytical results are verified against PSpice-based simulation results as well as the experimentally measured values. Using an experimental TENG for circuit validation, SSHI circuits are measured and showed up to 8.5 fold per-cycle energy gain over the optimal (MPP operated) FWR circuit.

Thus, the SSHI circuits achieve the objective of boosting the energy output beyond the FWR circuit; however, in practice, their optimal operation over time-varying mechanical input conditions (changing TENG electrical parameters) requires a second-stage DC-DC converter with a closed-loop Maximum Power Point Tracking (MPPT) circuit for maintaining the optimal load voltage. The added MPPT circuit increases cost/complexity, and its overhead power consumption reduces the net output.

Chapter 3 presents our work [48]/[J2], built on top of our preliminary work reported in [49] studies the Synchronous Charge Extraction (SCE) circuit, used earlier in piezoelectric context

and introduced for TENG in [50, 51]. SCE circuit uses a flyback transformer to decouple the source from the load and achieve load-agnostic energy output, as in providing constant per-cycle transduced energy irrespective of the load voltage, eliminating the need for MPPT. The operation of SCE circuit with a TENG is analyzed in a generalized setting to derive the per-cycle energy output of the SCE circuit and is shown to exceed that of the optimal FWR. In the same work, we propose the use of pre-biased SCE (pSCE) architecture for TENG that adds an operation step of synchronously pre-charging (pre-biasing) the TENG using the load-battery itself at each of the TENG operation extreme (TENG plates in contact and fully separated), to enhance the net transduced energy beyond that of the SCE circuit. The per-cycle energy output of the proposed pSCE circuit is derived analytically and shown to always exceed the SCE output. A control circuit for enabling synchronous inductor switching for both pre-biasing and energy extraction is developed and is experimentally implemented using discrete components over a Printed Circuit Board (PCB). The measured results provide validation, showcasing the pSCE circuit's per-cycle energy gains up to 6.65 times over the standard FWR and up to 2.12 times over the SCE circuit.

The SCE and pSCE circuits provide a significant energy gain over the standard FWR and are free from the MPPT requirement. A drawback of these circuits is their complex control. For example, pSCE circuit's each of the five switches (implemented with MOSFETs) requires a synchronous gate control pulse with a specific on-time period decided by the TENG operation parameters resulting in an elaborate control circuit with thirteen active (power consuming) components and still requires TENG-specific manual tuning; while, auto-tuned switching can be achieved with this approach, but will require further addition of active components, increasing the complexity and the overhead power consumption.

Chapter 4 introduces a novel self-propelled pre-biased SCE (spSCE) circuit architecture [52]/[J3] for TENG that retains the synchronous pre-biasing trait of the pSCE circuit for high energy-output, while achieving plug-and-play operation as in self-tuned switching for any TENG operating under any ambient vibration. Another advantage of the spSCE circuit is its simple low-power consumption control circuit with only one active component (a comparator).

Additionally, the pre-biasing level in the proposed spSCE can be any multiple of the load battery, whereas, in pSCE, it was limited to be twice the load battery. Here too, as with the other introduced circuits, the spSCE circuit is theoretically analyzed, per-cycle energy output and upper bound on load voltage beyond which spSCE action is not feasible are derived, and finally implemented over PCB and tested using an experimental TENG. The spSCE's self-tuned yet low-power control circuit is measured to consume 4.3 times lower power than the pSCE circuit, validating the proposed approach.

Shifting gears, moving from discrete component circuit design, chapter 5 presents our on-chip designed EEC for TENG [53]/[J4]. To date, very few Integrated Circuits (ICs) have been reported in the literature as EECs for TENG, primarily due to the ultra-high-voltage nature of the TENG, and we address this challenge here by introducing a novel technique that extracts energy in multiple discrete steps to regulate the TENG voltage below the breakdown limit of the technology (70 V in this case), making it suitable for the IC implementation. The developed circuit architecture for this technique is termed ‘Multi-Shot Synchronous Charge Extraction (MS-SCE)’ and is implemented in TSMC 0.18 μ m 70 V BCD process. MS-SCE is shown to provide a constant level of transduced power, regardless of the load-voltage, i.e., MPPT-free operation using only a single switched inductor in contrast to SCE, pSCE, and spSCE circuits that are MPPT-free but requires two or more inductors, saving space/cost. Further, MS-SCE is mathematically shown to maintain higher gain over the optimal standard FWR even as the external vibration condition (accordingly, the TENG parameters) changes, proving it to be a universally-optimized EEC, suitable for real-world applications. The MS-SCE's block-by-block implementation is discussed, and the simulation results using test TENG parameters provide validation by showing 1.91 times per-cycle energy gain over even an ideal optimal FWR (gain will be higher with respect to a real FWR implementation).

Towards the end, Chapter 6 summarizes the key contribution of all the presented works [45, 47, 48, 49, 52, 53] and discusses the future research directions towards enabling wide-scale adoption of TENG powered IoTs.

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CHAPTER 2. SYNCHRONOUS INDUCTOR SWITCHED ENERGY EXTRACTION CIRCUITS FOR TRIBOELECTRIC NANOGENERATOR

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2.1 Abstract

Triboelectric nanogenerator (TENG), a class of mechanical to electrical energy transducers, has emerged as a promising solution to self-power Internet of Things (IoT) sensors, wearable electronics, etc. The use of synchronous switched energy extraction circuits (EECs) as an interface between TENG and battery load can deliver multi-fold energy gain over simple-minded Full Wave Rectification (FWR). This paper presents a detailed analysis of Parallel and Series Synchronous Switched Harvesting on Inductor (P-SSHI and S-SSHI) EECs to derive the energy delivered to the battery load and compare it with the standard FWR (a 3rd circuit) in a common analytical framework, under both realistic conditions, and also ideal conditions. Further, the optimal value of battery load to maximize output and upper bound beyond which charging is not feasible are derived for all the three considered circuits. These closed-form results derived with general TENG electrical parameters and first-order circuit non-idealities shed light on the physics of the modeling and guide the choice and design of EECs for any given TENG. The derived analytical results are verified against PSpice based simulation results as well as the experimentally measured values. In our experiments, P-SSHI and S-SSHI circuits are found to provide 1.18 and 8.59 fold per-cycle energy gain over the standard FWR circuit at 15 V battery load, respectively.

2.2 Introduction

One of the major challenges faced by today’s ever-expanding field of mobile electronics, Internet of Things (IoT), implantables, and wearable electronics is limited onboard battery lifetime. Placing a high capacity battery presents the demerits of increased size, weight, maintenance, and cost. Hence, recent years have seen a tremendous interest in integrating a miniaturized energy harvester to increase the battery life by scavenging the ambient energy [1]. Many potential sources of energy are available in the environment, such as mechanical, solar, thermal, and chemical [2, 3, 4, 5]. Among these, tapping the mechanical energy in the form of ambient vibration, human body motion, airflow, ocean currents, etc., is almost always possible. Hence, mechanical to electrical energy transducers have received significant attention both academically and commercially [6].

Recently, a new class of mechanical to electrical energy transducers termed triboelectric nanogenerators (TENGs) based on the conjugation of friction-induced electrification with electrostatic induction as its working principle have been developed [7]. A major advantage of TENG is that almost all materials have triboelectric properties, offering the flexibility of design, fabrication, and operation mode to suit the application [8]. TENG based on low-cost paper, stretchable interwoven threads, printed circuit board (PCB), and environmentally degradable materials are some of the many examples, demonstrating the versatility of TENG [9, 10, 11, 12]. TENGs have been employed in terms of application, ranging from harnessing heartbeat vibration for implantables to ocean wave motions for large-scale energy harvesting [13, 14].

There remain engineering and technical challenges, e.g., integrating TENG with electronic devices for practical applications, optimal design of transducer, and energy extraction: A critical issue arises from the fact that TENG’s output harnessing energy from environment with fluctuating movement is non-D.C. and random. Hence, it needs to be “rectified” to a stable positive form to be able to charge an on-board battery or capacitor. Also, TENGs are capacitive in nature with high inherent impedance, which might be fixed or non-linearly varying based on the mode of TENG[15]. Hence, directly charging battery or capacitor with TENG will in general,

lead to a poor charging efficiency due to a severe impedance mismatch. Thus, an interface circuit referred to as Energy Extraction Circuit (EEC) is required between a TENG and energy storage (battery or capacitor).

Full Wave Rectifier (FWR) is one of the simplest EEC in terms of implementation [16, 17]. However, it has been demonstrated in the literature that higher per-cycle energy output can be achieved by more complex EEC architectures such as switched circuits [18]. Our previous work introduced synchronous switched inductor circuits as EECs for TENG, which involve switching at the TENG voltage output extrema to obtain manifold gain over the FWR output. Wherein, Parallel Synchronous Switched Harvesting on Inductor (P-SSHI), and Series Synchronous Switched Harvesting on Inductor (S-SSHI) EECs for TENG transducers were introduced for the first time to the best of our knowledge [19]. This work extends it by providing a full mathematical derivation, a complete simulation and includes additional results on hardware implementation and validation with the following contributions:

- The closed-form equations for the *per-cycle energy output* (E_{cycle}) of both the P-SSHI and S-SSHI circuits at a given battery load are derived for the first time. In addition, the *upper limit on battery load, optimal battery load, and corresponding maximum E_{cycle} for both the SSHI circuits* are also derived. Effect of TENG parameters (determined by construction and operation of the given TENG) and circuit non-idealities on the E_{cycle} have been captured in our models to guide the design of these EECs.
- Incorporation of the following critical non-idealities in the analytical model to study their adverse effect on the output energy (E_{cycle}) and also to provide a more accurate model for both the SSHI circuits:
 - Leakage charge through any off switch over a cycle and also due to other sources such as ringing transients of oscillators at switch toggle times;
 - Limited quality factor of the resonator circuits determined by parasitic resistance of inductor and the on-state resistance of switches;

- On-state voltage drop of diodes.
- Experimental implementation of FWR and both the SSHI circuits using self-propelled electronic switches with a simple control circuit comprising just one active component (a comparator).
- Validation of the presented analytical models by way of a close match with those experimentally measured and PSpice simulated E_{cycle} at different battery loads.
- Comparison of P-SSHI, S-SSHI, and the standard FWR circuit in a common framework to bring forward their respective pros and cons.

It is important to note that while these EECs have been explored previously for piezoelectric transducers [20, 21, 22], their circuit models and hence analysis are entirely different in the case of triboelectric transducers as discussed ahead, mainly owing to the fact that while the piezoelectric capacitor appears in parallel to the load and is fixed, the triboelectric capacitor appears in series and is time-varying. To deal with time-varying nature, we have innovated to carry out analysis via a smart discretization, namely, at the two extremities (plates fully contracted versus separate); no such discretization is needed in the piezoelectric case as the same set of time-invariant equations remain valid at all instances. The resulting analysis framework in the triboelectric case is much more involved and has been developed in the presented generality for the first time. Also, consequently, due to differences in the circuit model and time-variability, the same switching control circuits used in the piezoelectric setting do not work in the TENG setting. Further, in contrast to the piezoelectric energy harvester, where the P-SSHI circuit tends to outperform the S-SSHI circuit [20], we find that the converse is typically the case for triboelectric nanogenerator. The contrasting behavior primarily stems from TENG's typically high open circuit voltage (in our implementation, 188.77 V; Refer Sec. 2.5.2) compared to that of a piezoelectric harvester which is in a range of tens of volts. The *parallel* switched SSHI circuit restricts the rising TENG voltage to load battery voltage level (in order of few volts), while the

serial switched SSHI circuit allows the build-up of TENG voltage over cycles to higher values and hence better performance of the latter in case of TENGs due to this higher pre-biasing.

2.2.1 Related Works

A variety of EEC architectures have been presented in literature [18]. A Half Wave Rectifier with a diode parallel to TENG was used to increase the energy output compared to FWR at an optimized load battery voltage. Further improvement was achieved by employing Bennet's voltage doubler circuit [23]. A transformer with optimal turns ratio can be used for impedance matching; however, the transformer is efficient only in the designed narrow frequency band [24]. Synchronous switched EECs include the approach by [25] and [26] of using a logic controlled switch to extract energy from a capacitor, being charged by a FWR circuit at an optimal instant, namely at an optimal capacitor voltage determined from TENG parameters. TENGs are characterized by high voltage and low transferred charge (or current). To address this condition, [27] presented a mechanically triggered extrema-seeking series-parallel switched capacitor scheme that reduces output voltage and increases charge in corresponding proportion. Also, a mechanically triggered parallel switch to short the TENG at the extrema was used in [17] to improve the efficiency and increase saturation voltage for capacitor load. Another approach is using a synchronous serial switch to extract energy from the TENG capacitor at the extrema. This extracted energy can then be transferred to the DC load with high efficiency by using a buck converter as shown by [28] or using coupled inductors (flyback converter) as demonstrated by [29] and [30]. Another example of a switched EEC is the use of Maximum Power Point Tracking (MPPT) for TENG executed using dual-input buck converter over a compact integrated circuit (IC) [31].

[32] recently described the P-SSHI circuit's implementation as an IC. For the first time, our work provides the analytical models for P-SSHI and S-SSHI circuits to help guide the EEC design, such as determining optimal load voltage to maximize energy extraction. [33] designed the P-SSHI circuit for a TENG paired with a parallel capacitor that provides an additional degree of controlling the variation between max to min capacitance ratio. In contrast, our work deals with

both P-SSHI and S-SSHI circuits in a fully generalized setting and also provides closed-form E_{cycle} equations. [34] demonstrated P-SSHI and S-SSHI circuits for a resistive load, one that does not need rectification, using mechanical switches. In contrast, our work studies both the SSHI circuits for varying battery loads commonly encountered in the practical IoT applications; uses convenient automated electronic switches for physical implementation, and demonstrates the desired match between the experimental, simulated, and the derived analytical E_{cycle} results.

2.2.2 Comments about Analysis Methodology

For the different EECs (FWR, P-SSHI, S-SSHI), we derive the per-cycle energy delivered to a battery load rather than the instantaneous output power since the vibration frequency can vary, affecting the power but not the per-cycle energy. A battery load is selected for analysis (as opposed to a resistive or capacitive load) since most frequently, there is an onboard battery for IoT, wearables and, other mobile electronic devices, and the harvester's role is to supplement their energy and extend the lifetime. The use of battery load as opposed to resistive load introduces additional complexity of rectification that our EECs also incorporate. The analytical derivations additionally include the computation of the optimal value of the battery load to maximize output and upper bound beyond which the charging becomes infeasible, providing additional insights into the 3 EECs.

Our analytical derivations and experimental verification are provided for the most generalized case: "Contact-Separation" mode TENGs, in which the internal capacitance varies with time so that the ratio of maximum to minimum TENG capacitances $\beta \geq 1$. This general class also includes Lateral Sliding and Single Electrode Contact mode TENGs. In contrast, the Sliding Freestanding and Contact Freestanding mode TENGs, having fixed internal capacitance ($\beta = 1$)[15], are a special case and can be derived by equating the maximum and minimum capacitances ($C_{T,\text{max}}$ and $C_{T,\text{min}}$) of our framework.

Both the SSHI circuits operate with an external inductor, connected briefly at the TENG operation extremes to form a LC oscillator along with the TENG capacitor. For accurate

modeling, we carefully consider the quality factor of this oscillator emanating from the non-idealities: parasitic series resistance of inductor (R_L) as well as the on-state resistance (R_{on}) of the switch. Additionally, the leakage charge (Q_L) through the off switches and during the oscillator ringing transients over an operation cycle is also included in our mathematical modeling. Further, the diode's on-state voltage drop (V_D) is the third analytically modeled non-ideality in our setup.

2.3 TENG Circuit Model

Here we summarize a 1st-order lumped circuit model for Contact-Separation mode TENG [35]. Fig. 2.1(a) shows the structure of TENG used for experimental validation of the circuit analysis in this study.

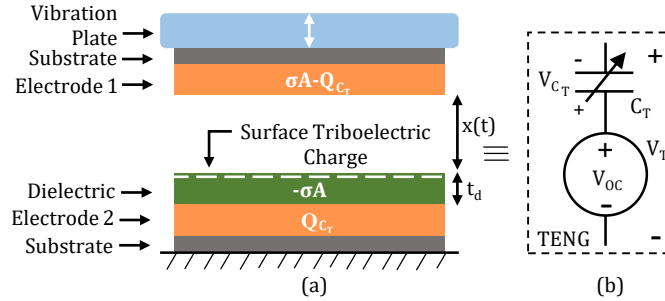


Figure 2.1 A contact-separation TENG's (a) cross section schematic and (b) equivalent circuit model.

It consists of a parallel plate variable capacitor with horizontal Aluminum plate electrodes (in orange). The top electrode attached to a vibrating platform can move vertically, making contact and separation with the fixed bottom electrode with a dielectric (Teflon) layer laid over its upper face. The plates have an area A and develop a charge with density σ when the two triboelectrics, Aluminum on top vs. Teflon on the bottom, come into repeated contact. Due to Aluminium vs. Teflon's triboelectric properties, the top plate is positively charged while the bottom plate is negatively charged. It can be reasonably assumed that the triboelectric charges ($-\sigma A$) generated on the bottom plate's dielectric layer are evenly distributed, close to the upper surface. When

connected to a circuit, the two plates of the TENG will draw/supply charge from/to the circuit due to the electric field of the triboelectric charges. Letting $Q_{CT}(t)$ denote the corresponding charge drawn on the bottom electrode of the TENG at time t , the total charge on the bottom structure at time t is $(Q_{CT}(t) - \sigma A)$, and by charge conservation, the top plate will have $(\sigma A - Q_C(t))$ charge at time t .

Using Gauss law of electrostatics, under infinite parallel plate approximation (no fringing field), the electric fields in the dielectric and air regions of the structure are given by:

$$E_d = \frac{Q_{CT}(t)}{\epsilon_0 \epsilon_d A}; \quad E_a = \frac{Q_{CT}(t) - \sigma A}{\epsilon_0 A}, \quad (2.1)$$

where ϵ_0 is the electrical permittivity of air, and ϵ_d is the relative dielectric constant of the Teflon dielectric layer. Denoting the thicknesses of the dielectric and air-gap as $t_d, x(t)$, respectively, the voltage across the two electrodes of TENG can be calculated using the Poisson's equation, as below:

$$V_T(t) = - \int_0^{t_d} E_d dx - \int_{t_d}^{x(t)+t_d} E_a dx \quad (2.2)$$

Inserting (2.1) in (2.2), the voltage across TENG can be written as:

$$V_T(t) = \frac{\sigma x(t)}{\epsilon_0} - \frac{Q_{CT}(t) \left(x(t) + \frac{t_d}{\epsilon_d} \right)}{\epsilon_0 A} \quad (2.3)$$

From (2.3), we can arrive at the lumped element circuit model of the “contact-separation mode TENG” shown in Fig. 2.1(b):

$$V_T(t) = V_{oc}(t) - \frac{Q_{CT}(t)}{C_T(t)} = V_{oc}(t) - V_{CT}(t), \text{ with} \quad (2.4)$$

$$V_{oc}(t) := \frac{\sigma x(t)}{\epsilon_0} \quad (2.5)$$

$$C_T(t) := \frac{\epsilon_0 A}{x(t) + d_{\text{eff}}}; \quad d_{\text{eff}} := \frac{t_d}{\epsilon_d}. \quad (2.6)$$

It is clear from (2.4)-(2.6) that TENG capacitance $C_T(t)$ and voltage $V(t)$ change as the air-gap $x(t)$ varies.

For the analysis purposes, we take $x(t)$ to be varying with period T , with minimum value 0 (when the top plate is fully down) and maximum value x_{max} (when the top plate is fully up).

Then at each integer multiple of the period ($t = nT$), the two plates are in contact ($x(t) = 0$), whereas at the corresponding half-period later ($t = (n + \frac{1}{2})T$), the two plates are maximally separated ($x(t) = x_{\max}$). Accordingly, there are two extreme states of the TENG operation:

- State I: $t = nT, x(t) = 0, C_T(t) = C_{T,\max} := \frac{\epsilon_0 A}{d_{\text{eff}}}, V_{\text{oc}}(t) = 0$;
- State II: $t = (n + \frac{1}{2})T, x(t) = x_{\max}, C_T(t) = C_{T,\min} := \frac{\epsilon_0 A}{x_{\max} + d_{\text{eff}}}, V_{\text{oc}}(t) = V_{\text{oc},\max} := \frac{\sigma x_{\max}}{\epsilon_0}$.

The voltage and capacitor values at these extreme states, namely, maximum open circuit voltage ($V_{\text{oc},\max}$), minimum TENG capacitance ($C_{T,\min}$), and maximum TENG capacitance ($C_{T,\max}$) constitute the TENG parameters that influence the energy output of the EECs. A convenient useful term in subsequent analysis is the ratio of the capacitances at the two extremes:

$$\beta := \frac{C_{T,\max}}{C_{T,\min}}.$$

2.4 Analysis of Energy Extraction Circuits

For each of the three circuits, the general approach to derive the per-cycle energy delivered to the battery load (E_{cycle}) is to track the TENG voltage at States I and II of the circuit operation. Since the capacitances at States I and II ($C_{T,\min}$ and $C_{T,\max}$) are known, the corresponding charge on the TENG capacitor (Q_{C_T}) can then be found using the TENG equation (2.4). By the law of conservation of charge, the change in the TENG capacitor charge over a cycle determines the charge flowing through the battery load and hence the delivered per-cycle energy is simply a value scaled by the battery value. Thus, the following analysis and results are purely dependent on the two extrema states mentioned above and independent of the TENG motion path to get to those two extrema. In other words, for a given extraction circuit, E_{cycle} is dependent on the separation at maxima ($x_{\max}$ and the corresponding $V_{\text{oc},\max}$) and not on the path, $x(t)$.

2.4.1 Full wave rectifier (FWR)

For a FWR, its battery charging process can be understood by following the voltage waveform shown in Fig. 2.3.

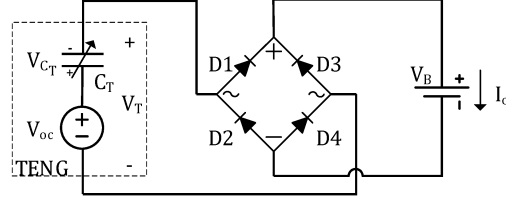
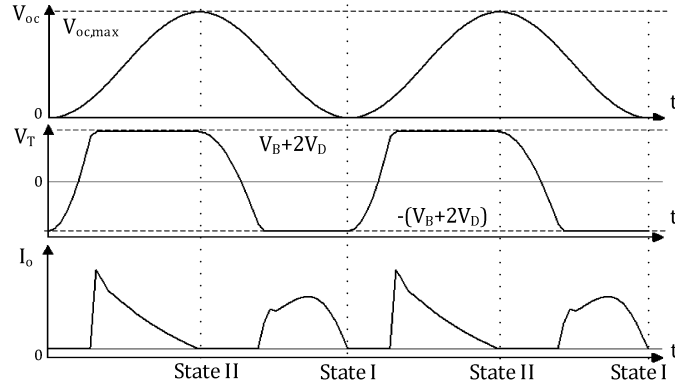


Figure 2.2 Full Wave Rectifier (FWR) circuit

Figure 2.3 Typical open circuit voltage: $V_{oc}(t)$, FWR circuit TENG voltage: $V_T(t)$ and output current: $I_o(t)$ plots.

The system starts at State I, and initially, the TENG capacitor has zero charge, and the TENG open circuit voltage is also zero. As the two plates separate, the open circuit voltage increases (linearly with separation, see (2.5)). The battery charging commences at the time when the TENG open circuit voltage exceeds the battery voltage by two diode drops ($V_{oc}(t) \geq V_B + 2V_D$), and from that point on, the TENG voltage remains clamped to that same value, while the TENG capacitor accumulates charge equivalent to the difference $V_{oc}(t) - (V_B + 2V_D)$ until State II is reached. This completes the first-half-cycle. As the second-half-cycle begins, V_{oc} starts to drop, causing the overall TENG voltage to fall below the threshold $V_B + 2V_D$ and the conduction stops. Battery no longer charges, and capacitor retains its charge to the level at State II, until the time when a dual situation arises, namely, the absolute TENG voltage reaches $|V_T(t)| \geq V_B + 2V_D$ and gets clamped at that value till State I is reached, thus completing one full cycle (Refer Fig. 2.3).

2.4.1.1 Per-cycle energy output

The energy delivered to the load battery in each cycle denoted E_{cycle} , is the product of the battery voltage (V_B) and the total charge flowing through it in that cycle (ΔQ_{cycle}). From the charge conservation, this total charge flowing through the battery equals the change in the TENG capacitor charge in the two half-cycles, $\Delta Q_{\text{cycle}} = |\Delta Q_{C_T}^{\text{I} \rightarrow \text{II}}| + |\Delta Q_{C_T}^{\text{II} \rightarrow \text{I}}|$.

By using (2.4), the voltage and the charge on the TENG capacitor at the two states, denoted $V_T^{\text{I}}, Q_{C_T}^{\text{I}}, V_T^{\text{II}}, Q_{C_T}^{\text{II}}$, can be written as follows:

$$V_T^{\text{I}} = -\frac{Q_{C_T}^{\text{I}}}{C_{T,\text{max}}} = -(V_B + 2V_D) \Rightarrow Q_{C_T}^{\text{I}} = C_{T,\text{max}}(V_B + 2V_D) \quad (2.7)$$

$$V_T^{\text{II}} = V_{\text{oc,max}} - \frac{Q_{C_T}^{\text{II}}}{C_{T,\text{min}}} = (V_B + 2V_D) \Rightarrow Q_{C_T}^{\text{II}} = C_{T,\text{min}}(V_{\text{oc,max}} - V_B - 2V_D) \quad (2.8)$$

It follows that, It follows that,

$$\begin{aligned} |\Delta Q^{\text{I} \rightarrow \text{II}}| &= |Q_{C_T}^{\text{I}} - Q_{C_T}^{\text{II}}| \\ &= C_{T,\text{min}}V_{\text{oc,max}} - (C_{T,\text{min}} + C_{T,\text{max}})(V_B + 2V_D) \\ &= |\Delta Q^{\text{II} \rightarrow \text{I}}| = |Q_{C_T}^{\text{II}} - Q_{C_T}^{\text{I}}|. \end{aligned}$$

Since this same change in charge flows through the load battery in the respective half-cycles, the energy that the battery gains during one cycle is given by twice this change in charge times the battery voltage:

$$E_{\text{cycle}} = 2V_B C_{T,\text{min}} [V_{\text{oc,max}} - (1 + \beta)(V_B + 2V_D)]. \quad (2.9)$$

2.4.1.2 Optimal battery load

From (2.9), E_{cycle} is a quadratic function of V_B , and it can be maximized with respect to V_B by differentiating (2.9) and setting it to zero, to yield the optimal battery load V_B^* and the optimal per-cycle energy, E_{cycle}^* :

$$\begin{aligned} V_B^* &= \frac{V_{\text{oc,max}}}{2(1 + \beta)} - V_D; \\ E_{\text{cycle}}^* &= \frac{C_{T,\text{min}} V_{\text{oc,max}}^2}{2(1 + \beta)} - 2C_{T,\text{min}} V_D [V_{\text{oc,max}} - (1 + \beta)V_D]. \end{aligned} \quad (2.10)$$

2.4.1.3 Upper bound to battery load

In order for the load battery to charge, certain conditions must hold. In particular, for the charging in the first-half-cycle to commence, the maximum achievable voltage must exceed the upper threshold voltage needed for charging:

$$V_{\text{oc,max}} \geq V_B + 2V_D.$$

Similarly, for the charging in the second-half-cycle to occur, the minimum achievable voltage must fall below the lower threshold voltage required for charging:

$$-V_{C_T}^{\text{I}} \leq -(V_B + 2V_D).$$

Combining the two cases, it follows that for charging in both half-cycles, the following should hold:

$$\min\{V_{\text{oc,max}}, V_{C_T}^{\text{I}}\} \geq V_B + 2V_D. \quad (2.11)$$

Once the first-half-cycle completes, the TENG capacitor acquires a voltage of

$V_{\text{oc,max}} - (V_B + 2V_D)$, and in the extreme case (corresponding to the upper bound battery load, where the conduction will occur just at the end of the second-half-cycle, i.e., at State I), the conduction ceases until State I, preserving the capacitor charge at:

$$Q_{C_T}^{\text{I}} = Q_{C_T}^{\text{II}} = C_{T,\min} [V_{\text{oc,max}} - (V_B + 2V_D)].$$

So,

$$V_{C_T}^{\text{I}} = \frac{Q_{C_T}^{\text{I}}}{C_{T,\max}} = \frac{Q_{C_T}^{\text{II}}}{C_{T,\max}} = \frac{C_{T,\min} [V_{\text{oc,max}} - (V_B + 2V_D)]}{C_{T,\max}} = \frac{[V_{\text{oc,max}} - (V_B + 2V_D)]}{\beta} < V_{\text{oc,max}}. \quad (2.12)$$

Now since $V_{C_T}^{\text{I}} < V_{\text{oc,max}}$, (2.11) simplifies to:

$$V_{C_T}^{\text{I}} \geq V_B + 2V_D \Leftrightarrow \frac{[V_{\text{oc,max}} - (V_B + 2V_D)]}{\beta} \geq V_B + 2V_D \Leftrightarrow V_B \leq \frac{V_{\text{oc,max}}}{\beta + 1} - 2V_D. \quad (2.13)$$

The last condition provides an upper bound to the load battery voltage for it to charge in the FWR extraction circuit. As expected of a quadratic function, it is double the optimal battery value.

2.4.2 Parallel Synchronous Switched Harvesting on Inductor (P-SSHI)

P-SSHI circuit is shown in Fig. 2.4. Compared to FWR, it has an added parallel path with a switch and an inductor. The parallel switch S is closed at States I and II for half the $L - C_T$ resonator time period, which flips TENG voltage polarity as apparent from the waveform plot in Fig. 2.5.

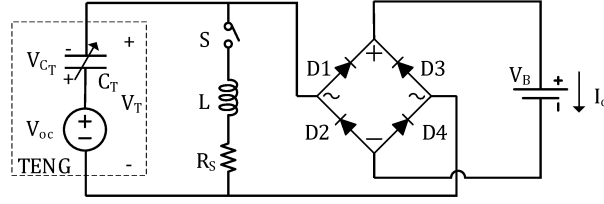


Figure 2.4 Parallel Synchronous Switched Harvesting on Inductor (P-SSHI) circuit

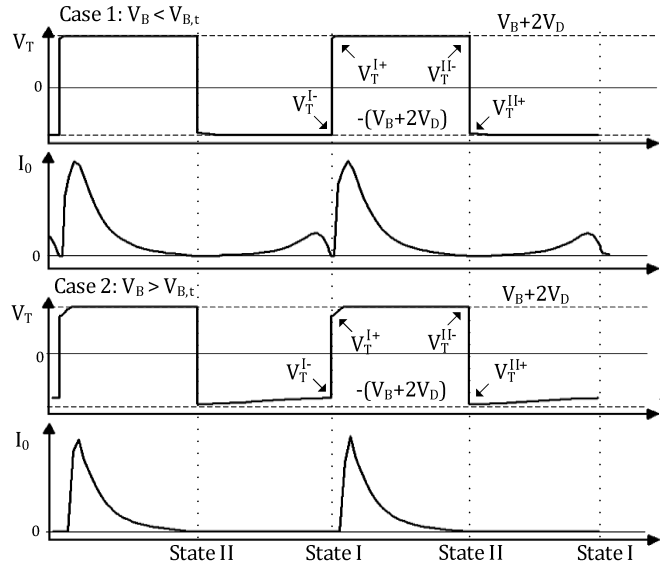


Figure 2.5 Typical P-SSHI circuit TENG voltage: $V_T(t)$ and output current: $I_o(t)$ plots.

This instant inversion increases the load charging duration (compared to the FWR circuit) in the following half-cycle. The voltage inversion is imperfect owing to the limited quality factor of the $L - C_T$ resonator due to the presence of switch on-state resistance (R_{on}) and the inductor parasitic resistance (R_L). Together those are modeled as R_S in the following derivation of the

per-cycle energy output (E_{cycle}). During the switch off states, the charging occurs similar to the FWR circuit with one difference: the TENG capacitor charge partly leaks through the parallel path of $S - L - R_s$ due to the finite off-state resistance (R_{off}) of the switch. Since the TENG voltage polarity and value, which dictate the extent of charge leakage, in the first-half-cycle (separation of plates) and the second-half-cycle (retraction of plates) are asymmetric, the corresponding leakage terms are also different, denoted Q_L^{I} and Q_L^{II} respectively in the following derivation.

2.4.2.1 P-SSHI circuit analysis at States I and II

For the sake of analytical convenience, we introduce four sets of notation for the pre and post switching TENG voltage ($V_T(t)$), TENG capacitor charge ($Q_{C_T}(t)$) and its voltage ($V_{C_T}(t)$) at States I and II:

- State I- $\xrightarrow{T_{\text{on}}^{\text{I}}}$ State I+ : $(V_T^{\text{I-}}, Q_{C_T}^{\text{I-}}, V_{C_T}^{\text{I-}}) \xrightarrow{T_{\text{on}}^{\text{I}}} (V_T^{\text{I+}}, Q_{C_T}^{\text{I+}}, V_{C_T}^{\text{I+}})$
- State II- $\xrightarrow{T_{\text{on}}^{\text{II}}}$ State II+ : $(V_T^{\text{II-}}, Q_{C_T}^{\text{II-}}, V_{C_T}^{\text{II-}}) \xrightarrow{T_{\text{on}}^{\text{II}}} (V_T^{\text{II+}}, Q_{C_T}^{\text{II+}}, V_{C_T}^{\text{II+}})$

Here, T_{on}^{I} and $T_{\text{on}}^{\text{II}}$ denote the switching periods at States I and II, respectively, and equal the corresponding half the $L - C_T$ resonator cycle time period. Those are designed to be small compared to the vibration cycle period (T); hence we can approximate the TENG capacitance $C_T(t)$ and open circuit voltage $V_{\text{oc}}(t)$ to be constant over the switching period.

At State II, the P-SSHI circuit can be simplified to that in Fig. 2.6(b). We analyze it first to obtain the relation between pre and post switching TENG voltages and charges.

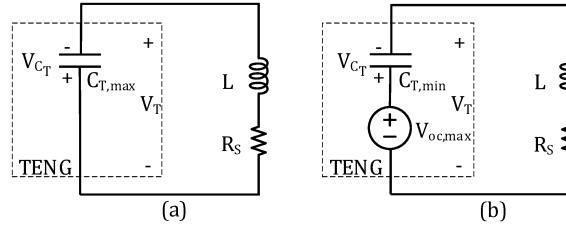


Figure 2.6 Simplified P-SSHI circuits at States (a) I and (b) II.

The differential equation for this resonator loop obtained using KVL is given by:

$$\frac{d^2 V_{C_T}(t)}{dt^2} + \frac{R_S}{L} \frac{dV_{C_T}(t)}{dt} + \frac{V_{C_T}(t)}{LC_{T,\min}} - \frac{V_{\text{oc,max}}}{LC_{T,\min}} = 0.$$

This can be solved for TENG capacitor voltage $V_{C_T}(t)$ with initial condition as $V_{C_T}(0) = V_{C_T}^{\text{II}-}$ to obtain:

$$V_{C_T}(t) = e^{-\frac{R_S t}{2L}} (V_{C_T}^{\text{II}-} - V_{\text{oc,max}}) \left(\cos(\omega_d^{\text{II}} t) + \frac{R_S}{2L\omega_d^{\text{II}}} \sin(\omega_d^{\text{II}} t) \right) + V_{\text{oc,max}}, \quad (2.14)$$

where ω_d^{II} is the resonance frequency given by,

$$\omega_d^{\text{II}} := \sqrt{\frac{1}{LC_{T,\min}} - \frac{R_S^2}{4L^2}}. \quad (2.15)$$

Switch is kept “on” for half the resonant time period ($T_{\text{on}}^{\text{II}} = \frac{\pi}{\omega_d^{\text{II}}}$). Hence,

$$V_{C_T}^{\text{II}+} = V_{C_T} \left(\frac{\pi}{\omega_d^{\text{II}}} \right) = -\alpha^{\text{II}} V_{C_T}^{\text{II}-} + (1 + \alpha^{\text{II}}) V_{\text{oc,max}}, \quad (2.16)$$

with

$$\alpha^{\text{II}} := e^{\frac{-\pi R_S}{2\omega_d^{\text{II}} L}} = e^{\frac{-\pi}{2Q_f^{\text{II}}}}, \text{ and } Q_f^{\text{II}} := \frac{\omega_d^{\text{II}} L}{R_S}. \quad (2.17)$$

Here, Q_f^{II} is the series resonator quality factor at State II, and $0 < \alpha^{\text{II}} < 1$ is its “normalized” form.

The TENG voltage at the end of switching period ($V_T^{\text{II}+}$) can then be obtained from (2.16) and the TENG equation (2.4):

$$V_T^{\text{II}+} = V_{\text{oc,max}} - V_{C_T}^{\text{II}+} = -\alpha^{\text{II}} V_T^{\text{II}-}. \quad (2.18)$$

Thus, the normalized quality factor, α^{II} captures the reduction in the voltage swing (flip) at State II due to the circuit’s series parasitic resistance (R_S). On the other hand, during the switching at State I, the P-SSHI circuit is simplified to as shown in Fig. 2.6(a). Following the same process as above, we obtain:

$$V_T^{\text{I}+} = -V_{C_T}^{\text{I}+} = -\alpha^{\text{I}} V_T^{\text{I}-}, \text{ where} \quad (2.19)$$

$$\alpha^{\text{I}} := e^{\frac{-\pi R_S}{2\omega_d^{\text{I}} L}} = e^{\frac{-\pi}{2Q_f^{\text{I}}}}; \quad Q_f^{\text{I}} := \frac{\omega_d^{\text{I}} L}{R_S}; \quad (2.20)$$

$$\omega_d^{\text{I}} := \sqrt{\frac{1}{LC_{T,\max}} - \frac{R_S^2}{4L^2}}. \quad (2.21)$$

Note that the resonance frequency (2.21) and the normalized quality factor (4.37) have changed from that in State II, since the TENG capacitor value has changed to $C_{T,\max}$ from $C_{T,\min}$.

2.4.2.2 Per-cycle energy output

Equations (2.18) and (2.19) related the post-switching TENG voltages to their pre-switching values at the States II and I, respectively. Next, we derive the values for the pre-switching TENG voltages at the two States to complete the characterization. This also allows us to then characterize the per-cycle energy output. As noted in the waveform plot (Fig. 2.5), similar to the FWR circuit, the TENG voltage is clamped at $V_B + 2V_D$ during the charging phase in the first-half-cycle until the time State II is reached, which is when a charge reversal due to the switch closure occurs (for $T_{\text{on}}^{\text{II}}$ duration). Thus,

$$V_T^{\text{II}-} = V_{\text{oc},\max} - \frac{Q_{C_T}^{\text{II}-}}{C_{T,\min}} = V_B + 2V_D \Rightarrow Q_{C_T}^{\text{II}-} = C_{T,\min}(V_{\text{oc},\max} - V_B - 2V_D). \quad (2.22)$$

Post switching at State II, using (2.18), we obtain,

$$V_T^{\text{II}+} = V_{\text{oc},\max} - \frac{Q_{C_T}^{\text{II}+}}{C_{T,\min}} = -\alpha^{\text{II}}(V_B + 2V_D) \Rightarrow Q_{C_T}^{\text{II}+} = C_{T,\min} [V_{\text{oc},\max} + \alpha^{\text{II}}(V_B + 2V_D)]. \quad (2.23)$$

In the second-half-cycle, there are two possibilities, either the TENG voltage reaches the lower threshold voltage, $-(V_B + 2V_D)$ for charging of load to occur (Fig. 2.5 Case 1) or the battery load is high enough to resist any current flow up to subsequent State I (Fig. 2.5 Case 2). It is necessary to differentiate the two cases in order to obtain energy output, E_{cycle} which is different for the two cases.

The “transition” load value, $V_{B,t}$ separating these two cases can be derived from the limiting case of no conduction in the second-half-cycle and TENG Voltage at State I ($V_T^{\text{I}-}$) just reaching the lower threshold, $-(V_{B,t} + 2V_D)$, i.e.,

$$V_T^{\text{I}-} = -\frac{Q_{C_T}^{\text{I}-}}{C_{T,\max}} = -(V_{B,t} + 2V_D). \quad (2.24)$$

Under the condition of no current flow through load in the second-half-cycle, considering leakage, $Q_{C_T}^{\text{I}-} = Q_{C_T}^{\text{II}+} - |Q_L^{\text{II}}|$. Then, inserting the value of $Q_{C_T}^{\text{II}+}$ from (2.23) into (2.24), and

invoking the definition of β , we arrive at:

$$V_{B,t} = \frac{V_{oc,max}}{\beta - \alpha^{II}} - 2V_D - \frac{|Q_L^{II}|}{(\beta - \alpha^{II})C_{T,min}}. \quad (2.25)$$

Case 1: $V_B < V_{B,t}$: Here, TENG conducts in the second-half-cycle, and hence, the TENG voltage is clamped to $-(V_B + 2V_D)$ until reaching State I. Hence,

$$V_T^{I-} = -\frac{Q_{C_T}^{I-}}{C_{T,max}} = -(V_B + 2V_D) \Rightarrow Q_{C_T}^{I-} = C_{T,max}(V_B + 2V_D). \quad (2.26)$$

Post switching at State I, using (2.19),

$$V_T^{I+} = -\frac{Q_{C_T}^{I+}}{C_{T,max}} = \alpha^I(V_B + 2V_D) \Rightarrow Q_{C_T}^{I+} = -\alpha^I C_{T,max}(V_B + 2V_D). \quad (2.27)$$

Current flows through the load during the switching periods at States I and II. As before, the per-cycle energy delivered to the load (E_{cycle}) is the battery load (V_B) times the charge flowing through it (ΔQ_{cycle}). The absolute difference between the TENG capacitor charge at State I after switching ($Q_{C_T}^{I+}$) and the TENG capacitor charge at State II before switching ($Q_{C_T}^{II-}$) obtained using (2.27) and (2.22), respectively, less the switch leakage charge between the above two states (Q_L^I) gives the total charge flowing through the load in the first-half-cycle,

$$|\Delta Q^{I+ \rightarrow II-}| := |Q_{C_T}^{II-} - Q_{C_T}^{I+}| - |Q_L^I| = C_{T,min} [V_{oc,max} + (\alpha^I \beta - 1)(V_B + 2V_D)] - |Q_L^I|.$$

Similarly, using (2.26) and (2.23) and taking into consideration the switch leakage charge between the States II+ and I- (Q_L^{II}), the charge flowing through the load in the second-half-cycle is given by,

$$|\Delta Q^{II+ \rightarrow I-}| := |Q_{C_T}^{I-} - Q_{C_T}^{II+}| - |Q_L^{II}| = C_{T,min} [V_{oc,max} + (\alpha^{II} - \beta)(V_B + 2V_D)] - |Q_L^{II}|.$$

Hence, $\Delta Q_{cycle} := |\Delta Q^{I+ \rightarrow II-}| + |\Delta Q^{II+ \rightarrow I-}|$ and for this case, $E_{cycle}^{C1} = V_B \Delta Q_{cycle}$, implies:

$$E_{cycle}^{C1} = V_B C_{T,min} \left[2V_{oc,max} - \left\{ (1 - \alpha^I)\beta + (1 - \alpha^{II}) \right\} (V_B + 2V_D) \right] - V_B (|Q_L^I| + |Q_L^{II}|). \quad (2.28)$$

Case 2: $V_B \geq V_{B,t}$: Here, no conduction occurs through load in the second-half-cycle, implying

$Q_{C_T}^{I-} = Q_{C_T}^{II+} - |Q_L^{II}|$. So,

$$V_T^{I-} = -\frac{Q_{C_T}^{I-}}{C_{T,max}} = -\frac{V_{oc,max} + \alpha^{II}(V_B + 2V_D)}{\beta} + \frac{|Q_L^{II}|}{C_{T,max}}$$

Post switching at State I, using (2.19), we obtain,

$$\begin{aligned} V_T^{I+} &= -\frac{Q_{C_T}^{I+}}{C_{T,\max}} = \frac{\alpha^I}{\beta} \left[V_{\text{oc,max}} + \alpha^{\text{II}}(V_B + 2V_D) \right] - \frac{\alpha^I |Q_L^{\text{II}}|}{C_{T,\max}} \\ \Rightarrow Q_{C_T}^{I+} &= -\alpha^I C_{T,\min} \left[V_{\text{oc,max}} + \alpha^{\text{II}}(V_B + 2V_D) \right] + \alpha^I |Q_L^{\text{II}}|. \end{aligned} \quad (2.29)$$

Since in this case, the charge flows through the load only in the first-half-cycle, we have

$\Delta Q_{\text{cycle}} = \left| \Delta Q^{I+ \rightarrow \text{II}-} \right|$. From (2.22), (2.29), and considering the leakage charge, Q_L^{I} , we obtain,

$$\begin{aligned} E_{\text{cycle}}^{\text{C2}} &= V_B \Delta Q_{\text{cycle}} = \left| Q_{C_T}^{\text{II}-} - Q_{C_T}^{I+} \right| - \left| Q_L^{\text{I}} \right| \\ &= V_B C_{T,\min} \left[(1 + \alpha^{\text{I}}) V_{\text{oc,max}} - (1 - \alpha^{\text{I}} \alpha^{\text{II}})(V_B + 2V_D) \right] - V_B \left(\left| Q_L^{\text{I}} \right| + \alpha^{\text{I}} |Q_L^{\text{II}}| \right). \end{aligned} \quad (2.30)$$

2.4.2.3 Optimal battery load

We first show that the optimal condition occurs in the case when, $V_B \geq V_{B,t}$. Using (2.25), we can show:

$$\begin{aligned} V_B &\geq \left\{ V_{B,t} = \frac{V_{\text{oc,max}}}{\beta - \alpha^{\text{II}}} - 2V_D - \frac{|Q_L^{\text{II}}|}{(\beta - \alpha^{\text{II}})C_{T,\min}} \right\} \\ \Leftrightarrow &(\beta - \alpha^{\text{II}})(V_B + 2V_D) - V_{\text{oc,max}} + \frac{|Q_L^{\text{II}}|}{C_{T,\min}} \geq 0. \end{aligned} \quad (2.31)$$

Also from (2.30) and (2.28), we obtain,

$$E_{\text{cycle}}^{\text{C2}} - E_{\text{cycle}}^{\text{C1}} = V_B C_{T,\min} (1 - \alpha^{\text{I}}) \left[(\beta - \alpha^{\text{II}})(V_B + 2V_D) - V_{\text{oc,max}} + \frac{|Q_L^{\text{II}}|}{C_{T,\min}} \right].$$

Employing the inequality of (2.31) into above equation, and noting that $C_{T,\min}, V_B > 0$ and

$0 < \alpha^{\text{I}}, \alpha^{\text{II}} < 1$, it follows that $E_{\text{cycle}}^{\text{C2}} - E_{\text{cycle}}^{\text{C1}} \geq 0$, implying that a larger per-cycle energy is

harvested when $V_B \geq V_{B,t}$. The optimal battery voltage (V_B^*) and the maximized per-cycle energy

(E_{cycle}^*) can then be found by analyzing this case to yield:

$$\begin{aligned}
V_B^* &= \frac{1}{2(1 - \alpha^I \alpha^{II})} \left[(1 + \alpha^I) V_{\text{oc,max}} - \frac{c}{C_{T,\min}} \right] - V_D; \\
E_{\text{cycle}}^* &= \frac{(1 + \alpha^I)^2}{4(1 - \alpha^I \alpha^{II})} (C_{T,\min} V_{\text{oc,max}}^2) - C_{T,\min} V_D \left[(1 + \alpha^I) V_{\text{oc,max}} - (1 - \alpha^I \alpha^{II}) V_D \right] \\
&\quad + \frac{c}{2(1 - \alpha^I \alpha^{II})} \left[\frac{c}{2C_{T,\min}} - (1 + \alpha^I) V_{\text{oc,max}} \right] + c V_D; \quad c = |Q_L^I| + \alpha^I |Q_L^{II}|. \quad (2.32)
\end{aligned}$$

As detailed in Sec. 2.6, the values of the non-ideality parameters (V_D , α^I , α^{II} , Q_L^I , and Q_L^{II}) change significantly over the operation range as the load battery varies, causing the currents and voltages in the circuits to change. Hence, their averaged values over the entire load operating range are used to estimate the optimal battery load and corresponding optimal energy output in the above-derived equations.

2.4.2.4 Upper bound to battery load

If the load V_B is higher than $V_{\text{oc,max}} - 2V_D - \frac{Q_L^I}{C_{T,\min}}$, there shall be transient operation cycles before the steady-state charging commences. We introduce the notation $V_{T,k}$ to denote the TENG voltage in the k th cycle. Then starting from rest, i.e., $V_{T,1}^I = 0$ and no conduction through the load in the first-half-cycle, the TENG voltage at State II is simply given by,

$$V_{T,1}^{II-} = V_{\text{oc,max}} - V_L^I; \quad V_L^I = \frac{|Q_L^I|}{C_{T,\min}}.$$

which is then followed by a voltage inversion due to the switching action, implying,

$$V_{T,1}^{II+} = -\alpha^{II}(V_{\text{oc,max}} - V_L^I).$$

Similarly, when no conduction occurs in the second-half-cycle,

$$V_{T,2}^{I-} = -\frac{(1 + \alpha^{II})}{\beta} V_{\text{oc,max}} + \frac{\alpha^{II}}{\beta} V_L^I + V_L^{II}; \quad V_L^{II} = \frac{|Q_L^{II}|}{C_{T,\max}}.$$

The voltage is flipped again at the onset of the second vibration cycle, implying,

$$\begin{aligned}
\Rightarrow V_{T,2}^{I+} &= \frac{\alpha^I(1 + \alpha^{II})}{\beta} V_{oc,max} - \frac{\alpha^I \alpha^{II}}{\beta} V_L^I - \alpha^I V_L^{II} \\
\Rightarrow V_{T,2}^{II-} &= (1 + \alpha^I + \alpha^I \alpha^{II}) V_{oc,max} - (1 + \alpha^I \alpha^{II}) V_L^I - \alpha^I \beta V_L^{II} \\
\Rightarrow V_{T,3}^{II-} &= \left[1 + \alpha^I \alpha^{II} + (\alpha^I \alpha^{II})^2 + \alpha^I (1 + \alpha^I \alpha^{II}) \right] V_{oc,max} - \left[1 + \alpha^I \alpha^{II} + (\alpha^I \alpha^{II})^2 \right] V_L^I \\
&\quad - \alpha^I (1 + \alpha^I \alpha^{II}) (\beta V_L^{II}).
\end{aligned}$$

Following the above reasoning, the maximum TENG voltage in the k^{th} cycle (at State II) can be written as a sum of geometric series with common ratio α^I, α^{II} , i.e.,

$$V_{T,k}^{II-} = \left[\frac{1 - (\alpha^I \alpha^{II})^k}{1 - \alpha^I \alpha^{II}} + \alpha^I \frac{1 - (\alpha^I \alpha^{II})^{k-1}}{1 - \alpha^I \alpha^{II}} \right] V_{oc,max} - \frac{1 - (\alpha^I \alpha^{II})^k}{1 - \alpha^I \alpha^{II}} V_L^I - \frac{1 - (\alpha^I \alpha^{II})^{k-1}}{1 - \alpha^I \alpha^{II}} (\alpha^I \beta V_L^{II}).$$

Thus, through the switching at the extremes, the TENG voltage will continue to build up until it reaches $V_B + 2V_D$, post to which charging commences and the energy output equation (E_{cycle}) derived in (2.30) yields the per-cycle harvested energy.

An upper bound to the load voltage can be derived from the extreme case where no charging occurs even as $k \rightarrow \infty$ and with $\alpha^I \alpha^{II} < 1$, we get,

$$V_B \leq \lim_{k \rightarrow \infty} V_{T,k}^{II-} - 2V_D \Leftrightarrow V_B \leq \frac{(1 + \alpha^I) V_{oc,max} - V_L^I - (\alpha^I \beta) V_L^{II}}{1 - \alpha^I \alpha^{II}} - 2V_D.$$

2.4.3 Series Synchronous Switched Harvesting on Inductor (S-SSHI)

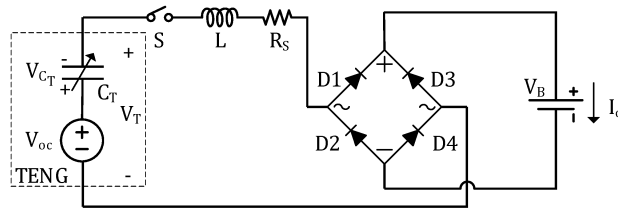


Figure 2.7 Series Synchronous Switched Harvesting on Inductor (S-SSHI) circuit

While TENGs generally have high open circuit voltage ($V_{oc,max}$), in the earlier discussed circuits, the maximum TENG voltage (V_T) gets clamped to a value limited by the battery load voltage. In contrast, a serial switch can allow the voltage buildup irrespective of the load voltage,

as in the presented case of the S-SSHI circuit. It consists of a serial switch connecting TENG with the battery load via an inductor L (Fig. 2.7). The TENG mostly operates in an open circuit condition (barring the leakage current) except when the switch is closed at States I and II for half the $L - C_T$ resonator cycle (T_{on}^{I} and $T_{\text{on}}^{\text{II}}$, respectively) to flip the TENG voltage polarity and in that process it charges the battery (Fig. 2.8). Since the switching time periods of T_{on}^{I} and $T_{\text{on}}^{\text{II}}$ are designed to be small compared to TENG's operation cycle, the load current (I_o) in the Fig. 2.8 appears as periodic spikes. It turns out that for the battery to be charged, the battery voltage must be below a critical value (derived below in Sec. 2.4.3.5). Fig. 2.8 contrasts the two cases, one where this condition is satisfied (top two plots, where the TENG voltage builds up and the battery charging current are shown) versus where the condition is not satisfied (bottom plot, where the TENG voltage does not build up and no battery charging current flows in the steady-state).

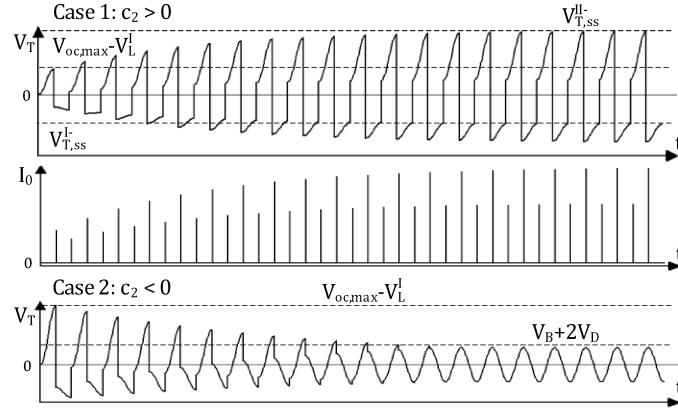


Figure 2.8 Typical S-SSHI circuit TENG voltage: $V_T(t)$ and output current: $I_o(t)$ plots.

2.4.3.1 S-SSHI circuit analysis at States I and II

We first analyze the simplified S-SSHI circuit at State II, as in Fig. 2.9(b), to obtain the relation between pre and post switched TENG voltages. The initial voltage of the TENG capacitor before the switching at Stage II is still denoted as $V_{C_T}^{\text{II}-}$. Using KVL around the loop,

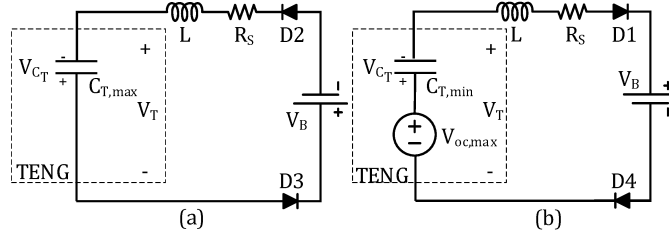


Figure 2.9 Simplified S-SSHI circuits at States (a) I and (b) II.

we arrive at the differential equation below,

$$\frac{d^2 V_{C_T}(t)}{dt^2} + \frac{R_S}{L} \frac{dV_{C_T}(t)}{dt} + \frac{V_{C_T}(t)}{LC_{T,\min}} + \frac{(V_B + 2V_D)}{LC_{T,\min}} - \frac{V_{oc,\max}}{LC_{T,\min}} = 0. \quad (2.33)$$

As in the case of the P-SSHI circuit, the switch is closed for half the $L - C_T$ resonator cycle.

Accordingly, solving the above differential equation and performing the analysis as in Sec. 2.4.2.1, the TENG capacitor voltage after the switching ($V_{C_T}^{II+}$) is given by,

$$V_{C_T}^{II+} = -\alpha^{II} V_{C_T}^{II-} + (1 + \alpha^{II})(V_{oc,\max} - V_B - 2V_D).$$

Using the TENG equation (2.4), we obtain,

$$V_T^{II+} = -\alpha^{II} V_T^{II-} + (1 + \alpha^{II})(V_B + 2V_D). \quad (2.34)$$

On the other hand, at State I, the S-SSHI circuit is simplified to that in Fig. 2.9(a), with pre and post switching TENG voltages related by (obtained by solving an equation of the type (3.30) with $V_{oc,\max}$ replaced by $V_{oc,\min} = 0$ so that $V_{C_T} = -V_T$, and $C_{T,\min}$ replaced by $C_{T,\max}$),

$$V_T^{I+} = -\alpha^I V_T^{I-} - (1 + \alpha^I)(V_B + 2V_D). \quad (2.35)$$

Here, α^I and α^{II} are the same as those defined earlier in (4.37) and (4.41), respectively.

2.4.3.2 Switching among States: Transient phase

The previous subsection discussed the S-SSHI circuit when the switch is closed at States I and II and derived the relations among the pre-switching and post-switching TENG voltages at both those states. Next, we derive the pre-switching TENG voltages at the two states to complete the

characterization of the TENG voltages. Unlike P-SSHI, the S-SSHI circuit has a transient phase, and either the maximum TENG voltage settles to a steady-state value higher than or equal to $V_{oc,max} - V_L^I$, or a value less than $V_B + 2V_D$ (refer Fig. 2.8), depending on whether the battery voltage is below or above a critical value. We model the TENG voltage transients to derive the steady-state values at States I and II. As before, we let the $V_{T,k}$ denote the TENG voltage in the k^{th} cycle.

With no current flow other than leakage between States I and II with switch S open,

$$Q_{C_T,k}^{II-} = Q_{C_T,k}^{I+} - |Q_L^I|. \text{ Hence,}$$

$$V_{T,k}^{II-} = V_{oc,max} - \frac{Q_{C_T,k}^{II-}}{C_{T,min}} = V_{oc,max} + \beta V_{T,k}^{I+} - V_L^I. \quad (2.36)$$

Using the above equation and the relation in (2.34), the post-switching TENG voltage at State II is given by,

$$V_{T,k}^{II+} = V_{oc,max} - \frac{Q_{C_T,k}^{II+}}{C_{T,min}} = -\alpha^{II}(\beta V_{T,k}^{I+} + V_{oc,max} - V_L^I) + (1 + \alpha^{II})(V_B + 2V_D). \quad (2.37)$$

With only leakage current up to reaching State I of the subsequent $(k+1)^{\text{th}}$ cycle

$(Q_{T,k+1}^{I-} = Q_{T,k}^{II+} - |Q_L^I|)$ and from above equation, it follows,

$$V_{T,k+1}^{I-} = -\frac{Q_{C_T,k+1}^{I-}}{C_{T,max}} = -\alpha^{II}V_{T,k}^{I+} + \frac{\alpha^{II}V_L^I}{\beta} + V_L^{II} - \frac{(1 + \alpha^{II})}{\beta}(V_{oc,max} - V_B - 2V_D). \quad (2.38)$$

Using (2.35), we arrive at the desired relation,

$$V_{T,k+1}^{I+} = c_1 V_{T,k}^{I+} + c_2, \text{ where,} \quad (2.39)$$

$$c_1 := \alpha^I \alpha^{II}; \quad c_2 := -[1 + \alpha^I + \frac{\alpha^I(1 + \alpha^{II})}{\beta}](V_B + 2V_D) + \frac{\alpha^I(1 + \alpha^{II})}{\beta} V_{oc,max} - \frac{\alpha^I \alpha^{II} V_L^I}{\beta} - \alpha^I V_L^{II}.$$

Above is a recursive relation, which can be solved to obtain the relation between $V_{T,k}^{I+}$ and $V_{T,1}^{I+}$:

$$V_{T,k}^{I+} = c_1^{k-1} V_{T,1}^{I+} + c_1^{k-2} c_2 + \dots + c_2.$$

Taking the TENG operation to start from rest, i.e., $V_{T,1}^{I+} = 0$, the above equates to a sum of geometric series with $(k-1)$ terms and common ratio, $c_1 = \alpha^I \alpha^{II} < 1$, and the first term as c_2 . It follows that,

$$V_{T,k}^{I+} = \frac{1 - c_1^{k-1}}{1 - c_1} c_2. \quad (2.40)$$

This provides a closed-form solution for the post-switching TENG voltage at State I of the k th cycle. Also using (4.5),

$$V_{T,k}^{\text{II}-} = V_{\text{oc,max}} + \beta \frac{1 - c_1^{k-1}}{1 - c_1} c_2 - V_L^{\text{I}}. \quad (2.41)$$

From the above equation, it is clear that when $c_2 > 0$, the TENG voltage builds up over time (increases with respect to k) as in Fig. 2.8 Case 1, and otherwise when $c_2 < 0$, it diminishes over time as in Fig. 2.8 Case 2. The latter case leads to no charging in the steady-state. No transient cycles are present for the special case of $c_2 = 0$.

2.4.3.3 Per-cycle energy output in steady-state

In the steady-state, from (3.8), the post-switching voltage and charge on TENG at State I can simply be written as:

$$V_{T,\text{ss}}^{\text{I}+} = \frac{c_2}{1 - c_1} = -\frac{Q_{C_T,\text{ss}}^{\text{I}+}}{C_{T,\text{max}}} \Rightarrow Q_{C_T,\text{ss}}^{\text{I}+} = -C_{T,\text{max}} \frac{c_2}{1 - c_1}. \quad (2.42)$$

Using this, along with the relations (4.5)-(3.7), we obtain the TENG capacitor charge values in the steady-state as:

$$Q_{C_T,\text{ss}}^{\text{II}-} = Q_{C_T,\text{ss}}^{\text{I}+} - |Q_L^{\text{I}}|; \quad (2.43)$$

$$Q_{C_T,\text{ss}}^{\text{II}+} = C_{T,\text{min}} \left[\frac{\alpha^{\text{II}} \beta c_2}{1 - c_1} + (1 + \alpha^{\text{II}})(V_{\text{oc,max}} - V_B - 2V_D) \right] - \alpha^{\text{II}} |Q_L^{\text{I}}|; \quad (2.44)$$

$$Q_{C_T,\text{ss}}^{\text{I}-} = Q_{C_T,\text{ss}}^{\text{II}+} - |Q_L^{\text{II}}|. \quad (2.45)$$

The change in TENG capacitor charge during the two switching periods flows through the load. S-SSHI being a series circuit, the leakage charge flows through the load too. So, the charge flowing through the load in one cycle equals,

$$\Delta Q_{\text{cycle}} = |\Delta Q^{\text{I}- \rightarrow \text{I}+}| + |\Delta Q^{\text{II}- \rightarrow \text{II}+}| + |Q_L^{\text{I}}| + |Q_L^{\text{II}}| = |Q_{C_T,\text{ss}}^{\text{I}+} - Q_{C_T,\text{ss}}^{\text{I}-}| + |Q_{C_T,\text{ss}}^{\text{II}-} - Q_{C_T,\text{ss}}^{\text{II}+}| + |Q_L^{\text{I}}| + |Q_L^{\text{II}}|.$$

The per-cycle energy output can be obtained as $V_B \Delta Q_{\text{cycle}}$. Using (2.42)-(2.45) and inserting value of c_1 and c_2 from (2.39),

$$E_{\text{cycle}} = \left[\frac{2(1 + \alpha^I)(1 + \alpha^{II})}{(1 - \alpha^I \alpha^{II})} \right] C_{T,\min} V_B [V_{\text{oc,max}} - (1 + \beta)(V_B + 2V_D)] - \frac{2V_B}{(1 - \alpha^I \alpha^{II})} c_3;$$

$$c_3 = (\alpha^{II}(1 + 2\alpha^I) - 1) \left| Q_L^I \right| + \alpha^I(1 + \alpha^{II}) \left| Q_L^{II} \right|.$$

The number of transient cycles required to attain the steady-state depends on the product of the two normalized quality factors $c_1 = \alpha^I \alpha^{II}$ (or equivalently their geometric mean). A system with a lower quality factor shall reach the steady-state quicker but with a lower per-cycle energy output for a given load.

2.4.3.4 Optimal battery load

E_{cycle} found in (2.46) is quadratic in V_B , which can be optimized to attain the optimal battery load (V_B^*) and maximized per-cycle energy (E_{cycle}^*):

$$V_B^* = \frac{V_{\text{oc,max}}}{2(1 + \beta)} - V_D - \frac{c_3}{2C_{T,\min}(1 + \beta)(1 + \alpha^I)(1 + \alpha^{II})};$$

$$E_{\text{cycle}}^* = \left[\frac{2C_{T,\min}(1 + \alpha^I)(1 + \alpha^{II})}{(1 - \alpha^I \alpha^{II})} \right] \left[\frac{V_{\text{oc,max}}^2}{4(1 + \beta)} - V_{\text{oc,max}} V_D + (1 + \beta) V_D^2 \right]$$

$$- \frac{c_3}{(1 - \alpha^I \alpha^{II})} \left[\frac{V_{\text{oc,max}}}{(1 + \beta)} - \frac{c_3}{2C_{T,\min}(1 + \beta)(1 + \alpha^I)(1 + \alpha^{II})} - 2V_D \right] \quad (2.46)$$

2.4.3.5 Upper bound to load battery

As discussed earlier, condition for S-SSHI circuit to reach a non-zero steady-state (so that battery can be charged in steady-state) is:

$$c_2 \geq 0 \Leftrightarrow V_B \leq \frac{V_{\text{oc,max}}}{1 + \frac{(1 + \alpha^I)\beta}{\alpha^I(1 + \alpha^{II})}} - \frac{(\alpha^I \alpha^{II}) V_L^I}{(1 + \alpha^I)(1 + \beta)} - \frac{V_L^{II}}{1 + \frac{1}{\alpha^I} + \frac{(1 + \alpha^{II})}{\beta}} - 2V_D. \quad (2.47)$$

The above condition sets an upper bound to the battery voltage for a sustained S-SSHI charging.

2.4.4 Comparative Analysis

In the above sections, we derived the closed-form results for each of the three considered circuits' per-cycle energy output. Here, we compare their optimal output in a common analytical

framework. For the sake of simplicity, we relax the analysis conditions by using ideal diodes and switches, i.e., take the values of diode voltage drop (V_D), leakage (Q_L^I, Q_L^{II}), and switch-on resistance (R_{on}) as zero. For further convenience, we define:

$$E_{\text{ref}} = C_{T,\min} V_{\text{oc,max}}^2.$$

This allows easy tabulation of optimal per-cycle energy output (E_{cycle}^*), optimal battery load (V_B^*), and maximum gain over FWR circuit ($\frac{E_{\text{cycle}}^*}{E_{\text{FWR,cycle}}^*}$) as in Table 2.1.

Table 2.1 Optimal energy output, optimal battery load, and maximum gain over FWR (under $V_D=0$; $Q_L^I=Q_L^{II}=0$)

Circuit	$\frac{V_B^*}{V_{\text{oc,max}}}$	$\frac{E_{\text{cycle}}^*}{E_{\text{ref}}}$	$\frac{E_{\text{cycle}}^*}{E_{\text{FWR,cycle}}^*}$
FWR	$\frac{1}{2(1+\beta)}$	$\frac{1}{2(1+\beta)}$	1
P-SSHI	$\frac{(1+\alpha^I)}{2(1-\alpha^I\alpha^{II})}$	$\frac{(1+\alpha^I)^2}{4(1-\alpha^I\alpha^{II})}$	$\frac{(1+\alpha^I)^2(1+\beta)}{2(1-\alpha^I\alpha^{II})}$
S-SSHI	$\frac{1}{2(1+\beta)}$	$\frac{(1+\alpha^I)(1+\alpha^{II})}{2(1-\alpha^I\alpha^{II})(1+\beta)}$	$\frac{(1+\alpha^I)(1+\alpha^{II})}{(1-\alpha^I\alpha^{II})}$

Using Table 2.1 values and taking the approximations,

$$\omega_d^I \approx \sqrt{\frac{1}{LC_{T,\max}}} \text{ and } \omega_d^{II} \approx \sqrt{\frac{1}{LC_{T,\min}}},$$

$$Q_f^{II} = \frac{\omega_d^{II} L}{R_L} \approx \sqrt{\beta} Q_f^I \text{ and } \ln \alpha^{II} \approx \frac{\ln \alpha^I}{\sqrt{\beta}},$$

we study the effect of quality factor on the optimal gains of P-SSHI and S-SSHI circuits over FWR as in Fig. 2.10.

- The optimal gains of P-SSHI and S-SSHI circuit are increasing with inductor quality factor (Fig. 2.10(Top)).
- For $\beta = 1$, the optimum gains turn out to be the same for both P-SSHI and S-SSHI circuits, and it improves with increasing β for both circuits (Fig. 2.10(Top)).
- For any $\beta > 1$, the optimal gain of P-SSHI is higher than S-SSHI (Fig. 2.10(Top)), but this is achieved for optimal battery load several times the maximum open circuit voltage

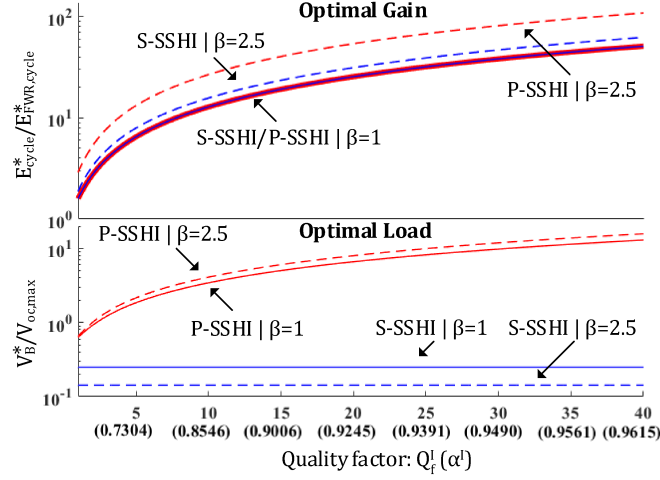


Figure 2.10 Top/Bottom: Comparison of optimal energy gain (resp., battery load) of the P-SSHI and S-SSHI circuits over FWR (resp., over $V_{oc,max}$) against the inductor quality factor.

($V_{oc,max}$) depending on the quality factor (Fig. 2.10(Bottom)). TENGs typically have high $V_{oc,max}$ (in tens to hundreds of volts), and hence implementing a P-SSHI circuit at optimal load shall be challenging.

- In contrast, optimal load for the S-SSHI circuit is independent of quality factor and lower than $V_{oc,max}$ (Fig. 2.10(Bottom)).

Further, the effect of battery load on the energy output is studied in Sec. 2.6.

2.5 Experimental Implementation

2.5.1 Experimental Setup

TENG with a contact area of 113.8 cm^2 is built as shown in the schematic of Fig. 2.1 using Al foil as the electrodes and Teflon of thickness 127 um as the dielectric. The bottom plate is fixed while the top plate is driven in a vertical contact-separation mode by a stepper motor (Applied Motion STM 17Q-3AE) programmed using vendor-provided software (Q ProgrammerTM) to

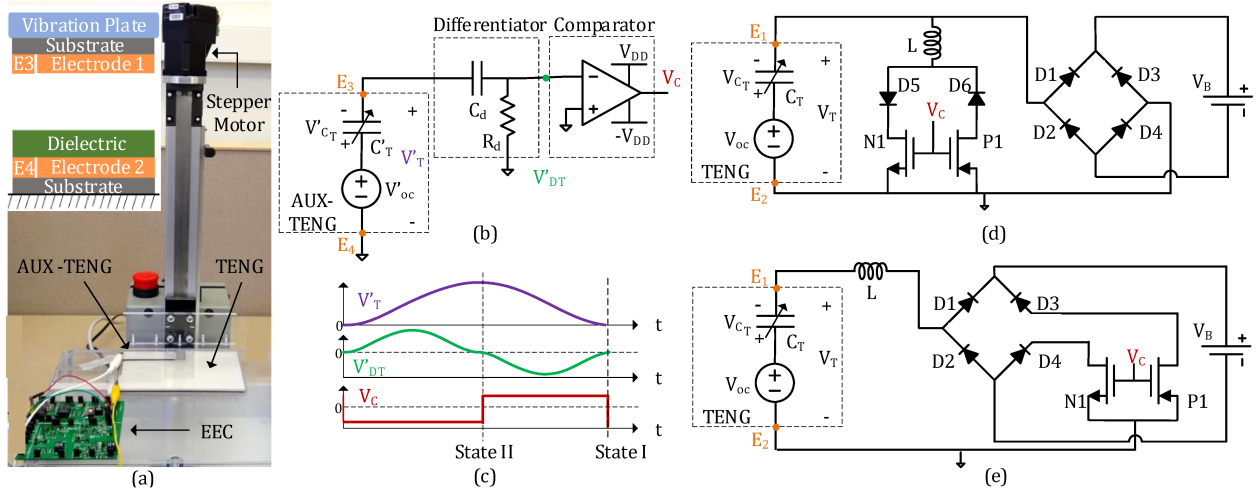


Figure 2.11 (a) Experimental setup; Inset: Cross section view of a contact-separation TENG with Aux-TENG (b) Control circuit for P-SSHI and S-SSHI circuits (c) Control circuit waveforms (d) P-SSHI circuit implementation (e) S-SSHI circuit implementation

operate at 10 Hz frequency and maximum separation ($x_{\max}$) of 1.2 mm. The setup picture is shown in Fig. 2.11(a).

2.5.2 TENG Characterization

The key electrical parameters to characterize TENG are maximum open circuit voltage ($V_{oc, \max}$), minimum and maximum TENG capacitance ($C_{T, \min}$ and $C_{T, \max}$).

2.5.2.1 TENG capacitance

We follow the method described in [23],[36] to measure the dynamic variation of the TENG Capacitance ($C_T(t)$) and extract the minimum and maximum value ($C_{T, \min}$ and $C_{T, \max}$). The details of the method are repeated in the Appendix 2.9 along with the plot of measured $C_T(t)$.

2.5.2.2 TENG maximum open circuit voltage

We use the standard FWR circuit to measure $V_{oc,max}$. In the Sec. 2.4.1.3, the upper bound on the load battery voltage is derived for the FWR circuit. Instead of a battery, if a capacitor (of any capacitance) is charged using a FWR circuit, its voltage will saturate at the same value (V_{sat}), which by (2.13) satisfies:

$$V_{oc,max} = (\beta + 1)(V_{sat} + 2V_D).$$

By charging a capacitor, V_{sat} was measured as 54.4 V using a high impedance electrometer (Keithley 6517). At saturation, negligible current flows through the FWR circuit, and hence diode voltage drop (V_D) can be neglected, yielding $V_{oc,max}$ as 188.77 V. The measured TENG parameters are summarized in Table 2.2.

Table 2.2 Measured TENG parameters

Maximum open circuit voltage: $V_{oc,max}$	188.77 V
Minimum TENG capacitance: $C_{T,min}$	97.28 pF
Maximum TENG capacitance: $C_{T,max}$	239.80 pF
TENG capacitance ratio: β	2.47

2.5.3 Implementation of Energy Extraction Circuits

Synchronous switched circuits (P-SSHI and S-SSHI) described above are implemented using the MOSFET as switches and operated through dedicated control circuits. The control circuit's function is to detect States I and II during the TENG operation and issue the required gate pulse to the MOSFET switches. The switching control circuit receives input from an “auxiliary” TENG (with contact area $1/8^{th}$ to that of the main TENG) that operates in parallel to the main TENG (Fig. 2.11(a)). Note that a part of the innovation is building both the TENGs within the same structure with shared dielectric and substrate to ensure synchronization. This design was achieved practically by cutting out a narrow strip of the Al sheet to create two separate

electrodes. This isolation of auxiliary TENG (from the main TENG) prevents performance degradation by enabling non-interfering and synchronized operation of the control circuit. The energy consumed by the control circuit can be deduced separately and is given in Table 2.3. Off-the-shelf components used for the implementation are listed in Appendix 2.10, while the measurement methods used for obtaining the control circuit current, TENG voltage, and load current are covered in Appendix 2.11.

Table 2.3 Control circuit power consumption

Circuit	Avg. Current	Supply Voltage ($2V_{DD}$)	Power
P-SSHI	257 nA	4 V	1.03 μ W
S-SSHI	590 nA	7 V	4.13 μ W

2.5.3.1 FWR circuit

Implementation of the FWR circuit that contains no synchronized switches is straightforward, as shown in Fig. 2.2. Fig. 2.12(a) shows the measured TENG voltage (V_T) and load current (I_o) for the battery load (V_B) of 15 V.

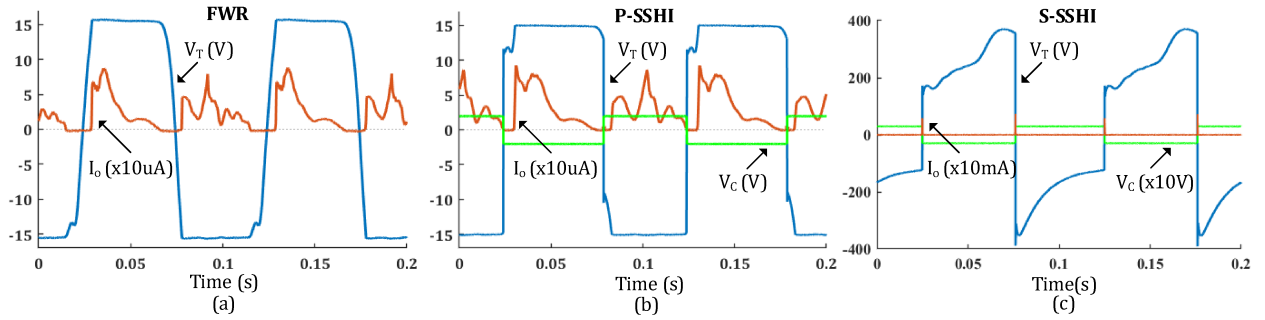


Figure 2.12 Measured TENG Voltage (V_T), load current (I_o) and (if) control voltage (V_C) waveforms at 15V battery load of the (a) FWR, (b) P-SSHI, and (c) S-SSHI circuits.

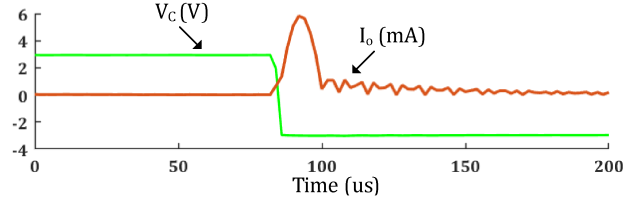


Figure 2.13 Zoomed-in view of S-SSHI circuit's measured load current (I_o) and control voltage (V_C) waveforms during switching at State I.

2.5.3.2 P-SSHI circuit

P-SSHI circuit is implemented as shown in Fig. 2.11(d). Its synchronized switching control circuit consists of a RC differentiator followed by a zero-crossing comparator (Fig. 2.11(b)). Value of RC differentiator is chosen to provide high output impedance to the Aux-TENG (“auxiliary” TENG); hence it operates in near open circuit condition (V_T'). The differentiated signal (V_{DT}') is zero at the extrema: States I and II, which triggers the state change of the comparator (V_C) (Fig. 2.11(c)). The NMOS switch is turned on at State II and PMOS at State I due to state change in gate signal (V_C). The switch turn-off is automatic since the current direction reversal at the end of half the $L - C_T$ resonator time period is blocked by the corresponding diode $D5$ (or $D6$). The control circuit is powered by ± 2 V external source. Fig. 2.12(b) shows the measured TENG voltage (V_T), control signal (V_C), and load current (I_o) for the battery load (V_B) of 15 V. Note the instants of voltage inversion at States I and II compared to the FWR circuit TENG voltage (Fig. 2.12(a)).

2.5.3.3 S-SSHI circuit

Here, the same control circuit as used for the P-SSHI circuit is used (Fig. 2.11(b)) and is powered by ± 3.5 V supply. Fig. 2.11(e) shows the implementation of the S-SSHI circuit. The circuit operation is the same as the P-SSHI circuit explained above, with the inductor, NMOS and PMOS switches in series connection with the TENG compared to parallel as in the case of the P-SSHI circuit. Fig. 2.12(c) shows the measured steady-state TENG voltage (V_T), control signal (V_C), and load current (I_o) for the battery load (V_B) of 15 V. Note the TENG voltage at

State II reaches almost twice the maximum open circuit voltage of the TENG ($V_{oc,max}$) due to the transient buildup via voltage inversions. Fig. 2.13 shows the zoomed-in view of the I_o and V_C during the switching at State I. The load current (I_o) is a half sinusoid since the switch is on for half the $L - C_T$ oscillation time period. The post-switching ringing transients observed in I_o can be attributed to the stray parasitics of the circuit.

2.6 Energy Results and Discussion

The experimentally measured, simulated, and analytically obtained per-cycle energy output (E_{cycle}) at different load battery values (V_B) for each of the three considered energy extraction circuits (EECs) are co-plotted in Fig. 2.14. Experimental results were obtained using the implemented TENG with parameters listed in Table 2.2. For simulation, the TENG circuit model described in Sec. 2.3 was implemented in a PSpice tool using the same measured parameters of Table 2.2 and operation frequency of 10 Hz. The circuits were built using the PSpice models of the off-the-shelf components (diodes, MOSFETs, and comparator) used in experimental implementation available from the vendor websites. The commercial inductor used in the P-SSHI/S-SSHI circuit was modeled as a series $L-R_L$ for simulation with frequency-dependent inductance and resistance values obtained experimentally using the LCR meter at the respective $L-C_T$ resonance frequencies of States I and II: ω_d^I and ω_d^{II} (refer Appendix 2.12 for details). Whereas for the analytical results, measured TENG parameters (Table 2.2) and the non-ideality parameters estimated from the manufacturer-provided PSpice models and the simulation of those models at multiple operating points were used in the equations derived in Sec. 2.4. The parameter values of the considered non-idealities: Diode voltage drop (V_D), Leakage charges (Q_L^I and Q_L^{II}), and the normalized quality factors (α^I and α^{II}), that change significantly over the operating range of the battery load, are tabulated for each circuit as Tables 2.7-2.9 in Appendix 2.13 and were estimated at each 2V increment of battery load using their PSpice model simulations.

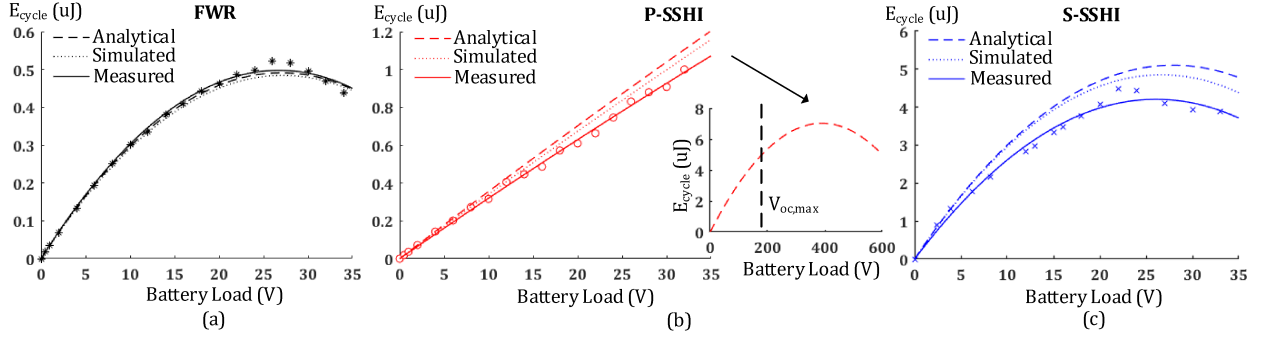


Figure 2.14 Analytical, simulated, and measured per-cycle energy plots for (a) FWR, (b) P-SSHI; Inset: Extrapolated P-SSHI analytical plot, and (c) S-SSHI circuits against the battery load.

2.6.1 FWR Circuit

Referring to Fig. 2.14(a), E_{cycle} shows the parabolic behavior to the change in V_B with peak at 26.7 V, as expected from the analytical derivation of (2.9). A close match between the analytical, simulated, and measured values is achieved.

2.6.2 P-SSHI Circuit

The E_{cycle} for the P-SSHI circuit strictly increases with V_B in the considered range of 0–35 V (Fig. 2.14(b)). From the analysis (2.30), the response is expected to be parabolic in nature with a peak obtained at battery load several times the maximum open circuit voltage ($V_{\text{oc,max}}$). Extrapolation of the analytical curve (inset Fig. 2.14(b)) indeed confirms the same with the peak around 400 V, keeping in mind that the extrapolation is based on the used non-ideality parameters at lower operating voltages.

2.6.3 S-SSHI Circuit

For the S-SSHI circuit, the parabolic response gives the peak E_{cycle} at around 26 V (Fig. 2.14(c)). For an ideal circuit, the peak is expected at the same voltage as the FWR circuit (refer Table 2.1), but the leakage and diode drop shifts the peak lower. S-SSHI circuit has a high steady-state voltage of almost 400 V (Fig. 2.12(c)), which requires the use of high-rated

MOSFETs (refer Appendix 2.10 for details) accompanied with significant leakage charge (refer cols 5 and 6 in Table 2.9 of Appendix 2.13). Hence, leakage charge becomes the dominant non-ideality affecting the S-SSHI circuit's performance. Also, stray parasitics such as inductor and MOSFET's parallel capacitance give rise to post-switching ringing transients as can be seen in the measured circuit current (Fig. 2.13). Such ringing leads to a post-switching additional loss of TENG charge, and so an immediate decrease (in absolute terms) in the post switching voltage (Fig. 2.12(c)), resulting in reduced E_{cycle} . This additional loss in the TENG charge is also captured in the analytical results through the added leakage charge term Q_L . Any additional remaining discrepancy between the experimental and the analytical results may be attributed to the unaccounted factors such as practical delay in the control circuit that leads to switching past the extrema (States I and II); measurement errors in the TENG parameters of Table 2.2; the TENG's own parasitic resistance (due to imperfect connection to the electrode, connection wires); etc.

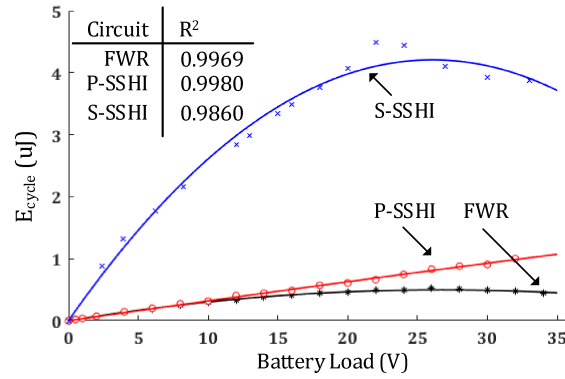


Figure 2.15 Comparison of measured per-cycle energy output for FWR, P-SSHI, and S-SSHI circuits against the battery load.

2.6.4 Overall Comparison

Fig. 2.15 plots the measured E_{cycle} for all the considered circuits. At lower battery loads, the P-SSHI circuit has output almost equal to the FWR circuit as expected: The MOSFET switches fail to turn “on” since the battery load equals the drain to source voltage (V_{ds}) of the MOSFETs,

that turns the P-SSHI circuit of Fig. 2.11(d) to simply the FWR circuit of Fig. 2.2. The S-SSHI circuit has the highest output in the considered load range.

Using Cycle for Maximized Energy Output (CMEO) [15] as a reference, the energy conversion efficiency (η) can be obtained as a metric for comparison of EECs as has also been done in [17, 27]. CMEO calculates the per-cycle energy by plotting voltage-vs-charge and finding the enclosed area that corresponds to simple switching at the two extremes to let the charge flow from one plate to the other via an ideal infinite load, thereby supplying energy to it, and is given by: $E_{\text{CMEO}} = \frac{1}{2} \left(1 + \frac{1}{\beta}\right) C_{T,\min} V_{\text{oc,max}}^2$. It should be noted that by its design, CMEO does not involve any “smart” altering of the polarity of the TENG charge, unlike the analyzed SSHI circuits, which by design flip the TENG charge by LC oscillation at extrema to invoke “pre-charging” of TENG and thereby achieve output greater than CMEO: This pre-charging of the TENG capacitor increases the electrostatic force between the two plates during the separation phase and thereby increasing the positive work, while during the contraction phase, it reduces the negative work by reducing the charge across the plates [37]. Table 2.4 lists η values for FWR, P-SSHI, and the S-SSHI circuit obtained by dividing their measured per-cycle energy output (E_{cycle}) by E_{CMEO} . The gain of the two SSHI circuits over the standard FWR circuit at battery load of 15 V and 30 V is also listed in Table 2.4.

Table 2.4 Energy conversion efficiency and gain over FWR circuit at battery load of 15V and 30V.

Circuit	Efficiency $\left(\eta = \frac{E_{\text{cycle}}}{E_{\text{CMEO}}}\right)$		Gain over FWR	
	$V_B=15 \text{ V}$	$V_B=30 \text{ V}$	$V_B=15 \text{ V}$	$V_B=30 \text{ V}$
FWR	16.50%	20.13%	-	-
P-SSHI	19.53%	38.07%	1.18	1.89
S-SSHI	141.65%	168.87%	8.59	8.39

It should be noted that since the two switched inductor circuits require overhead power for the control circuit (Table 2.3), their net output and gain over FWR is lower. For example, in our implementation, the P-SSHI control circuit requires 1.03 μW . Hence, the operation at 10 Hz

extracts net positive energy for battery load greater than 3.2 V and has increased gain over FWR circuit post battery load of 16.75 V.

2.7 Conclusion

This work developed a mathematical analysis framework for the synchronous switched energy extraction circuits: P-SSHI and S-SSHI along with the standard FWR circuit for TENG transducers and derived closed-form formulae for their per-cycle energy output, optimum battery load value, and also the upper bound on battery voltage beyond which extraction is not feasible. The modeling included the non-idealities of diode drop, leakage current, and switch and inductor resistances. The strong match of analytical model results with simulation and measured ones shows that the analytical models can be used to assess TENG EEC performance once the TENG parameters have been measured.

An ideally switched P-SSHI/S-SSHI circuit at optimal load was found to provide more than 100 fold gain over the FWR circuit at their optimum values, depending on the inductor quality factor. The effect of load battery change on the per-cycle energy output was examined. All the circuits show a parabolic response, providing an optimal battery load and an upper bound. Experimental implementation showcased the P-SSHI and S-SSHI circuit's gain of 1.18 and 8.59 over the standard FWR circuit at the load voltage of 15 V, respectively. While the measured energy conversion efficiency with respect to the Cycle for Maximized Energy Output (CMEO) at the same load of 15 V was found to be 16.50%, 19.53%, and 141.65%, respectively, for the FWR, P-SSHI, and S-SSHI circuits.

Such comparison of energy extraction circuits brought forward their pros versus cons over each other. S-SSHI has superior energy output compared to other circuits but operates over a smaller load range. While P-SSHI energy output can exceed that of S-SSHI, it is optimized at a load voltage value several times the TENG maximum open circuit voltage ($V_{oc,max}$). Use of a DC/DC converter can make this feasible, but with added complexity and loss, and so P-SSHI shall be more suited for TENG with low $V_{oc,max}$. Also, for a TENG with low $V_{oc,max}$ or high β ,

the low upper bound on the battery load in the case of the S-SSHI circuit can be limiting. In summary, the presented work offers design insights/tradeoffs for TENG energy extraction circuits.

A possible direction of further research is to implement the discussed circuit architectures by using “passive” control circuits. Development of integrated, efficient DC/DC converters to operate the P-SSHI and S-SSHI circuit at their optimal load for any given TENG and the on-board battery is another direction. Further, implementing the EECs identified leakage through MOSFET switches as one of the major loss factors. So other switching technologies with high rated voltage and low leakage, such as SiC (Silicon Carbide), can be explored.

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2.9 Appendix A: Dynamic measurement of TENG capacitance

To measure the TENG capacitance, a programmable function generator (Agilent E3646A) was used as an AC voltage source with frequency f_{ac} (set several magnitudes higher than the TENG operation frequency f) and was connected to TENG as seen in Fig. 2.16. Using a voltage follower, built using high input impedance op-amp (TI OPA454), Voltages V_A and V_B were observed on the two channels of an oscilloscope (Keysight DSOX2024A). The voltage data was collected through the National Instruments Data Acquisition Card and Labview program and processed to compute $C_T(t) = \frac{1}{2\pi f_{ac} R_M \tan(\theta(t))}$, wherein θ is the measured phase difference between the AC voltages V_A and V_B . Fig. 2.16 plot shows the computed $C_T(t)$, from which we determined $C_{T,max} = 239.80$ pF and $C_{T,min} = 97.28$ pF.

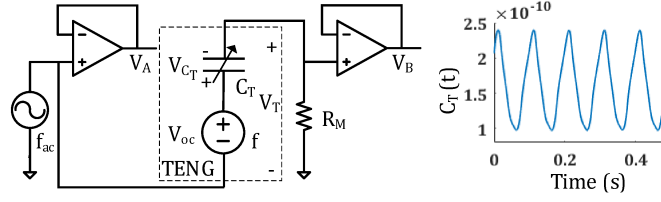


Figure 2.16 Measurement setup for TENG capacitance ($C_T(t)$) and its plot.

2.10 Appendix B: List of off-the-shelf components used

All MOSFETs were sourced from Diodes Inc. (diodes.com), inductor from Bourns Inc. (bourns.com), didoes from ON Semiconductors (onsemi.com), and TS881 used as a comparator in the control circuit from STMicroelectronics (st.com). PSpice models used were downloaded from vendor websites.

Table 2.5 List of discrete components used

Circuit	FWR	P-SSHI	S-SSHI
Diode	1N4148	1N4148	MUR160
NMOS	-	DMN601K	DMN60H080DS
PMOS	-	DMP510DL	DMP45H150DE
Inductor	-	RLB1014-104KL	RLB1014-104KL

2.11 Appendix C: Measurement methods

To measure the TENG voltage, an op-amp based voltage follower circuit was employed. The time-varying voltage plot was obtained through an oscilloscope, which was then collected through the National Instruments Data Acquisition Card and Labview program.

For measuring the load current as well as implementing a battery load, an op-amp based scheme of Fig. 2.17 below was used (except for S-SSHI—see the below discussion for that case). Due to this op-amp based scheme, the load voltage as seen by the circuit (namely, the voltage of the negative input terminal of the op-amp) remains constant at V_B irrespective of the load current, as desired. The output voltage of op-amp (V_o) was recorded using an oscilloscope, which was then processed to obtain load current waveform as $I_o(t) = \frac{V_B - V_o(t)}{R_F}$. The same op-amp

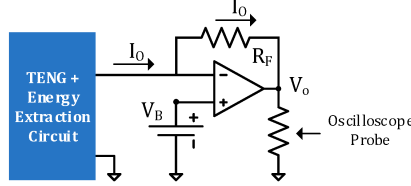


Figure 2.17 Circuit for load current measurement and implementing constant voltage load.

based scheme is not feasible for the S-SSHI circuit operating at high voltage. But since it has high output current (in mA), it is possible to simply use Zener diodes of different rated voltages to act as battery loads and measure the load current by monitoring voltage drops across a sensing resistor placed in series with the Zener diodes.

The average biasing current of the control circuit listed in Table 2.3 was measured with the help of a current sense amplifier (TI INA293) and an oscilloscope.

2.12 Appendix D: Inductor Characterization

The inductor is modeled as series L - R_L for the simulation. Both L and R_L were measured using the LCR meter (Keysight E4980A) at the State I and State II resonance frequency (ω_d^I and ω_d^{II}) and are tabulated below. The nominal inductance for RLB1014-104KL used in P-SSHI/S-SSHI circuit was 100 mH.

Table 2.6 Inductor Characterization

Frequency	L(mH)	$R_L(\Omega)$
$\omega_d^I = 227.02$ kHz	80.91	296
$\omega_d^{II} = 343.55$ kHz	87.09	395.6

2.13 Appendix E: Non-ideality parameters

Table 2.7 lists the values of the diode voltage drops (V_D), averaged across all the diodes, for the FWR circuit, and was obtained from manufacturer PSpice models and their simulation at the increments of 2V battery load (V_B).

Table 2.7 FWR circuit's average diode voltage drop at different battery load

V_B (V)	V_D (mV)	V_B (V)	V_D (mV)
2	239.190	24	239.000
4	239.195	26	235.895
6	239.170	28	236.880
8	240.010	30	233.820
10	241.085	32	232.110
12	241.715	34	231.190
14	240.405	36	229.975
16	240.890	38	228.430
18	239.935	40	225.680
20	239.660	42	222.920
22	238.615	44	219.840

Table 2.8 and Table 2.9 list the values of non-ideality parameters obtained from manufacturer PSpice models and the simulation of those models at increments of 2V battery load (V_B) for the P-SSHI and S-SSHI circuits, respectively. In both the tables, the diode voltage drop: V_D averaged across all diodes is listed first. Following two columns list α^I and α^{II} , the normalized resonator quality factor during switching at States I and II, respectively. In the last two columns, Q_L^I and Q_L^{II} list the leakage charge during the first-half-cycle and second-half-cycle, respectively.

Table 2.8 P-SSHI circuit's non-ideality parameters at different battery load

V_B (V)	V_D (mV)	α^I	α^{II}	Q_L^I (nC)	Q_L^{II} (nC)
2	238.630	0.982685	0.992048	0.417454	0.336543
4	238.610	0.964918	0.972427	0.471214	0.355721
6	238.580	0.962172	0.963049	0.527053	0.374757
8	238.530	0.958906	0.962619	0.573477	0.392414
10	238.480	0.956383	0.959136	0.618310	0.410486
12	238.360	0.955017	0.960197	0.663186	0.429357
14	238.565	0.954870	0.961392	0.705960	0.447556
16	238.485	0.954431	0.960071	0.748835	0.463513
18	238.375	0.954023	0.959017	0.787447	0.480360
20	238.260	0.953624	0.958170	0.825341	0.497374
22	238.115	0.953273	0.958331	0.866459	0.516530
24	237.955	0.952561	0.958361	0.906872	0.531336
26	237.780	0.952291	0.957609	0.937981	0.549390
28	237.620	0.952431	0.957765	0.979318	0.565194
30	237.420	0.951825	0.958160	1.012891	0.582427
32	237.210	0.952550	0.957170	1.046312	0.598388
34	236.970	0.951946	0.957555	1.075120	0.616600
36	236.730	0.951743	0.957006	1.119814	0.631156
38	236.480	0.951257	0.957007	1.169261	0.647248
40	236.195	0.951298	0.956769	1.216217	0.666166
42	235.915	0.951122	0.957339	1.270956	0.689827
44	235.595	0.951433	0.956825	1.360819	0.712828

Table 2.9 S-SSHI circuit's non-ideality parameters at different battery load

V_B (V)	V_D (mV)	α^I	α^{II}	Q_L^I (nC)	Q_L^{II} (nC)
2	711.620	0.824141	0.973194	6.729874	16.094671
4	711.205	0.827699	0.973968	6.644104	15.083334
6	710.860	0.829109	0.973642	6.570467	13.609666
8	710.585	0.827362	0.97366	6.515866	12.701908
10	710.065	0.831173	0.971093	6.434156	11.453035
12	709.680	0.833499	0.969869	6.402619	10.413612
14	708.965	0.838585	0.962589	6.410849	9.182698
16	707.990	0.844684	0.964754	6.421081	8.230673
18	707.440	0.851579	0.961934	6.453288	7.315406
20	701.105	0.861117	0.961399	6.474542	6.541747
22	705.045	0.872938	0.95959	6.571256	5.896586
24	703.925	0.881601	0.958869	6.505392	5.273539
26	703.040	0.895017	0.960909	6.471428	4.810095
28	700.830	0.908616	0.954769	6.471593	4.286924
30	699.540	0.924828	0.957486	6.472602	3.974769
32	697.450	0.945902	0.957086	6.455887	3.526472
34	692.645	0.960356	0.956701	6.499851	2.90527
36	682.280	0.94225	0.94882	6.101366	1.892802
38	673.480	0.943536	0.953631	5.625206	1.738115
40	660.885	0.940743	0.948493	5.171155	1.474435
42	647.110	0.940695	0.951682	4.715545	1.242598
44	629.710	0.942761	0.950688	4.058914	1.021044

CHAPTER 3. SYNCHRONOUS PRE-BIASING OF TRIBOELECTRIC NANOGENERATOR FOR ENHANCED ENERGY EXTRACTION

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3.1 Abstract

Triboelectric Nanogenerator (TENG) is a class of ambient mechanical energy harvesters used to augment the battery life of electronic devices such as sensors in implantables, wearables, and Internet of Things (IoT) applications. In this work, the fundamentals of pre-biasing (pre-charging) the TENG at the start of the operation cycle to enhance the per-cycle extracted energy is presented. The energy gain is mathematically formulated, and the optimum pre-biasing voltage (equivalently charge) is derived by analyzing the energy exchange between the mechanical and the electrical domain over a periodic cycle. Further, a novel Energy Extraction Circuit (EEC) termed as “Pre-biased Synchronous Charge Extraction (pSCE)” is introduced to 1) Realize synchronous pre-biasing of TENG using the load battery itself and 2) Achieve enhanced energy extraction from TENG. Energy output per-cycle is derived analytically for the pSCE circuit and compared to the state of the art Synchronous Charge Extraction (SCE) circuit. The experimental implementation is performed for the proposed pSCE circuit that shows a 6.65 fold gain over the Full Wave Rectifier (standard EEC) and 1.45 over the SCE circuit for a 5 V battery load.

3.2 Introduction

Wireless sensor nodes used in the Internet of Things (IoT), wearable, and implantable applications are commonly powered by an onboard battery. Harnessing the ambient mechanical energy via an integrated energy harvester to charge the onboard battery is a green solution to

prolonging the battery life [1]. Recently developed Triboelectric Nanogenerator (TENGs) involving friction-induced triboelectrification and electrostatic induction have shown promising potential as versatile mechanical-to-electrical energy transducers [2, 3]. TENGs with its almost universal choice of materials and multiple operation modes [2] have been shown to harvest energy from variety of sources such as wind/water flow [4, 5, 6], machine/structure vibration [7], human body motion [8, 9], etc.

Motion transduction by TENG leads to variable output that needs rectification to charge DC battery load, and thus, Full Wave Rectifier (FWR) can be considered the simplest Energy Extraction Circuit (EEC) [10]. Approaches to enhance TENG's energy output require improving the source to load matching. To this end, several novel EEC architectures have been proposed in the literature to increase the energy output beyond the FWR circuit such as [11, 12, 13, 14, 15, 16, 17]. It is shown in [11] that all these different EEC outputs are confined within the cycle for maximized energy output (CMEO), where the *synchronously serial switched flyback converter with the rectified TENG output* can achieve the CMEO irrespective of the load value [14, 17, 18, 19]. This last architecture has been proposed previously in the piezoelectric context [20, 21, 22], by the name of Synchronous Charge Extraction (SCE), which is how we also refer to it in this paper.

The aforementioned EECs may be viewed as *passive EECs*, where no harvested energy is fed back to the TENG. In this work, we propose synchronous *pre-biasing* (or pre-charging) of TENG by feeding back some of the load battery energy to the TENG, thereby realizing an “*active*” *EEC*, which enables to achieve a net output beyond the CMEO limit. Here, synchronous pre-biasing refers to charging the TENG capacitor at the start of each half-cycle (at the minimum and maximum separation of TENG plates) by using the battery. During the separation phase, pre-biasing increases the electrostatic force between the two TENG plates and thereby the transduced energy in form of work done against it by the mechanical source, while during the contraction phase, pre-biasing reduces the TENG charge to zero for no loss of stored potential electrical energy to the environment. This work provides the following major contributions:

- A novel Energy Extraction Circuit (EEC) termed as “Pre-biased Synchronous Charge Extraction (pSCE)” is introduced for the first time for synchronous energy extraction in-tandem with synchronous pre-biasing of TENG.
- The per-cycle energy output of the proposed pSCE circuit is mathematically derived and is shown to exceed the SCE circuit’s CMEO output at all load voltages.
- Upper limits and optimum values, if any, on the pre-biasing voltage for each half-cycle of TENG operation are mathematically derived by analyzing the interplay of mechanical motion and electrostatic forces.
- The experimental implementation of the pSCE circuit along with its synchronous switching controller is also presented, and an output gain of 1.45x over its peer SCE circuit and 6.65x over the standard Full Wave Rectifier (FWR) circuit is experimentally achieved. The comparative advantage over those reported in prior works [12, 13, 14, 15, 16, 17], [23, 24, 25, 26, 27, 28] is also reported, along with a *quantitative* comparison summarized in Table V.

Note that while we perform pre-biasing using the load battery itself, this can also be achieved by feeding back a fraction of the output charge [28, 29, 30] or also by the use of LC circuit oscillation, i.e., by using a parallel or series synchronous switched harvesting on inductor (P-SSHI/S-SSHI) circuit as EECs, as presented in our earlier works [23, 24] and in [25, 26, 27]. A key advantage of the proposed pSCE circuit as derived in this work is a guaranteed output beyond CMEO at all load voltages, unlike P-SSHI, S-SSHI EECs that may require additional power-consuming Maximum Power Point Tracking (MPPT) circuit to operate at their optimal load and to exceed the CMEO[24].

Also, it should be stated that while pSCE circuit architecture has been explored previously for piezoelectric transducers [21, 31], the analysis is entirely different in the case of triboelectric transducers since it has a different circuit model: For a piezoelectric transducer, capacitor appears in *parallel* to the source and is *fixed*, whereas the triboelectric capacitor appears in *series* and is

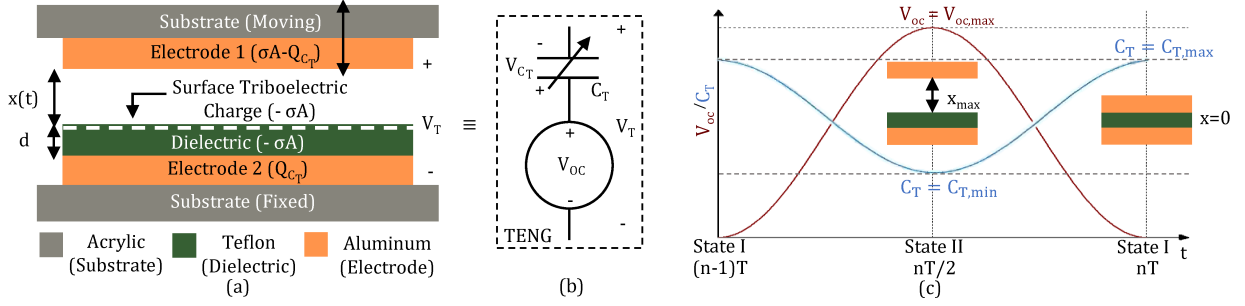


Figure 3.1 (a) Cross-section view of a contact-separation TENG with a parallel auxiliary TENG (b) Equivalent circuit model of TENG (c) Periodic variation of open-circuit voltage ($V_{oc}(t)$) and TENG capacitance ($C_T(t)$) over a period T .

time-varying. The work reported here innovates to deal with this time-varying nature by *smart discretization*, i.e., by performing analysis at the two extremities (plates fully contracted versus separate); *no such discretization is needed in the piezoelectric case* as the same set of time-invariant equations remain valid at all instances. The triboelectric analysis framework is thus much more intricate and has been developed in the presented generality for the first time. Also, owing to the above differences in the circuit model, the switching control circuits of the piezoelectric setting do not work in the TENG setting, and new switching circuits have been devised for the experimental implementation.

3.3 Preliminaries: TENG Model

The most generic form of TENG operation is in contact-separation mode where, as depicted in Fig. 3.1(a), the two parts of the TENG, namely, a metal film acting as Electrode 1 (upper Al plate here) and a metal film covered with dielectric acting as Electrode 2 (bottom Al plate covered with a Teflon tape) repeatedly comes in contact and separates under the influence of an external motion. Repeated contact-separation between the two plates generates equal and opposite triboelectric static charges on the two plates, with density, denoted σ . Ignoring the fringing field effect, the resulting field is given by,

$$\vec{E}_\sigma = \frac{-\sigma}{\epsilon_0} \vec{1}_x, \quad (3.1)$$

where ϵ_0 is the electrical permittivity of air, and $\vec{1}_x$ is the unit vector pointing upwards in the direction of increasing x . The voltage induced between the two electrodes by the above electric field is termed as open-circuit voltage and is given by,

$$V_{oc}(t) = - \int_0^{x(t)} \vec{E}_\sigma \cdot \vec{1}_x dx = \frac{\sigma x(t)}{\epsilon_0}. \quad (3.2)$$

Also, TENG forms a variable capacitor with air gap, $x(t)$ and dielectric of thickness d between the two electrodes:

$$C_T(t) = \frac{\epsilon_0 A}{x(t) + d_{eff}}; \quad d_{eff} = \frac{d}{\epsilon_d}.$$

Here, A is the contact surface area of the plates, and ϵ_d is the relative permittivity of the dielectric layer, lowering its effective thickness to d_{eff} .

When TENG is connected to an external circuit, the movement of the conduction charge (distinct from the triboelectric charge) from one electrode to another, say $Q_{C_T}(t)$ (Refer Fig. 3.1(a)), leads to a capacitor voltage, $V_{C_T}(t)$ between the two electrodes. Thus, the net TENG voltage (V_T) is the superposition of open-circuit voltage (V_{oc}), owing to the static triboelectric charge and its induced electrostatic emf, and the TENG capacitor voltage (V_{C_T}), owing to the free conduction charges on the electrodes:

$$V_T(t) = V_{oc}(t) - V_{C_T}(t) = \frac{\sigma x(t)}{\epsilon_0} - \frac{Q_{C_T}(t)}{C_T(t)}. \quad (3.3)$$

The above TENG operating equation leads to the circuit model shown in Fig. 3.1(b)) with a variable voltage source ($V_{oc}(t)$) in series with a variable capacitor ($C_T(t)$)[32].

As visualized in Fig. 3.1(c), we designate one extremity of TENG operation, where the two plates are in contact ($x(t) = 0$) as State I. While State II designates the other extremity of the TENG operation, where the two plates are maximally apart ($x(t) = x_{max}$). TENG electrical parameters V_{oc} and C_T at these two states are listed in Table 3.1. Further for analysis convenience, a system constant, ratio of maximum to minimum capacitance, is introduced:

$$\beta = \frac{C_{T,max}}{C_{T,min}} = \frac{x_{max} + d_{eff}}{d_{eff}} = \frac{x_{max}}{d_{eff}} + 1. \quad (3.4)$$

Table 3.1 TENG parameters at the operation extremes

Operation State	Airgap (x)	Capacitance (C_T)	Open-circuit voltage (V_{oc})
State I	$x_{min} = 0$	$C_{T,max} = \frac{\epsilon_0 A}{d_{eff}}$	$V_{oc,min} = 0$
State II	x_{max}	$C_{T,min} = \frac{\epsilon_0 A}{x_{max} + d_{eff}}$	$V_{oc,max} = \frac{\sigma x_{max}}{\epsilon_0}$

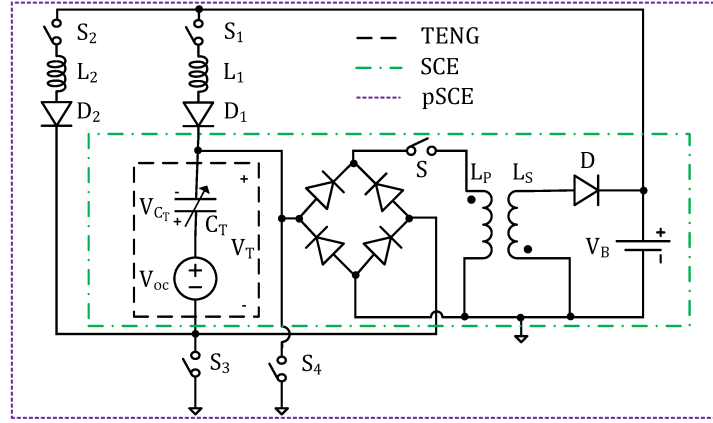


Figure 3.2 SCE and pSCE circuit diagram (SCE portion of pSCE is enclosed in the green box)

3.4 Synchronous Charge Extraction (SCE)

The circuit in the green box of Fig. 3.2 represents the SCE circuit obtained by cascading a full wave rectifier with the flyback converter [14, 17, 18]. With switch S open, TENG achieves its high open-circuit maximum voltage ($V_{oc,max}$). An efficient energy transfer is made possible by closing the switch S at the extremes (States I and II), thereby forming a L_P - C_T oscillator and enabling the transfer of C_T energy to L_P (in one-quarter of the oscillation cycle), and subsequently transferring that energy to the load through L_S . Here, we start by deriving the TENG voltage and charge at the extremes (States I and II) and use those to derive the per-cycle energy extracted, confirming that it equals the CMEO. This then serves as a baseline for comparing the achieved gain in the extracted energy when pre-biasing is incorporated.

3.4.1 SCE operation

The SCE circuit operation can be understood by following the operation cycle diagram of Fig. 3.3(a) and the TENG voltage waveform of Fig. 3.4(a). The cycle starts with the two plates pressed together ($x = 0$) with TENG voltage (V_T) and TENG capacitor charge (Q_{C_T}) being zero. The switch S is opened, and as the two plates are separated, TENG voltage increases with TENG operating in open-circuit condition. When the plates are maximally apart, V_T reaches the maxima, with Q_{C_T} still being zero. This is State II (right top of Fig. 3.3(a)), with:

$$V_T^{II} = V_{oc,max}; \quad Q_{C_T}^{II} = 0 \Rightarrow V_{C_T}^{II} = 0.$$

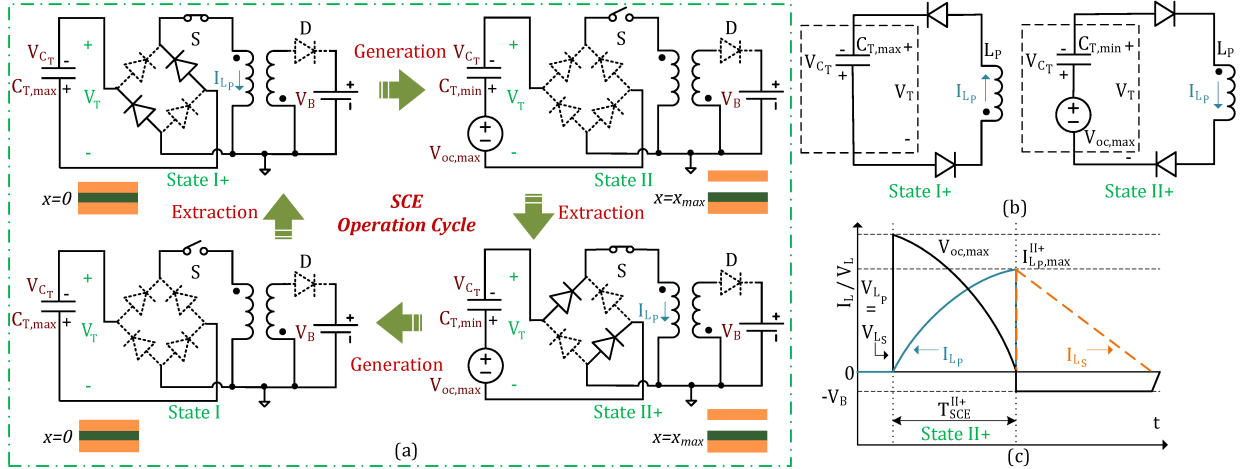


Figure 3.3 SCE Circuit (a) Operation cycle, (b) Simplified circuit during energy extraction States I+ and II+ and (c) Primary Inductor Current (I_{L_P}), Voltage (V_{L_P}) and, Secondary Inductor Current (I_{L_S}) during switching at State II.

At this point, switch S is closed resulting in State II+ (right bottom of Fig. 3.3(a)) and simplifying the circuit to a L_P - $C_{T,min}$ oscillator as shown in the right half of Fig. 3.3(b). Then, the differential equation evolution of the TENG capacitor voltage satisfies:

$$\frac{d^2 V_{C_T}(t)}{dt^2} + \frac{V_{C_T}(t)}{L_P C_{T,min}} - \frac{V_{oc,max}}{L_P C_{T,min}} = 0. \quad (3.5)$$

Above can be solved with initial condition as $V_{C_T}(0) = V_{C_T}^{II} = 0$ to obtain:

$$V_{C_T}(t) = -V_{oc,max} \cos(\omega_{SCE}^{II+} t) + V_{oc,max}; \quad \omega_{SCE}^{II+} = \frac{1}{\sqrt{L_P C_{T,min}}},$$

where ω_{SCE}^{II+} is the resonance frequency of the oscillator. Switch S is kept closed for one-fourth the L_P - $C_{T,min}$ oscillation cycle, yielding:

$$V_{C_T}^{II+} := V_{C_T} \left(\frac{\pi}{2\omega_{SCE}^{II+}} \right) = V_{C_T} \left(T_{SCE}^{II+} \right) = V_{oc,max},$$

where T_{SCE}^{II+} denotes the switch-closure time at State II. At this point, the TENG capacitor voltage is the opposite of the TENG voltage source, and the overall TENG voltage V_T^{II+} has dropped to zero (from the TENG operating equation (Eq. (3.3)). Then, the TENG capacitor charge $Q_{C_T}^{II+}$ can be derived as,

$$V_T^{II+} = V_{oc,max} - V_{C_T}^{II+} = V_{oc,max} - V_{oc,max} = 0; \quad Q_{C_T}^{II+} = C_T^{II+} V_{C_T}^{II+} = C_{T,min} V_{oc,max}. \quad (3.6)$$

Thus, during T_{SCE}^{II+} , the TENG voltage ($V_T(t)$) falls from the maxima ($V_{oc,max}$) to zero, while the current in the loop ($I_{L_P}(t)$) rises sinusoidally from zero to its maxima ($I_{L_P,max}^{II+}$) (refer to ‘blue’ curve of Fig. 3.3(c)). During this time period the current in the secondary inductor L_S is blocked by the reverse-biased diode D , with the energy transferred from TENG being stored as magnetic energy in the core of transformer. On opening the switch S after T_{SCE}^{II+} , the primary inductor current quickly falls to zero while the secondary inductor current shoots up to $I_{L_P,max}^{II+}$ (for turns ratio = 1), which in turn linearly decays to charge the load battery. Note that since the switching period T_{SCE}^{II+} is designed to be minuscule compared to the TENG operation period (T), the TENG capacitance $C_T(t)$ and open-circuit voltage $V_{oc}(t)$ are considered unchanged at $C_{T,min}$ and $V_{oc,max}$, respectively, during the switching period.

With the start of second half-cycle, upper plate moves downward with switch S open, to reach the starting position ($x = 0$) and State I is achieved (left bottom of Fig. 3.3(a)). Due to open-circuit operation, the charge on the TENG capacitor is retained from State II+, however the capacitance changes from $C_{T,min}$ to $C_{T,max}$, while the open-circuit voltage ($V_{oc}(t)$) falls to zero

(Fig. 3.1(c)). Thus,

$$\begin{aligned} Q_{C_T}^I &= Q_{C_T}^{II+} = C_{T,min} V_{oc,max}; \\ V_T^I &= V_{oc,min} - V_{C_T}^I = 0 - \frac{Q_{C_T}^I}{C_{T,max}} = -\frac{V_{oc,max}}{\beta}. \end{aligned} \quad (3.7)$$

To extract the TENG energy, switch S is closed for one-fourth the L_P - $C_{T,max}$ oscillation cycle, entering State I+ (left top of Fig. 3.3(a)), with oscillation frequency and switch S closure time given by,

$$\omega_{SCE}^{I+} = \frac{1}{\sqrt{L_P C_{T,max}}}; T_{SCE}^{I+} = \frac{\pi}{2\omega_{SCE}^{I+}} = \sqrt{\beta} T_{SCE}^{II+}. \quad (3.8)$$

With S closed, the SCE circuit is simplified to a L_P - $C_{T,max}$ oscillator as shown in the left half of Fig. 3.3(b). Similar to the energy extraction process during State II+, energy is transferred to the primary inductor, followed by to the secondary inductor (when S is opened T_{SCE}^{I+} time later), and then to the battery load. During the time switch S is closed, the TENG capacitor discharges through the primary inductor, and hence $V_{C_T}(t)$ falls to zero. This resets TENG for the start of the next cycle (and State I+ ends):

$$V_T^{I+} = V_{oc,min} - V_{C_T}^{I+} = 0 - 0 = 0; \quad Q_{C_T}^{I+} = 0.$$

3.4.2 Per-Cycle Energy Output

Cyclic TENG Voltage ($V_T(t)$) vs. TENG Capacitor Charge ($Q_{C_T}(t)$) diagram can be used to derive the per-cycle energy output (E_{cycle})[11]:

$$E_{cycle} = \int_0^T V_T I_T dt = \int_0^T V_T dQ_{C_T}. \quad (3.9)$$

Above equation shows that the energy output during the extraction step is equal to the area enclosed by the V_T curve against the Q_{C_T} axis. Using the TENG voltage (V_T) and capacitor charge (Q_{C_T}) derived at States I, I+, II and II+ in the above section, the V_T vs. Q_{C_T} plot for SCE is obtained as in Fig. 3.4(b). The first energy extraction step, at the end of the first half-cycle, II-II+, translates to a line with a slope of $-(C_{T,min})^{-1}$ enclosing the area of region ‘1’ in Fig. 3.4(b) equivalent to the extracted energy of E_{SCE}^I . While at the end of the second

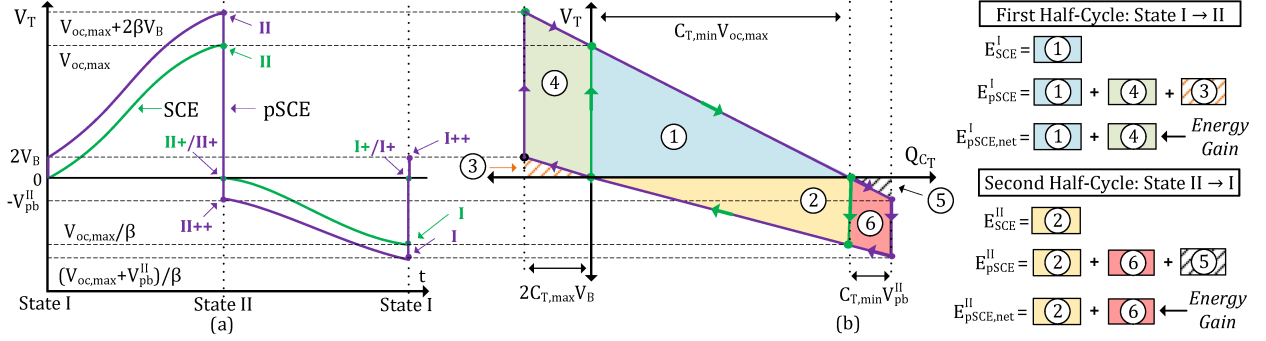


Figure 3.4 (a) TENG voltage waveform plot (green under SCE vs. purple under pSCE). End of different circuit operation states are marked on both the waveforms. (b) TENG voltage vs. charge ($V_T - Q_{C_T}$) plot for SCE (areas 1-2) and pSCE (areas 1-6).

half-cycle, I-I+ step with a slope of $(C_{T,max})^{-1}$ extracts energy E_{SCE}^{II} equal to the area of region '2'. The energy output found by computing the enclosed triangular areas of the regions '1' and '2' in Fig. 3.4(b) are stated below:

$$E_{SCE}^I = \frac{1}{2} \times C_{T,min} V_{oc,max} \times V_{oc,max}; \quad E_{SCE}^{II} = \frac{1}{2} \times C_{T,min} V_{oc,max} \times \frac{V_{oc,max}}{\beta};$$

$$E_{SCE} = E_{SCE}^I + E_{SCE}^{II} = \frac{1}{2} \left(1 + \frac{1}{\beta} \right) C_{T,min} V_{oc,max}^2. \quad (3.10)$$

Remark 1 The V_T vs. Q_{C_T} plot for SCE cycle matches that of CMEO [11, 14]. Thus, all *passive* EECs i.e., without pre-biasing, are limited to the area enclosed by the SCE's V_T vs. Q_{C_T} trapezoid, and in this sense, SCE is optimal among all the passive EECs. Also, SCE's energy output (Eq. (4.8)) is independent of the load voltage value, which is another desirable feature eliminating the need for complex and power-intensive Maximum Power Point Tracking (MPPT).

3.5 Synchronous Pre-biasing for Enhanced Extraction

Synchronous pre-biasing refers to charging the TENG capacitor before the start of each half-cycle to possibly increase the energy output beyond the SCE output (CMEO). In this

section, the electromechanical energy transduction at each step of the SCE circuit is first analyzed to motivate and quantify the effect of the proposed pre-biasing.

3.5.1 First half-cycle

For the SCE circuit, starting at State I+ ($x = 0$), the charge on the TENG capacitor is zero ($Q_{C_T}^{I+} = 0$). Hence, the charge on the TENG's upper plate (Q_1^{I+}) and the lower plate (Q_2^{I+}) are given by,

$$Q_1^{I+} = Q_{T,1} - Q_{C_T}^{I+} = \sigma A; \quad Q_2^{I+} = -Q_1^{I+} = -\sigma A. \quad (3.11)$$

In transitioning from State I+ ($x = 0$) to State II ($x = x_{max}$), external mechanical excitation moves up the upper plate against the electrostatic force of attraction (F_e^I) acting on it (Refer Fig. 3.5(a)). Noting that the electric field due to the bottom plate that acts on the charges of the upper plate is $\frac{1}{2}\vec{E}_\sigma$, using Eq. (3.1), we get:

$$\begin{aligned} \vec{F}_e^I &= \frac{1}{2}\vec{E}_\sigma Q_1^{I+} = -\frac{1}{2} \left(\frac{\sigma}{\epsilon_0} \vec{1}_x \right) (\sigma A) = -\frac{1}{2} \left(\frac{\sigma^2 A}{\epsilon_0} \right) \vec{1}_x; \\ W_e^I &= \int_0^{x_{max}} \vec{F}_e^I \cdot d\vec{x} = -\frac{1}{2} \left(\frac{\sigma^2 A}{\epsilon_0} \right) x_{max} = -\frac{1}{2} \left(\frac{(Q_1^{I+})^2}{\epsilon_0 A} \right) x_{max} \\ &= -\frac{1}{2} \left(\frac{\beta}{\beta - 1} \right) C_{T,min} V_{oc,max}^2, \end{aligned} \quad (3.12)$$

where to derive the last equality, we use the defining equations of $C_{T,min}$, $V_{oc,max}$, and β from Table 3.1 and Eq. (3.4), respectively. The work W_e^I done by the mechanical source (and stored as electrical potential energy) is proportional to the electrostatic force, which in turn is proportional to the square of the upper electrode charge ($(Q_1^{I+})^2$). Thus, by pre-biasing (i.e., adding extra charge) the TENG at State I+, Q_1^{I+} can be increased to in turn increase the transduced energy. This establishes the motivation behind pre-biasing, and in the following section, we quantify this energy gain for the proposed pSCE circuit.

Remark 2 It is clear that the transduced energy in the first half-cycle will continue to increase on increasing the pre-bias charge. In practice, the upper limit may be set by the level of available external mechanical force (equivalently acceleration). For a given periodic mechanical force with

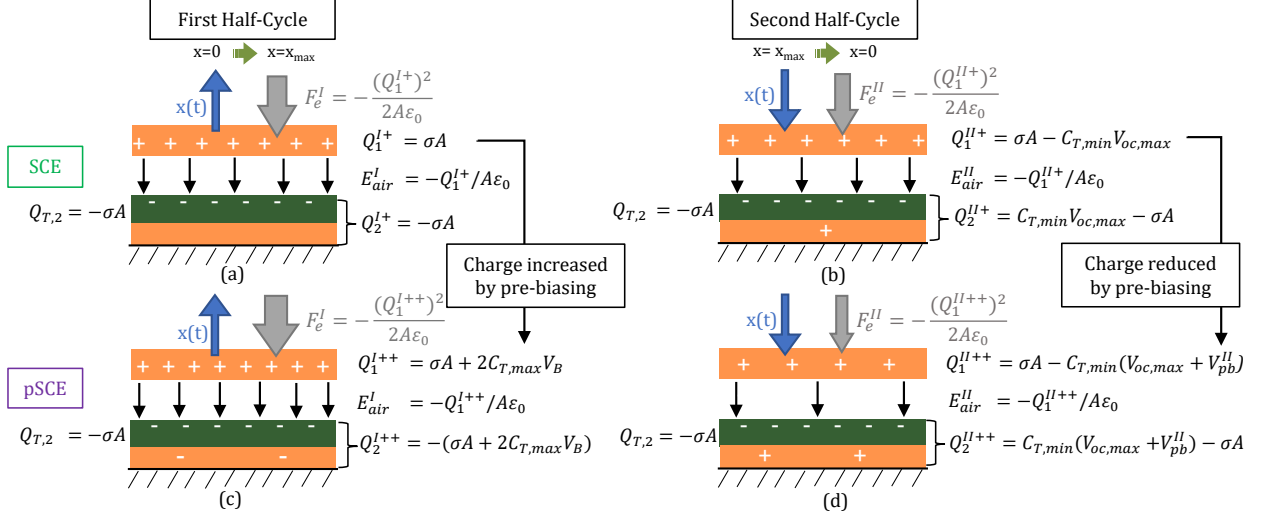


Figure 3.5 TENG schematic depicting mechanical motion ($x(t)$) and electrostatic force (F_e) with the SCE circuit during (a) separation of TENG plates, i.e., first half-cycle and (b) retraction of the plates, i.e., second half-cycle. Comparative plots for the pSCE circuit during the (c) first half-cycle with relatively increased F_e and (d) second half-cycle with relatively reduced F_e .

fixed acceleration, increasing the level of pre-biasing will increase the countering electrostatic force that will eventually reduce the maximum reachable separation between the two plates (x_{max}) and, as a result, decrease the TENG's maximum open-circuit voltage ($V_{oc,max}$). This feedback effect of the electrostatic force in a vibration-driven electrostatic transducer on its mechanical motion and the transduced energy has been previously studied in works such as [33, 34]. In a typical TENG application with a moving part (upper plate in our case) of mass m , the deceleration due to electrical attraction (F_e/m) is an order or two lower in magnitude than the external mechanical acceleration. For example, human walking provides $2\text{--}3 \text{ ms}^{-2}$ acceleration, while a car engine compartment provides 12 ms^{-2} [35]. In contrast, for the TENG used in this work (moving mass, $m = 113.7\text{g}$), the electrical deceleration is 0.013 ms^{-2} with no pre-biasing (SCE operation) and 0.026 ms^{-2} when pre-biased at 30 V as derived in Appendix 3.12. Thus, pre-biasing does not overpower the mechanical acceleration to cause an appreciable reduction in x_{max} value. Thereby in most mesoscale implementations, the pre-biasing

level is limited only by the upper limit of the voltage source available for pre-biasing, the voltage ratings of the circuit components, or air electric field breakdown.

3.5.2 Second half-cycle

At the end of the first half-cycle, part of the transduced energy is extracted and delivered to the load (E_{SCE}^I), while part of it remains stored on the TENG capacitor. The charge on the upper plate at this stage, i.e., at State II+ (Q_1^{II+}) can be found using Eq. (4.7):

$$Q_1^{II+} = Q_{T,1} - Q_{C_T}^{II+} = \sigma A - C_{T,min} V_{oc,max}. \quad (3.13)$$

With the start of the second half-cycle, as shown in Fig. 3.5(b), the direction of upper plate motion is reversed to match that of electrostatic force. This results in positive work, i.e., a part of stored TENG capacitor energy is dissipated back into the environment. This energy loss can be derived similarly to Eq. (3.12):

$$W_e^{II} = \frac{1}{2} \left(\frac{(Q_1^{II+})^2}{\epsilon_0 A} \right) x_{max} = \frac{1}{2} \left(\frac{(\sigma A - C_{T,min} V_{oc,max})^2}{\epsilon_0 A} \right) x_{max} = \frac{1}{2} \left(\frac{1}{\beta(\beta-1)} \right) C_{T,min} V_{oc,max}^2. \quad (3.14)$$

In the entire cycle, the net work done (the work done in the first half cycle minus the energy lost in the second half cycle) is extracted. Indeed adding the above energy loss W_e^{II} (Eq. (3.14)) to the extracted energy E_{SCE} (Eq. (4.8)) gives us the transduced energy of the first cycle W_e^I (Eq. (3.12)). Since, the three multipliers of the common term $\frac{1}{2} C_{T,min} V_{oc,max}^2$ appearing in W_e^{II} , E_{SCE} , W_e^I satisfy:

$$\left(\frac{1}{\beta(\beta-1)} \right) + \left(1 + \frac{1}{\beta} \right) = \left(\frac{\beta}{\beta-1} \right) \Rightarrow |W_e^{II} + E_{SCE}| = |W_e^I|,$$

verifying the energy balance. We make a note that this the first time such an energy balance among the mechanical energy transduced, mechanical energy lost, and the electrical energy extracted for a TENG with SCE as EEC has been demonstrated to the best of our knowledge. For reducing the above energy loss to zero, the pre-biasing charge should be added to turn the

plate charges ($Q_1^{II+} = -Q_2^{II+}$) to zero. Using Eq. (3.13),

$$\begin{aligned}
 Q_1^{II+} = 0 &\Rightarrow \sigma A - C_{T,min} V_{oc,max} - Q_{pb,opt}^{II} = 0 \\
 &\Rightarrow V_{pb,opt}^{II} := \frac{Q_{pb,opt}^{II}}{C_{T,min}} = \frac{\sigma A}{C_{T,min}} - V_{oc,max} \\
 &\Rightarrow V_{pb,opt}^{II} = \frac{V_{oc,max}}{\beta - 1}.
 \end{aligned} \tag{3.15}$$

However, pre-biasing voltage beyond twice the above derived optimum value ($V_{pb,opt}^{II}$) would decrease the upper plate charge below $-\left[\sigma A - C_{T,min} V_{oc,max}\right]$, increasing the electrostatic attraction between the TENG plates beyond SCE, thereby causing a higher loss to the environment in the second half-cycle than that of SCE. Thus,

$$V_{pb,u}^{II} := 2V_{pb,opt}^{II} = \frac{2V_{oc,max}}{\beta - 1} \tag{3.16}$$

provides the upper limit to pre-biasing in the second half cycle for it to remain favorable over SCE. In contrast, pre-biasing is always favorable in the first half-cycle and also overall, combining the two cycles, as demonstrated in the next section.

3.6 Proposed pSCE Circuit Analysis

Here we describe the proposed circuit that is used for pre-biasing the TENG at the start of each half-cycle. To enable the same with either polarity, four additional switches S1-S4 configured as H-bridge are added to the SCE circuit architecture (Fig. 3.2).

3.6.1 pSCE operation

pSCE operation is obtained by extending the SCE operation discussed above with two added states for pre-biasing at the start of each half-cycle: State I++ (following I+) and State II++ (following II+). Circuit operation can be understood by following the operation cycle diagram of Fig. 3.7 and TENG voltage waveform of Fig. 3.4(a). As in SCE, the operation commences at $x = 0$, with all switches open and $V_{oc} = 0$ (State I+). Then for pre-biasing, switches S1 and S3 are closed (State I++ at the left top in Fig. 3.7) to form the pre-bias charging loop,

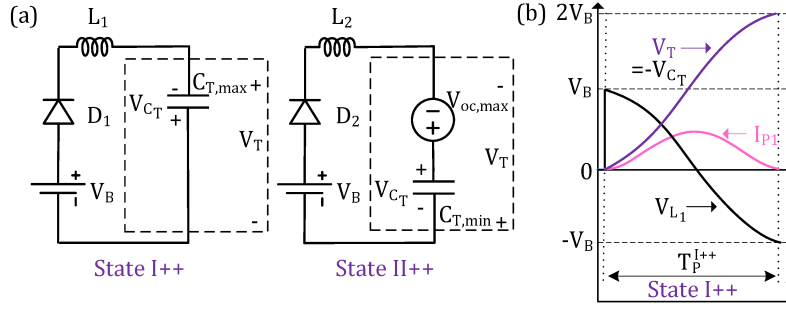


Figure 3.6 pSCE circuit (a) Simplified circuit during pre-biasing at start of both the half-cycle and (b) L_1 inductor voltage (V_{L1}), pre-biasing loop current (I_{P1}) and, TENG voltage (V_T) during pre-biasing State I++.

$V_B - S_1 - L_1 - D_1 - C_T - S_3$ with the circuit simplified to a L_1 - $C_{T,max}$ oscillator as shown in the left half of Fig. 3.6(a). The corresponding circuit differential equation is similar to Eq. (4.10).

The TENG capacitor voltage $V_{C_T}(t)$ with initial condition $V_{C_T}(0) = I_{C_T}(0) = 0$ is obtained as,

$$V_{C_T}(t) = V_B(\cos(\omega_P^{I++}t)) - V_B; \quad \omega_P^{I++} = \frac{1}{\sqrt{L_1 C_{T,max}}}.$$

On enabling S1 and S3 for half the oscillation cycle (denoted T_P^{I++}), the TENG capacitor voltage reaches $-2V_B$:

$$V_{C_T}^{I++} := V_{C_T}\left(\frac{\pi}{\omega_P^{I++}}\right) = V_{C_T}\left(T_P^{I++}\right) = -2V_B.$$

Using the TENG operating equation (Eq. (3.3)), with $V_{oc} = 0$,

$$V_T^{I++} = -\frac{Q_{C_T}^{I++}}{C_{T,max}} = 2V_B \Rightarrow Q_{C_T}^{I++} = -2C_{T,max}V_B. \quad (3.17)$$

Thus, using the L_1 - C_T resonance, the pre-biasing voltage is passively boosted to twice the pre-biasing source (battery) voltage by introducing the extra inductor L_1 (correspondingly L_2 for the second half-cycle). At this point, the two plates separate with switch S open, and TENG voltage increases to reach its maxima at State II. As no current has flown through TENG since the last state, $Q_{C_T}^{II} = Q_{C_T}^{I++}$. Hence,

$$V_T^{II} = V_{oc,max} - \frac{Q_{C_T}^{II}}{C_{T,min}} = V_{oc,max} + 2\beta V_B. \quad (3.18)$$

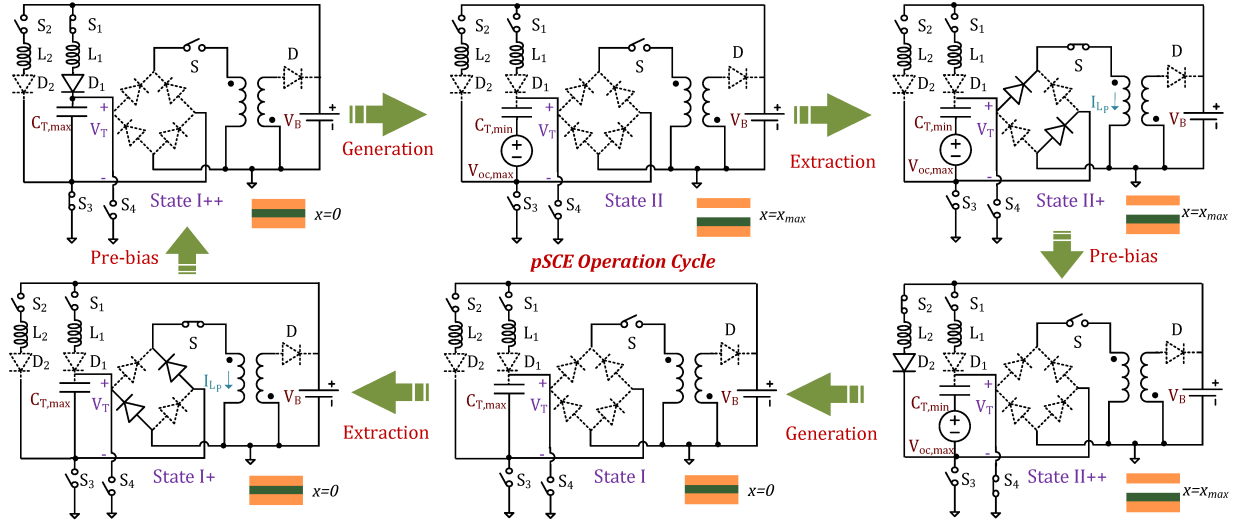


Figure 3.7 The proposed pSCE circuit's operation cycle.

Note the increase in the voltage by $2\beta V_B$ compared to the SCE circuit. At this stage, similar to the SCE circuit, switch S is closed for one-fourth the L_P - $C_{T,min}$ oscillation cycle (T_{SCE}^{II+}) to achieve State II+. TENG voltage falls to zero, and the energy is transferred to the primary inductor L_p , which is subsequently transferred to the load via secondary inductor L_S . With the first half-cycle complete, similar to the State I++ operation, the State II++ operation is performed to pre-bias the TENG by closing S2 and S4 (right bottom in Fig. 3.7) to form the $V_B - S_2 - L_2 - D_2 - C_T - S_4$ loop, with the circuit simplified to a L_2 - $C_{T,min}$ oscillator as shown in the right half of Fig. 3.6(a). With initial conditions: $V_{C_T}(0) = V_{oc,max}$; $I_{C_T}(0) = 0$, the TENG capacitor satisfies:

$$V_{C_T}(t) = V_B(1 - \cos(\omega_P^{II++}t)) + V_{oc,max};$$

$$\omega_P^{II++} = \frac{1}{\sqrt{L_2 C_{T,min}}}.$$

Since $V_{C_T}(t)$ oscillates between $V_{oc,max}$ and $V_{oc,max} + 2V_B$, the TENG voltage $V_T(t) = V_{oc,max} - V_{C_T}(t)$ oscillates between 0 and $-2V_B$. Thus by controlling the duration over which S2 and S4 are closed, i.e., the duration of pre-biasing, the TENG voltage can be set to any

value $-V_{pb}^{II}$ such that $-2V_B \leq -V_{pb}^{II} \leq 0$ (Refer Appendix 3.13 for further explanation). Then,

$$V_T^{II++} = V_{oc,max} - \frac{Q_{C_T}^{II++}}{C_{T,min}} = -V_{pb}^{II} \Rightarrow Q_{C_T}^{II++} = C_{T,min}(V_{oc,max} + V_{pb}^{II}). \quad (3.19)$$

Next, as per the periodic motion, the plates come together ($x = 0$) as in State I. Since the TENG is in open-circuit condition during this movement, $Q_{C_T}^I = Q_{C_T}^{II++}$. Hence,

$$V_T^I = -\frac{Q_{C_T}^I}{C_{T,max}} = -\frac{V_{oc,max} + V_{pb}^{II}}{\beta}. \quad (3.20)$$

Again, at this stage, the TENG voltage is higher (in absolute terms) over the SCE circuit (see Eq. (3.7)), meaning larger energy will be recovered in going from State I to State I+. Next, the switch S is closed for one-fourth the L_p - $C_{T,max}$ oscillation cycle, i.e., for T_{SCE}^{I+} to extract the energy from TENG (State I+ at the left bottom in Fig. 3.7). TENG voltage falls to zero, completing one full operation cycle.

3.6.2 Per-Cycle Energy Output

As with the case of SCE per-cycle energy output calculation, we plot the TENG voltage (V_T) and TENG capacitor charge (Q_{C_T}), derived above, at different states to obtain the V_T - Q_{C_T} plot of Fig. 3.4(b). Note due to pre-biasing, the trapezoidal area of SCE extends on both sides (beyond the regions labeled '1' and '2' of SCE), adding the regions labeled as '3', '4', '5', and '6'. The pre-biasing adds charge $-2C_{T,max}V_B$ raising TENG voltage to $2V_B$ during State I++ (Eq. (3.17)), while during State II++ adds charge $C_{T,min}V_{pb}^{II}$ lowering TENG voltage to $-V_{pb}^{II}$ (Eq. (3.19)). As a result, the energy extracted at the end of the first half-cycle (E_{pSCE}^I) is equal to the triangular area enclosed by the extraction step, namely, State II to II+ line, and the Q_{C_T} axis (areas '1'+ '3'+ '4'). Similarly, energy extracted at the end of the second half cycle (E_{pSCE}^{II}) is the triangular area between State I to I+ line and the Q_{C_T} axis (areas '2'+ '5'+ '6'):

$$\begin{aligned} E_{pSCE}^I &= \frac{1}{2} \times C_{T,min}(V_{oc,max} + 2\beta V_B) \times (V_{oc,max} + 2\beta V_B); \\ E_{pSCE}^{II} &= \frac{1}{2} \times C_{T,min}(V_{oc,max} + V_{pb}^{II}) \times \frac{(V_{oc,max} + V_{pb}^{II})}{\beta}. \end{aligned} \quad (3.21)$$

The energy consumed from the load battery for the TENG pre-biasing at the start of each half-cycle is equal to the product of the battery voltage and the charge flow during the pre-biasing periods. The consumed pre-biasing energy for the first half-cycle ($E_{pre-bias}^I$) and that for the second half-cycle ($E_{pre-bias}^{II}$) are thus respectively equal to the areas marked as ‘3’ and ‘5’ on the V_T - Q_{C_T} plot of Fig. 3.4(b):

$$E_{pre-bias}^I = 2C_{T,max}V_B^2 = 2\beta C_{T,min}V_B^2; \quad E_{pre-bias}^{II} = \frac{1}{2}C_{T,min}(V_{pb}^{II})^2. \quad (3.22)$$

Since the total extracted energy is the sum of areas ‘1’ through ‘6’, it can be said that the “invested energy” of ‘3’+‘5’ is recouped with a “return on investment” (in addition to the SCE output of ‘1’+‘2’) as ‘4’+‘6’. Now individually, the net energy delivered to the battery load in the two half-cycles obtained by deducting the respective pre-biasing energy from the extracted energy can be expressed as,

$$\begin{aligned} E_{pSCE,net}^I &= \frac{1}{2}C_{T,min}[(V_{oc,max} + 2\beta V_B)^2 - 4\beta V_B^2]; \\ E_{pSCE,net}^{II} &= \frac{1}{2}C_{T,min}\left[\frac{(V_{oc,max} + V_{pb}^{II})^2}{\beta} - (V_{pb}^{II})^2\right]. \end{aligned} \quad (3.23)$$

Sum of the above two equals the area enclosed by the pSCE operation (regions ‘4’+‘1’+‘2’+‘6’) on the V_T - Q_{C_T} plot of Fig. 3.4(b) and represents the net per-cycle energy extracted from TENG,

$$E_{pSCE,net} = \frac{1}{2}C_{T,min}[(V_{oc,max} + 2\beta V_B)^2 + \frac{(V_{oc,max} + V_{pb}^{II})^2}{\beta} - 4\beta V_B^2 - (V_{pb}^{II})^2]. \quad (3.24)$$

3.6.3 Conditions for Pre-biasing

For the first half-cycle, **Remark 2** above discussed that compared to the SCE operation, pre-biasing increases the transduced energy which can now be verified from energy point of view by showing that $E_{pSCE,net}^I$ at any arbitrary pre-biasing voltage (substituting V_{pb}^I for $2V_B$ in Eq. (3.23)) is greater than E_{SCE}^I (Eq. (4.8)) and continues to increase with V_{pb}^I :

$$\begin{aligned} E_{pSCE,net}^I - E_{SCE}^I &\geq 0 \Leftrightarrow [(V_{oc,max} + \beta V_{pb}^I)^2 - \beta (V_{pb}^I)^2] - V_{oc,max}^2 \geq 0 \\ &\Leftrightarrow \beta [2V_{oc,max} + (\beta - 1)V_{pb}^I] V_{pb}^I \geq 0. \end{aligned}$$

Since $\beta \geq 1$, the above inequality clearly holds, where the left hand side is an increasing function of V_{pb}^I (higher the pre-biasing; higher the gain).

For the second half-cycle, we noted in Sec. 3.5.2 that pre-biasing beyond a limit increases the energy loss to the environment, so it becomes higher than the corresponding energy loss of SCE. The same limit on the load voltage, beyond which it is preferable to skip pre-biasing for the second half-cycle, can be derived by way of energy considerations:

$$\begin{aligned}
 E_{pSCE,net}^{II} - E_{SCE}^{II} &\geq 0 \\
 \Leftrightarrow \left[\frac{(V_{oc,max} + V_{pb}^{II})^2}{\beta} - (V_{pb}^{II})^2 \right] - \frac{V_{oc,max}^2}{\beta} &\geq 0 \Leftrightarrow 2V_{oc,max} - (\beta - 1)V_{pb}^{II} \geq 0 \\
 \Leftrightarrow V_{pb}^{II} &\leq \frac{2V_{oc,max}}{(\beta - 1)} =: V_{pb,u}^{II}. \quad (3.25)
 \end{aligned}$$

This condition obtained based on energy considerations matches the condition of Eq. (3.16) that was derived using the level of charge on the two plates (and the corresponding level of electrostatic attraction), providing a correctness check to our derivations. Differentiating the above gain of pSCE circuit over SCE in the second half-cycle ($E_{pSCE,net}^{II} - E_{SCE}^{II}$) with respect to V_{pb}^{II} and equating it to zero provides the optimum level of pre-biasing as,

$$V_{pb,opt}^{II} = \frac{V_{oc,max}}{(\beta - 1)}, \quad (3.26)$$

which is again consistent with the result of Eq. (3.15) derived from the charges/forces perspective in Sec. 3.5.2.

Another novel result can be deduced by mapping the derived optimal battery voltage value $V_{pb,opt}^{II}$ to the TENG parameters:

$$V_{pb,opt}^{II} = \frac{V_{oc,max}}{\beta - 1} = \frac{\frac{\sigma x_{max}}{\epsilon_0}}{\frac{x_{max} + d_{eff}}{d_{eff}} - 1} = \frac{\sigma d_{eff}}{\epsilon_0},$$

a constant value for a given TENG. This implies that the optimal load voltage $V_{pb,opt}^{II}$ does not depend on the operation parameters such as amplitude (x_{max}) or operation frequency, and as such, no dynamic closed-loop control is required to adjust the pre-biasing voltage for optimized pSCE operation.

Remark 3 Since $V_{pb,opt}^{II} < V_{pb,u}^{II}$ (the former is the half of the latter), it follows that it is favorable to operate at the optimum pre-bias level of $V_{pb,opt}^{II}$ in the second half cycle whenever it is feasible. So if $V_{pb,opt}^{II} \leq 2V_B$, then in the second half cycle, one would pre-bias the TENG to the voltage $-V_{pb,opt}^{II}$ by appropriately controlling the on-time of the switches S2 and S4 (note as discussed just prior to Eq. (3.19), it is possible to pre-bias the TENG voltage to as low as $-2V_B$). On the other hand, in the sub-optimal case of $2V_B < V_{pb,opt}^{II}$, the best one can do in the second half cycle from the energy perspective is to pre-bias the TENG to the voltage $-2V_B$. We next show that even in the sub-optimal operation of the second half cycle (namely, pre-biasing TENG voltage to $-2V_B$ in all cases), the net energy gain of pSCE over SCE in the combined two half-cycles is positive for any V_B value. This can be seen from the following sequence of equivalences:

$$\begin{aligned}
& \left[E_{pSCE,net} |_{V_{pb}^{II}=2V_B} \right] - E_{SCE} \geq 0 \\
& \Leftrightarrow (V_{oc,max} + 2\beta V_B)^2 + \frac{(V_{oc,max} + 2V_B)^2}{\beta} \\
& \quad - 4(1 + \beta)V_B^2 - \left(1 + \frac{1}{\beta}\right) V_{oc,max}^2 \geq 0 \\
& \Leftrightarrow \left(\beta + \frac{1}{\beta}\right) V_{oc,max} + (\beta - 1) \left(\beta - \frac{1}{\beta}\right) V_B \geq 0.
\end{aligned} \tag{3.27}$$

By definition, $\beta \geq 1$ and thus, the above condition is satisfied at all load values for any given TENG. Also, in the final inequality of Eq. (3.27), the left-hand side is an increasing function of V_B , implying that the energy gain of the pSCE circuit over the SCE circuit shall continue to rise with increasing value of V_B . Thus, barring an eventual reduction in x_{max} due to the increased pre-biasing or air electric field breakdown (as discussed earlier in **Remark 2**), there is no other upper limit on V_B as far as being able to boost the energy output through pre-biasing.

Pre-biasing to a level higher than the presented design's upper limit of twice the battery voltage ($\pm 2V_B$) is also possible, but only at the added energy cost of DC/DC boosting. It is an easy exercise to check if the *net* energy gain by introducing such a boosted pre-biasing would be positive for a given TENG, and if so, a DC/DC boost can be integrated if the application can afford its added area.

Remark 4 While our paper proposes and derives results for pre-biasing the TENG operating in the generic contact-separation mode, the results are also valid for the lateral sliding mode TENG, which has similar time-varying capacitance and open-circuit voltage characteristics [2]. However, for the freestanding mode TENG, wherein a dielectric plate oscillates in the air-gap of two stationary metal electrodes, the capacitance is fixed and hence $\beta = 1$ [2]. In this case, both the half-cycles (upward and downward stroke of the dielectric plate) are symmetric and both transduce energy from the mechanical source and in that sense, are similar to the above described contact-separation mode TENG's first half-cycle. Thus, in line with **Remark 2**, synchronous pre-biasing can also be used for the freestanding mode TENG to increase the net energy extracted, and as such, no upper limit exists on the level of pre-biasing (other than that imposed by the breakdown voltage of the operating medium).

3.7 Circuit Implementation

The proposed pSCE circuit's implementation with MOSFET switches is shown in Fig. 3.8(a). The SCE circuit is implemented in a similar fashion, minus the H-bridge portion of the pSCE.

3.7.1 Switching controller

The pSCE circuit operates by switching at the extrema (States I and II), with the NMOS switches receiving the signal from the control circuit. Fig. 3.8(b) shows the control circuit that comprises of a peak detector and four pulse generators that issues gate pulse V_G for switching S and achieving the energy extraction States I+ and II+, V_{G1} for switching S1 and S3 and achieving pre-biasing State I++, and V_{G2} for switching S2 and S4 and achieving pre-biasing State II++.

The peak detector identifies the operation extrema by tracking the output voltage of an electrically isolated auxiliary TENG (Aux-TENG) built with a fraction of area compared to the main TENG that operates synchronously in parallel to the main TENG as schematized in Fig. 3.8(c). The output voltage V_T' of Aux-TENG is differentiated by the CR circuit (V_{DT}'), to convert the signal peaks into zero crossings, which trigger state change of the comparator output

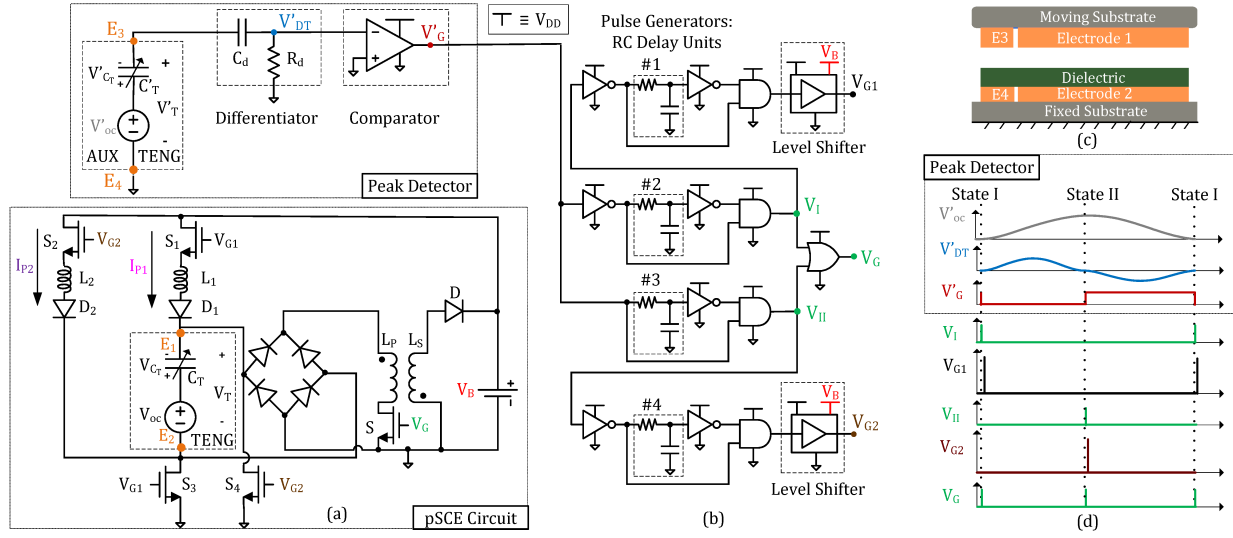


Figure 3.8 (a) pSCE circuit implementation (b) Control circuit with peak detector and four pulse generators (c) Cross-section diagram of TENG showing parallel isolated Aux-TENG (d) Schematic of control circuit waveforms

V'_G , at States I and II as schematized in Fig. 3.8 (d). Independent Aux-TENG is used as an input for the control circuit as opposed to the rectified voltage of the main TENG to be able to distinguish State I from State II and accordingly set the switching time T_{SCE}^{I+} or T_{SCE}^{II+} (Eq. (3.8)) for switch S, and additionally enable either pair of switches (S1,S3) or (S2,S4) to pre-bias the TENG with the correct polarity. Use of Aux-TENG also avoids loading of the main TENG by the control circuit and subsequent interference. Further, four pulse generating arms of the circuit are designed to generate a pulse at the rising edge of the input: Arm 3 receives the comparator output and generates a pulse at State II (V_{II}). Similarly, Arm 2 generates the pulse at State I (V_I) on receiving the inverted comparator output. The pulse width is set by the RC product of the respective delay unit. It is set to T_{SCE}^{I+} and T_{SCE}^{II+} for the Arms 2 and 3, respectively. Both these signals are combined through OR gate to produce signal V_G for the NMOS S. Arm 1 is used to generate a pulse for switching on NMOS S1 and S3 (V_{G1}) at the falling edge of the signal V_I for the follow-up pre-biasing of State I++. The source of S1 reaches voltage up to V_B by the end of the pre-biasing action, hence to keep it turned on, the signal (V_{G1}) is shifted up from control

circuit supply voltage V_{DD} to V_B using the voltage level shifter. The pulse width of this signal should be greater than or equal to half the L_1 - $C_{T,max}$ resonator cycle (T_P^{I++}) to complete the pre-biasing action. At the end of the half-cycle, the current direction reverses and is automatically cut-off due to diode D_1 in the loop. Similarly, V_{G2} is generated using Arm 4 to switch on NMOS S2 and S4 for the pre-biasing step of State II++. Note that the SCE circuit too operates with the same switching controller of Fig. 3.8(a) barring the Arms 3 and 4 of the circuit.

3.7.1.1 Control Circuit Delay

Here we quantify the control circuit's time delay in detecting the TENG operation extremes, and show how it is orders of magnitude lower than the TENG's operation cycle time and hence has a negligible impact on its overall performance. The consequential source of delay is the peak detector's CR differentiator, introducing a quarter-cycle delay to attain the zero crossings at States I and II. Referring to the circuit of Fig. 3.8(b), the Aux-TENG is connected in series with resistor R_d and a small valued capacitor C_d (of the order of 1 pF) compared to the minimum Aux-TENG capacitance rendering the effective series capacitance as $\sim C_d$. The amplitude ($|V'_{DT}|$) and phase (θ) of the voltage across R_d that is input to the comparator can be derived as:

$$\begin{aligned} |V'_{DT}| &= \left(\frac{V'_{oc,max}}{2} R_d \right) \frac{\omega_{ext} C_d}{\sqrt{1 + (\omega_{ext} R_d C_d)^2}}; \\ \theta &= \arctan \left(\frac{1}{\omega_{ext} R_d C_d} \right) = \frac{\pi}{2} - \arctan(\omega_{ext} R_d C_d) \end{aligned} \quad (3.28)$$

Here, ω_{ext} is the external (mechanical) operation frequency. The offset $\arctan(\omega_{ext} R_d C_d)$ to $\pi/2$ in θ is the undesirable delay that can be written in time difference/delay (t_d) form as:

$$t_d = \frac{\arctan(\omega_{ext} R_d C_d)}{\omega_{ext}} \approx R_d C_d$$

Clearly, this delay can be minimized by reducing the $R_d C_d$ product. With a typical choice of $C_d = 1$ pF, a R_d of the order of 100 M Ω is sufficient to produce large enough output ($|V'_{DT}| \propto V'_{oc,max} R_d C_d$ by Eq. (3.28)) to trigger the zero-crossing in the comparator. The above choice translates to a delay of the order of ~ 10 μ s that is negligible compared to TENG

operating time period (100 ms corresponding to operation frequency of 10 Hz for this work). The propagation delay added by the comparator and other logic gates is again of the order of a few μs . Thus, the control circuit's time delay is safely ignored for analysis purposes.

3.7.2 Impact of circuit non-idealities

In practical implementation of the SCE/pSCE circuit, different circuit parasitic losses impact the energy delivered to the load as computed using the $V_T-Q_{C_T}$ plot in the above sections, which we describe next.

3.7.2.1 Conduction Loss

Firstly, in the SCE circuit, the resistive losses occur due to the series parasitic inductor resistance and the on-state resistance of switch S, during the two energy extraction steps of States I+ and II+. The full derivation of per-cycle energy delivered to the load with consideration of the resistive loss is provided in Appendix 3.14. In brief, this loss due to cumulative series resistance, denoted R_S , can be modeled by defining the series quality factor (Q_f) of the $L_P C_T$ resonator loops formed by closing switch S for energy extraction. For convenience, we use the “normalized” forms $0 < \alpha^I < 1$ and $0 < \alpha^{II} < 1$ of the quality factors during State I+ and II+, respectively, as defined below:

$$\begin{aligned}\alpha^I &:= e^{\frac{-\pi}{2Q_f^I}}; Q_f^I := \frac{\omega_d^I L_P}{R_S}, \omega_d^I := \sqrt{\frac{1}{L_P C_{T,max}} - \frac{R_S^2}{4L_P^2}}; \\ \alpha^{II} &:= e^{\frac{-\pi}{2Q_f^{II}}}; Q_f^{II} := \frac{\omega_d^{II} L_P}{R_S}, \omega_d^{II} := \sqrt{\frac{1}{L_P C_{T,min}} - \frac{R_S^2}{4L_P^2}}.\end{aligned}$$

Now, the per-cycle energy delivered to the load can be stated as (see Eq. (3.35) of Appendix 3.14):

$$E_{SCE} = \frac{1}{2} \left(\frac{\alpha^I}{\beta} + \alpha^{II} \right) C_{T,min} V_{oc,max}^2.$$

Here, while the two diode voltage drops ($2V_D$) in the FWR of the SCE circuit has been ignored due to high voltage nature of the TENG, it can be easily incorporated in the derivation.

Note since the SCE circuit acts as the extraction circuit in the pSCE operation, the conduction loss of pSCE during the energy extraction steps (marked as “Loss 2” in the energy

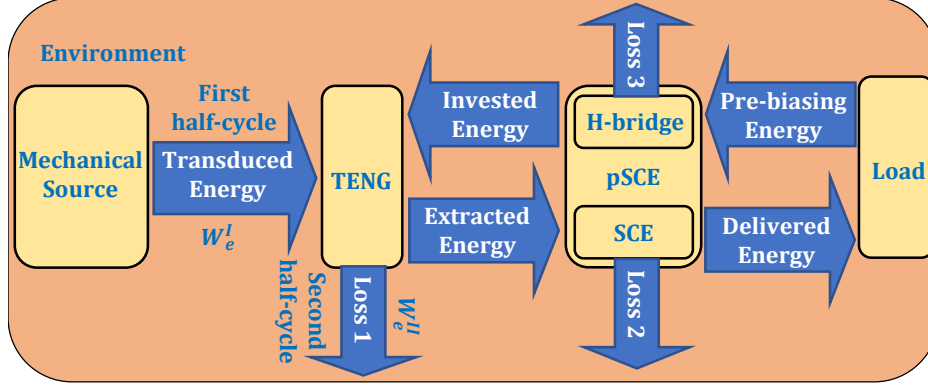


Figure 3.9 Energy flow diagram for the pSCE operation. Loss 1 is electrostatic environmental loss while Loss 2 and 3 are parasitic conduction losses.

flow diagram of Fig. 3.9) can be modeled similar to the SCE circuit already presented above. The additional losses in the two pre-biasing paths of $S_1 - L_1 - S_3$ and $S_2 - L_2 - S_4$ (“Loss 3” in Fig. 3.9) need to be incorporated as well. Letting $L_1 = L_2 = L_P$ so that the quality factor of the pre-biasing loops $L_1 C_{T,max}$ and $L_2 C_{T,min}$ are also α^I and α^{II} during States I++ and II++, respectively, the per-cycle energy delivered to the load V_B using pSCE circuit can be stated as (see Eq. (3.40) of Appendix 3.15):

$$E_{pSCE,net} = \frac{1}{2} C_{T,min} \left[(\alpha^{II}) \left(V_{oc,max} + (1 + \alpha^I) \beta V_B \right)^2 + \frac{(\alpha^I) \left(V_{oc,max} + (1 + \alpha^{II}) V_B \right)^2}{\beta} - 2 \left(1 + \alpha^{II} + (1 + \alpha^I) \beta \right) V_B^2 \right], \quad (3.29)$$

for the case where the TENG is pre-biased for half the LC_T resonator cycle, i.e., up to the maximum achievable voltage during both States I++ and II++.

3.7.2.2 Leakage current loss

Both the SCE and pSCE circuits operate with switches off most of the time (barring the short duration at States I and II), and the leakage of charge through the non-ideal MOSFET switches and the reverse biased diodes of the FWR results in lower voltage magnitudes at States I and II and hence, lower extracted energy. The leakage current changes dynamically as the TENG

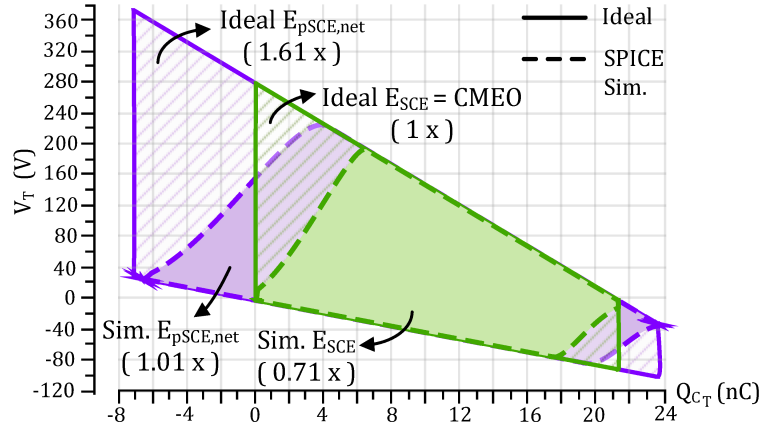


Figure 3.10 Ideal and simulated TENG voltage vs. charge plot for the SCE and pSCE circuits at 15 V load. Enclosed area represents the net energy extracted from one operation cycle of TENG.

voltage varies during the operation cycle and is also governed by the non-ideal characteristics of diodes and MOSFETs. To understand the effect of leakage on energy extraction, we take the aid of simulation using SPICE models of the diodes and MOSFETs used in the experimental implementation of this work (The list of these off-the-shelf components is provided in Appendix 3.16). Consider the simulated circuit operation (plotted in dotted lines) for the SCE and pSCE circuits at 15 V load in the form of TENG voltage vs. charge ($V_T - Q_{C_T}$) plot of Fig. 3.10: It can be observed that leakage alters the operation contour from the envisaged ideal operation contour (co-plotted using solid lines), reducing the enclosed area or equivalently the net extracted energy. In case the estimate of leakage charges (that depends on TENG voltage as well as switch and diode characteristics) during the switch off-times are available, the per-cycle energy results can be revised, e.g., in the SCE circuit, the voltage at State II, $V_T^{II} = V_{oc,max}$ will be revised to $V_{oc,max} - (C_{T,min} Q_L^I)$, where Q_L^I is the leakage charge in the first half-cycle.

For the TENG with parameters of Table 3.2, the ideal net per-cycle energy output of the pSCE circuit at 15 V load as per the area enclosed by $V_T - Q_{C_T}$ plot is 6.34 uJ or 1.61 times the CMEO, as marked in Fig. 3.10. In contrast, the simulation shows the net extracted energy to be 3.96 uJ. Finally, the net energy delivered to the load is further reduced to 2.51 uJ due to

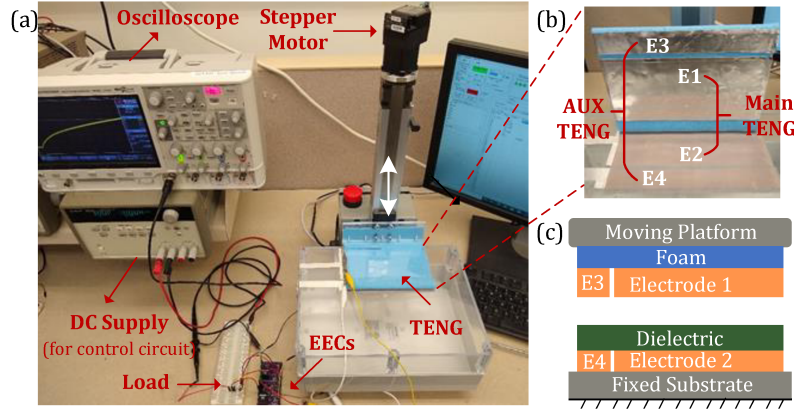


Figure 3.11 (a) Experimental Setup (b) Disassembled view of TENG (c) Schematic cross-section diagram of the implemented TENG.

conduction losses during energy extraction and pre-biasing steps. While there would be other losses such as parasitic losses due to non-ideal coupling in the transformer, these results already closely match the ones experimentally observed.

3.8 Experimental Implementation

3.8.1 Experimental Setup

The overall experimental setup is shown in Fig. 3.11(a). TENG with a contact area of 112.5 cm^2 is implemented as in the schematic of Fig. 3.11(c). The fixed bottom plate is made of Teflon (dielectric) of thickness $127 \text{ }\mu\text{m}$ on top of an Al sheet (electrode). The upper plate with the Al sheet (electrode) is driven in a reciprocating fashion by a stepper motor (Applied Motion STM 17Q-3AE) programmed using vendor-provided software (Q ProgrammerTM) at 10 Hz frequency, with an amplitude (x_{max}) of 1.64 mm. An electrically isolated auxiliary TENG (Aux-TENG) with 1/5th the main TENG area is created to operate synchronously in parallel (a blow-up of the same is shown in Fig. 3.11(b)), and is tapped using Electrodes 3 and 4 to provide the input signal to the control circuit, issuing switching pulses to the SCE/pSCE circuits in synchrony with the main TENG. Fig. 3.11(a) also shows the implemented EEC and load. Output is measured using the oscilloscope (Keysight DSOX2024A) and the data is collected through the NI's Data

Acquisition Card and Labview program. The DC supply powers the control circuit so that the energy consumed by the control circuits of SCE/pSCE can be measured non-interferingly.

Table 3.2 Measured TENG Parameters

Maximum open-circuit voltage: $V_{oc,max}$	279.92 V
Minimum TENG capacitance: $C_{T,min}$	75.97 pF
Maximum TENG capacitance: $C_{T,max}$	239.23 pF
TENG capacitance ratio: β	3.15

3.8.2 TENG Characterization

TENG is characterized by the three main parameters: minimum and maximum TENG capacitance ($C_{T,min}$ and $C_{T,max}$), and maximum open-circuit voltage ($V_{oc,max}$), that are summarized in Table 3.2 for our experimental TENG. Dynamic variation of TENG capacitance is measured using the phase response based method described in [28] and is plotted in Fig. 3.18 of Appendix 3.17 from which the maximum and minimum values of the TENG capacitor are obtained. On the other hand, the maximum open-circuit voltage is measured with the aid of the FWR circuit as in [24], with details provided in Appendix 3.18.

3.8.3 Implementation

Both the pSCE circuit and its switching controller are implemented as per Fig. 3.8 using off-the-shelf components over a PCB as shown in Fig. 3.12(a). Additionally, SCE and the standard Full Wave Rectifier (FWR) circuits are implemented over PCB (shown in Fig. 3.12(a) and (b), respectively) for performance comparison with the proposed pSCE circuit. As mentioned earlier, the SCE circuit is implemented similar to the pSCE circuit, barring the H-bridge and the control circuit's Arms 1 and 4 (refer Fig. 3.8) and same transformer with turns ratio 2:1 (refer Appendix Table 3.6) is used for both the circuits. The control circuit of both the SCE and pSCE circuits are powered at voltage V_{DD} of 3 V with their per-cycle control circuit consumption measured as 0.293 μJ and 0.423 μJ (at $V_B = 10V$), respectively. It should be noted that for our validation experiments, off-the-shelf components are used to implement the control circuit as a

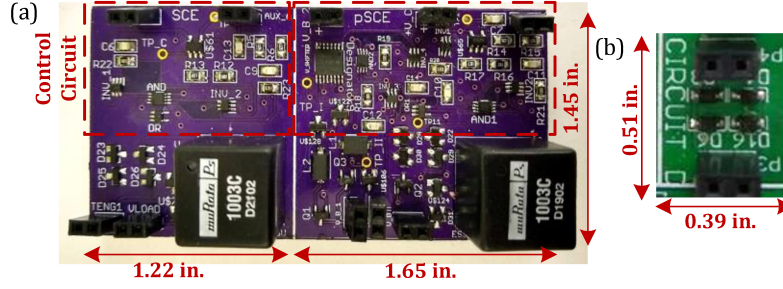


Figure 3.12 PCB implementations of the (a) SCE circuit, pSCE circuit, and (b) FWR circuit.

proof-of-study. Hence, there is a large room for further optimization to reduce this consumption, for example, by using a custom-designed IC. The extraction circuits have been designed to have the onboard load battery also supply the power needed for the switching actions of both SCE and pSCE operations. In case a cold-start is needed, the battery charging can first start in the passive FWR mode, requiring no switching energy (as for example in [19]), and once sufficient energy for SCE/pSCE action has been accumulated, the switch to SCE/pSCE operation can initiate. Note that the battery voltage needs to rise above the H-bridge path's threshold voltage of one diode and two switches, typically $\sim 2V$, for the pSCE action to start.

3.9 Results and Discussion

Given $V_{oc,max} = 279.92$ V and $\beta = 3.15$ (see Table 3.2), optimum pre-biasing voltage in second half-cycle ($V_{pb,opt}^{II}$) is calculated to be 130.19 V. Since we employ battery load of at most 16 V for testing, in our experiments it holds that $2V_B \leq V_{pb,opt}^{II}$, and so following **Remark 3**, we pre-bias to $-2V_B$ at State II++ (The pre-biasing at State I++ is always at the maximum possible level of $2V_B$). The measured TENG voltage (V_T), primary inductor (load) current (I_{L_S}), and the control voltage (V_G) waveforms for the pSCE circuit at 10 V battery load are shown in the center of Fig. 4.8. The two zoomed-in views at States I and II show the rising primary inductor current (I_{L_P}) as the switch S is enabled by V_G for energy extraction, which is followed by the rise of secondary inductor current (I_{L_S}) as triggered by the fall of signal V_G (NMOS S turns off). The

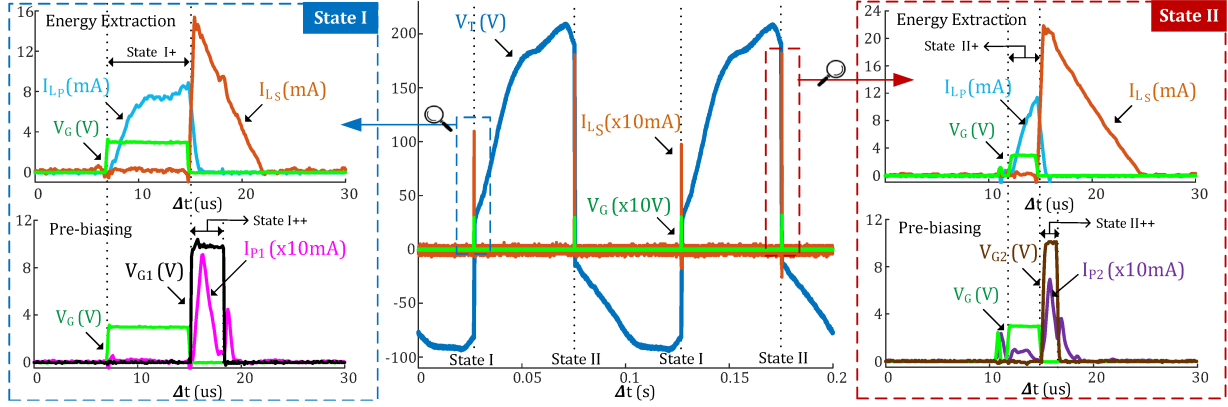


Figure 3.13 The measured TENG Voltage V_T , secondary inductor (load) current I_{LS} , and the control signal V_G for the switch S over two operation cycles of the pSCE circuit at 10V battery load. Additionally, the zoomed-in views at States I and II plot the primary inductor current I_{LP} during the energy extraction step of State I+ (resp., State II+), the control signal V_{G1} for S1 and S3 (resp., V_{G2} for S2 and S4), pre-biasing current I_{P1} (resp., I_{P2}) during State I++ (resp., State II++).

zoomed-in views at States I and II also show the measured pre-biasing control signal, V_{G1} (resp., V_{G2}), triggered by the fall of V_G , and the pre-biasing current, I_{P1} that flows through the V_B - S_1 - L_1 - D_1 - C_T - S_3 (resp., I_{P2} through V_B - S_2 - L_2 - D_2 - C_T - S_4) path. Fig. 3.14 plots the measured periodic TENG voltage waveforms, $V_T(t)$ for the pSCE circuit with load voltage V_B as 5V, 10V, 15V along with the SCE circuit (as a base case). In line with the derivations above, the pSCE circuit, pre-biased with twice the battery load ($2V_B$), shows increasingly higher TENG voltage magnitudes at both States I and II with rising load battery voltage V_B and is always higher than its SCE counterpart as observed from Fig. 3.14. This contributes to pSCE's increased per-cycle energy output as quantified in the following.

3.9.1 Comparison with FWR and SCE circuits

The fundamental comparison of the first time presented pSCE circuit is with its peer SCE circuit, together with the base case FWR circuit. For our experimental TENG with the parameters listed in Table 3.2, the measured per-cycle energy output (E_{cycle}) using FWR, SCE,

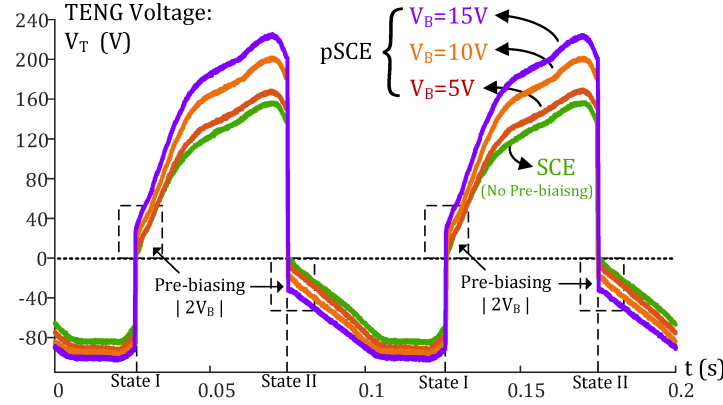


Figure 3.14 TENG Voltage V_T waveforms over two operation cycles for the SCE circuit and the pSCE circuit with load voltage V_B as 5V, 10V, and 15V.

and pSCE circuit as Energy Extraction Circuits (EECs) against battery loads are compared in Fig. 3.15. It is calculated as the product of load voltage (V_B) and integration of the measured current (charge) flowing through the load battery over one cycle. For the pSCE circuit, the net per-cycle energy ($E_{pSCE,net}$) is plotted, which is obtained by deducting the pre-biasing energy ($E_{pre-bias}$: calculated as the product of V_B and the integration of pre-biasing current, I_P over one cycle) from the gross output energy (E_{pSCE}). As evident from Fig. 3.15, E_{cycle} for FWR shows the expected parabolic response with variation in load voltage [10, 24]. SCE circuit has a constant energy output irrespective of V_B as expected from the circuit analysis in Sec. 3.4 and confirming **Remark 1**. For the pSCE circuit, an increasing net energy output trend is observed with the increasing value of V_B validating the theoretical development in Sec. 3.6. Table 3.3 lists the gain of the pSCE circuit over SCE and FWR circuit at three different load voltages. The pSCE circuit's gain increases with higher pre-biasing through the battery as the SCE output remains constant. Initially, the gain over FWR decreases with rising V_B due to the parabolic nature of FWR's E_{cycle} but is expected to rise later at higher V_B . Further, the power density figures of FWR, SCE, and pSCE circuits from our experimental implementation at 10 Hz operational frequency and 10V battery load are listed in Table 3.4. It should be noted that we implement the

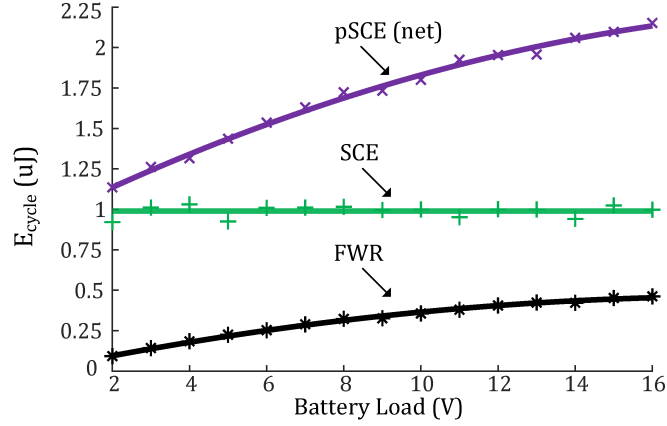


Figure 3.15 Comparison of measured per-cycle energy for the FWR, SCE, and pSCE circuits against the load voltage, V_B .

TENG only for circuit validation using readily available material such as Aluminum and Teflon tape. The power density values can significantly improve for the real-world implementations using the recent advances in TENG materials and designs.

Table 3.3 Measured energy and gain of the pSCE circuit over SCE and FWR circuit at different battery load

V_B (V)	E_{pSCE} (uJ)	$E_{pre-bias}$ (uJ)	$E_{pSCE,net}$ (uJ)	Gain over SCE	Gain over FWR
5	1.455	0.018	1.437	1.453	6.653
10	1.853	0.052	1.801	1.821	4.934
15	2.185	0.088	2.097	2.120	4.705

3.9.2 Comparison with EECs reported in literature

As mentioned in the Introduction, the Cycle for Maximized Energy Output (CMEO) defined in [11] sets the upper limit for energy extracted by any *passive* method (involving no pre-biasing) and serves as the reference for comparison, as has also been used in previous works such as [12] and [13]. Thus, for comparison, the per-cycle energy output (E_{cycle}) using different circuit

Table 3.4 Experimental Power Density of the FWR, SCE, and the pSCE circuits at 10V battery load

Circuit	PCB Area (cm ²)	Power Density (uW/cm ²)	PCB+TENG Area (cm ²)	Power Density (uW/cm ²)
FWR	1.290	2.829	113.790	0.032
SCE	11.413	0.867	146.413 ^a	0.068
pSCE	15.435	1.167	150.435 ^a	0.120

[a] includes Aux-TENG area

architectures is first normalized against CMEO as:

$$E_{norm} = \frac{E_{cycle}}{E_{CMEO}} \times 100\%; \quad E_{CMEO} = \frac{1}{2} \left(1 + \frac{1}{\beta} \right) C_{T,min} V_{oc,max}^2.$$

Table 5.1 first lists the maximum theoretical output normalized to CMEO (E_{norm}^*) that the considered circuit architecture can achieve at its optimal load with *ideal circuit* implementation.

As noted in **Remark 1**, SCE theoretically attains E_{CMEO} (implying its $E_{norm}^* = 100\%$) at all load voltages. In contrast, the proposed pSCE always outperforms SCE, and its energy output continues to grow with the load voltage leading to an unbounded E_{norm}^* (Refer **Remark 3**).

Table 5.1 next lists the reported experimental load voltage and the measured E_{norm} at that voltage. The energy outputs of FWR, S-SSHI, P-SSHI, and other such circuits listed in the table depend on load voltage, and an optimized load is needed to maximize the energy output, which requires an additional MPPT feature that consumes additional energy, and will reduce the net energy output. A key advantage of the proposed pSCE architecture is that it guarantees an energy output greater than CMEO at any load voltage as derived in Eq. (3.27).

3.10 Conclusion

This work proposed *active* pre-biasing of Triboelectric Nanogenerator (TENG) using the already present load battery for boosting the output energy beyond the Synchronous Charge Extraction (SCE) architecture, one that is proven to operate at CMEO (Cycle for Maximized Energy Output), but in a *passive* setting. It was shown that the increase in output due to pre-biasing in the first half-cycle of TENG operation (separation of the TENG plates) is

Table 3.5 Performance comparison with reported EECs for TENG

Ref	Circuit Architecture	Normalized maximum theoretical output (E_{norm}^*) and comment	Measurement Load	Normalized experimental output (E_{norm}) ^a
[24]	FWR	$\leq 25\%$ (max at $\beta = 1$)	26.75 V (Optimal)	20.43%
This Work	FWR	$\leq 25\%$	15 V	11.37%
[28]	Half wave rectifier with parallel diode	50%	~ 58 V	15.49%
[12]	Synchronous switched serial/parallel capacitor	25% (depends on load & number of intermediate capacitors)	~ 90 V	23% (mechanical switching)
[13]	Synchronous parallel switch	$\leq 50\%$ (max at $\beta = 1$)	~ 70 V (Optimal)	$\sim 42.86\%$ (mechanical switching)
[28]	Bennet voltage doubler	Unbounded; limited by air breakdown (needs $\beta > 2$)	~ 50 V	58.43%
[24]	P-SSHI	Limited by quality factor; high optimal load, so, impractical	15 V	19.53%
[24]	S-SSHI	Limited by quality factor; multiple transient cycles	26.15 V (Optimal)	172.8%
[14]	SCE	100% (capacitor load)	-	29.6%
[17]	SCE	100% (capacitor load)	-	37.8%
This Work	SCE	100% (battery load)	-	25.22%
This Work	pSCE	Unbounded; limited by air breakdown (161.72% at 15 V)	15 V	53.48%

[a] ignores control circuit energy consumption

attributed to the increase in the transduced energy from the mechanical source. In contrast, the gain in the second half-cycle (retraction of plates) is due to a reduction in the dissipated TENG electrical (potential) energy into the environment. We showed that this loss could be reduced to zero by using an optimum pre-biasing voltage that sets the plate charges to zero. It was further shown that increasing the pre-biasing voltage increases the overall output, and the upper limit to pre-biasing is essentially determined by air dielectric-breakdown voltage or the level of available mechanical excitation, namely, till the electrostatic attraction due to pre-biasing becomes comparable to the external excitation force.

For implementation of the proposed technique, a Pre-biased Synchronous Charge Extraction circuit (pSCE) circuit was presented to enable the pre-biasing of TENG at the start of each half-cycle using the load battery. The energy output of the pSCE circuit and conditions on pre-biasing voltages for net-benefit over the SCE circuit were mathematically derived. Experimental implementation of the pSCE circuit validates the expected gain in the energy output. Using the pSCE circuit with 5V battery load, experimental gains of 1.453 over the SCE circuit and 6.653 over the standard Full Wave Rectifier (FWR) circuit were achieved. A future research direction could explore the use of low-power active DC-DC converters to achieve optimum pre-biasing. We believe that the presented effort to increase the energy output by designing a novel pSCE circuit will bring us closer to the real-world feasibility of powering wireless sensor nodes by TENG.

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3.12 Appendix A: Calculation for electrostatic attraction for SCE and pSCE

Here, we perform first order calculations to determine the deceleration acting on the moving upper plate of TENG due to electrostatic force of attraction in the first half-cycle. For the SCE circuit, using Eq. (3.3), Eq. (3.11) and, Eq (3.12),

$$|\vec{F}_e^I| = \frac{(Q_1^{I+})^2}{2A\epsilon_0} \Rightarrow a_e^I = \frac{(Q_1^{I+})^2}{2mA\epsilon_0} = \frac{\sigma^2 A}{2m\epsilon_0}; \quad \sigma = \frac{V_{oc,max}\epsilon_0}{x_{max}}.$$

Here, m is the mass of the upper plate (113.7g). Using the operation and TENG parameters (Refer Sec. 3.8), electrostatic deceleration (a_e^I) is calculated as 0.013 m/s^2 . Similarly for the pSCE circuit (Refer Fig. 3.5(c)),

$$|\vec{F}_e^I| = \frac{(Q_1^{I++})^2}{2A\epsilon_0} \Rightarrow a_e^I = \frac{(Q_1^{I++})^2}{2mA\epsilon_0} = \frac{(\sigma A + 2C_{T,max}V_B)^2}{2mA\epsilon_0}.$$

The above electrostatic attraction is calculated as 0.026 m/s^2 at battery load (V_B) of $15V$. This is at least 2 orders of magnitude smaller compared to acceleration of natural sources (such as $2\text{-}3 \text{ m/s}^2$ for human walking, while 12 m/s^2 for car compartment [35]).

3.13 Appendix B: Lossless pre-biasing during State II++ for arbitrary voltage

As discussed in Sec. 3.6.1, at the start of the second half cycle (State II++), the TENG voltage can be set to any value $-V_{pb}^{II}$ such that $-2V_B \leq -V_{pb}^{II} \leq 0$ by adjusting the duration of pre-biasing. If the switches S_2 and S_4 are enabled for half the $L_2 - C_{T,min}$ resonator cycle, the maximum value of $V_{pb}^{II} = 2V_B$ is obtained. By reducing the “on” duration of these switches, a lower V_{pb}^{II} voltage can be obtained. However, in that case the instantaneous current in the loop (I_P) at the time of cut-off is non-zero and the energy stored on the inductor $\left(\frac{1}{2}L_2 (I_P)^2\right)$ is wasted. To recover this stored inductor energy, a diode (D_F) is added to the circuit as shown in Fig. 3.16(b) that gives path to freewheeling inductor current and in turn continue to charge the TENG capacitor. As shown in the waveform plots of Fig. 3.16(c), the switch on duration of S_2 is adjusted to obtain the required V_{pb}^{II} value. While, the switch S_4 is enabled for greater than or equal to half the $L_2 - C_{T,min}$ resonator cycle for completing the freewheeling current loop and is automatically cut-off as the inductor is completely discharged.

3.14 Appendix C: Derivation of per-cycle energy output of SCE with consideration for resistive loss

The energy output (E_{SCE}) derived in Sec. 3.4.2 through the V_T vs. Q_{C_T} plot represents the energy extracted from the source (TENG). Here, instead we derive the energy delivered to the load to include the resistance loss in the extraction circuit.

The SCE circuit with switch S on at State I is simplified to that shown in Fig. 3.17(a). Here, R_S is the sum of series parasitic resistance of the inductor and the on-state resistance of the

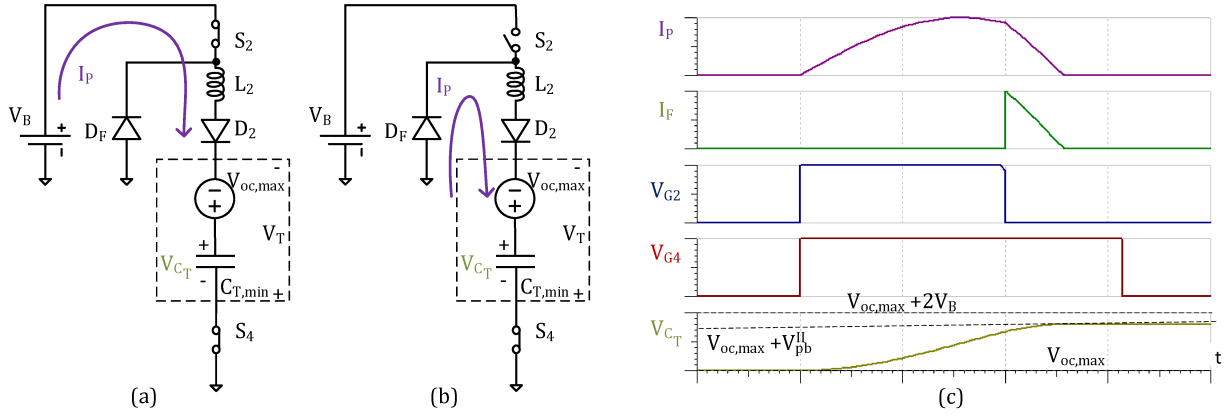


Figure 3.16 Simplified circuit during State II++ (a) with switches S_2 and S_4 closed. (b) with switch S_2 open and S_4 closed enabling the inductor current flow through the freewheeling diode (D_F). (c) Simulated waveforms for the pre-biasing loop current (I_P^{II+}), freewheeling current (I_F), enable signals for switches S_2 (V_{G2}) and S_4 (V_{G4}), and TENG capacitor voltage (V_{C_T}).

switch S. The differential equation for the current in the loop can be written as:

$$L_P \frac{d^2 I_{L_P}(t)}{dt^2} + R_S \frac{dI_{L_P}(t)}{dt} + \frac{1}{C_{T,max}} I_{L_P}(t) = 0.$$

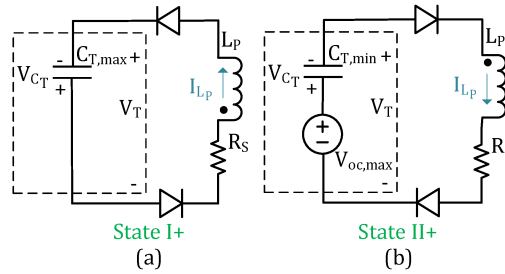


Figure 3.17 Simplified circuit during energy extraction with Switch S on during (a) State I+ and (b) State II+.

Note that the circuit loop with L_P can be independently analyzed as both primary and secondary inductors are decoupled. The above equation can be solved with initial condition as

$I_{LP}(0) = 0$ and $\frac{dI_{LP}}{dt}(0) = \frac{V_{CT}^I}{L_P} = \frac{V_{oc,max}}{\beta L_P}$ (Refer Eq. (3.7)) to obtain:

$$I_{LP}(t) = \left(\frac{e^{-\frac{R_S t}{2L_P}}}{L_P \omega_{d,SCE}^{I+}} \right) \left(\frac{V_{oc,max}}{\beta} \right) \sin(\omega_{d,SCE}^{I+} t); \quad \omega_{d,SCE}^{I+} := \sqrt{\frac{1}{L_P C_{T,max}} - \frac{R_S^2}{4L_P^2}}.$$

The switch is opened at one-fourth the $L_P - C_{T,max}$ cycle with the peak current as,

$$I_{LP} \left(\frac{\pi}{2\omega_{d,SCE}^{I+}} \right) = I_{LP,max}^{I+} = \left(\frac{\sqrt{\alpha^I}}{L_P \omega_{d,SCE}^{I+}} \right) \left(\frac{V_{oc,max}}{\beta} \right);$$

$$\alpha^I := e^{\frac{-\pi R_S}{2\omega_{d,SCE}^{I+} L_P}} = e^{\frac{-\pi}{2Q_f^I}}; \quad Q_f^I := \frac{\omega_{d,SCE}^{I+} L_P}{R_S}. \quad (3.30)$$

Here, Q_f^I is the series resonator quality factor at State I, and $0 < \alpha^I < 1$ is its “normalized” form that effectively captures the resistive circuit loss in the extraction step. Opening switch S leads to a sharp cut-off of I_{LP} in the primary loop. The negative voltage developed on the coupled inductors due to this current fall is conducive for current flow in the secondary side, and I_{LS} rises to a maximum of $I_{LP,max}^{I+}$ (taking coupling coefficient as 1 with $L_P = L_S$), which then is discharged through the diode D into the load battery. Using KVL in the secondary loop gives,

$$L_S \frac{dI_{LS}(t)}{dt} + V_B = 0 \Leftrightarrow I_{LS}(t) = -\frac{V_B}{L_S} t.$$

Here, by nature of the circuit, DC parasitic resistance of the secondary inductor L_S comes into play which is typically negligible and hence has been ignored in above equation. $I_{LS}(t)$ decays linearly from peak value of $I_{LP,max}^{I+}$ to zero during the charging duration, say T_L^I (Refer Fig. 3.3(c)), which can be computed by integrating the above equation:

$$\int_{I_{LP,max}^{I+}}^0 dI_{LS}(t) = \int_0^{T_L^I} \left(-\frac{V_B}{L_S} \right) dt \Rightarrow T_L^I = \frac{I_{LP,max}^{I+} L_S}{V_B}. \quad (3.31)$$

The energy delivered to the battery load is total charge flowing over the time T_L^I times the battery voltage which simplifies to,

$$E_{SCE}^{II} = V_B \int_0^{T_L^I} I_{LS}(t) dt = V_B \int_0^{T_L^I} \left(-\frac{V_B}{L_S} t \right) dt = \frac{1}{2} L_P \left(I_{LP,max}^{I+} \right)^2. \quad (3.32)$$

Substituting the value of $I_{LP,max}^{I+}$ from Eq. (4.33) gives,

$$E_{SCE}^{II} = \frac{1}{2} \left(\frac{\alpha^I}{\beta} \right) C_{T,min} V_{oc,max}^2. \quad (3.33)$$

Similar analysis at State II yields,

$$E_{SCE}^I = \frac{1}{2} \alpha^I C_{T,min} V_{oc,max}^2; \quad \alpha^{II} := e^{\frac{-\pi R_S}{2\omega_{d,SCE}^{II+} L_P}} = e^{\frac{-\pi}{2Q_f^{II}}}; \quad Q_f^{II} := \frac{\omega_{d,SCE}^{II+} L_P}{R_S}; \quad \omega_{d,SCE}^{II+} := \sqrt{\frac{1}{L_P C_{T,min}} - \frac{R_S^2}{4L_P^2}}, \quad (3.34)$$

where, Q_f^{II} , the series resonator quality factor at State II and its normalized form $0 < \alpha^{II} < 1$ are different than their State I counterparts (Eq. 4.33) due to change in TENG capacitance from $C_{T,max}$ to $C_{T,min}$. Then, the per-cycle energy delivered to the load shall be,

$$E_{SCE} = E_{SCE}^I + E_{SCE}^{II} = \frac{1}{2} \left(\frac{\alpha^I}{\beta} + \alpha^{II} \right) C_{T,min} V_{oc,max}^2. \quad (3.35)$$

3.15 Appendix D: Derivation of net per-cycle energy output of pSCE with consideration for resistive loss

The SCE circuit acts as the extraction circuit in the pSCE operation. Hence, from Eq. (3.21) and following the derivation of the SCE circuit's output in Appendix 3.14 above, the energy output of the pSCE circuit at the end of first half-cycle (E_{pSCE}^I) and that at the end of second half-cycle (E_{pSCE}^{II}) are given by,

$$E_{pSCE}^I = \frac{1}{2} (\alpha^I) C_{T,min} \left(V_{oc,max} + \beta V_{pb}^I \right)^2; \quad E_{pSCE}^{II} = \frac{1}{2} \left(\frac{\alpha^I}{\beta} \right) C_{T,min} \left(V_{oc,max} + V_{pb}^{II} \right)^2, \quad (3.36)$$

where, V_{pb}^I and V_{pb}^{II} are the pre-biasing voltages at States I and II, respectively. The normalized quality factors: $0 < \alpha^I, \alpha^{II} < 1$ at States I and II have been defined in Eq. (4.33) and Eq. (3.34), respectively.

Next, we analyze the H-bridge circuit considering resistive loss of the non-ideal inductors: L_1 and L_2 and the H-bridge switches ("Loss 3" in Fig. 3.9) to derive the pre-biasing voltages (V_{pb}^I and V_{pb}^{II}), and the energy used (invested) for the same ($E_{pre-bias}^I$ and $E_{pre-bias}^{II}$) at States I and II. For analytical convenience, we consider the case where TENG is pre-biased for half the LC_T resonator cycle i.e., up to the maximum achievable voltage at both States I and II. Further, the series resistance of the pre-biasing loop is taken to be same as that in the extraction loop, i.e., R_S .

First, we consider the pre-biasing circuit at State I++ with the switches S_1 and S_3 (Refer Fig. 3.7) closed. The differential equation for the pre-biasing loop is given by,

$$\frac{d^2 V_{C_T}(t)}{dt^2} + \frac{R_S}{L_1} \frac{dV_{C_T}(t)}{dt} + \frac{V_{C_T}(t)}{L_1 C_{T,max}} - \frac{V_B}{L_1 C_{T,max}} = 0.$$

Solving the above equation for $V_{C_T}(t)$ with the initial condition as $V_{C_T}(0) = V_{C_T}^{I+} = 0$ and taking $L_1 = L_P$,

$$V_{C_T}(t) = e^{-\frac{R_S t}{2L_P}} (V_B) \left[\cos(\omega_{d,SCET}^{I+} t) + \frac{R_S}{2L_P \omega_{d,SCET}^{I+}} \sin(\omega_{d,SCET}^{I+} t) \right] - V_B,$$

where, $\omega_{d,SCET}^{I+}$ is same as defined earlier in Eq. (4.33). With the switches S_1 and S_3 closed for half the $L_1 - C_{T,max}$ resonator cycle,

$$V_{C_T} \left(\frac{\pi}{\omega_{d,SCET}^{I+}} \right) = -(1 + \alpha^I) V_B.$$

Thus, a pre-biasing charge equal to $C_{T,max}(1 + \alpha^I)V_B$ is added by the load battery corresponding to energy of

$$E_{pre-bias}^I = \beta C_{T,min}(1 + \alpha^I)V_B \times V_B = (1 + \alpha^I)C_{T,min}\beta V_B^2, \quad (3.37)$$

and the pre-biasing voltage equal to $V_{pb}^I = V_T^{I++} = -V_{C_T}^{I++} = (1 + \alpha^I)V_B$. Now, using Eq. (3.36) and Eq. (3.37), the net energy delivered at the end of first half-cycle can be found as,

$$E_{pSCET,net}^I = E_{pSCET}^I - E_{pre-bias}^I = \frac{1}{2} C_{T,min} \left[(\alpha^{II}) \left(V_{oc,max} + (1 + \alpha^I)\beta V_B \right)^2 - 2(1 + \alpha^I)\beta V_B^2 \right]. \quad (3.38)$$

Performing similar analysis at the end of second half cycle gives $V_{pb}^{II} = (1 + \alpha^{II})V_B$ and the net per-cycle energy output as,

$$E_{pSCET,net}^{II} = E_{pSCET}^{II} - E_{pre-bias}^{II} = \frac{1}{2} C_{T,min} \left[\frac{(\alpha^I) \left(V_{oc,max} + (1 + \alpha^{II})V_B \right)^2}{\beta} - 2(1 + \alpha^{II})V_B^2 \right]. \quad (3.39)$$

Then the net per-cycle energy output of the pSCE circuit is given by,

$$\begin{aligned}
E_{pSCE,net} &= E_{pSCE,net}^I + E_{pSCE,net}^{II} \\
&= \frac{1}{2} C_{T,min} \left[(\alpha^{II}) \left(V_{oc,max} + (1 + \alpha^I) \beta V_B \right)^2 + \frac{(\alpha^I) \left(V_{oc,max} + (1 + \alpha^{II}) V_B \right)^2}{\beta} \right. \\
&\quad \left. - 2 \left(1 + \alpha^{II} + (1 + \alpha^I) \beta \right) V_B^2 \right].
\end{aligned} \tag{3.40}$$

3.16 Appendix E: List of off-the-shelf components

List of discrete components used in the pSCE implementation along with their manufacturers are presented in Table 3.6. SCE implementation uses a subset of these, i.e., without the H-bridge and the arms 1 and 4 of the control circuit in Fig. 3.8. FWR circuit is implemented on PCB using 1N4148WS diodes sourced from ON Semiconductors.

Table 3.6 List of off-the-shelf components

pSCE Circuit	Mfr. Part No.	Mfr.
Diodes	BAS21LT1G	ON Semiconductor
N-MOSFET (S_1, S_2)	DMN24H3D5L-7	Diodes Inc.
N-MOSFET (S, S_3, S_4)	DMN30H4D0L-7	Diodes Inc.
Inductors (L_1, L_2)	CC453232-101KL	Bourns Inc.
Pulse Transformer (L_p, L_s)	1003C	Murata Power Solutions
pSCE Control Circuit	Mfr. Part No.	Mfr.
Comparator	TS881LT	STMicroelectronics
Inverter	SN74LVC2G14DCK3	Texas Instruments
AND Gate	SN74AUP2G08DCUR	Texas Instruments
OR Gate	SN74AUP1G32DCKR	Texas Instruments
Voltage Level Shifter	CD4504BPWR	Texas Instruments

3.17 Appendix F: Measurement of dynamic TENG capacitance

TENG Capacitance ($C_T(t)$) is measured using the method based on phase response presented in [28, 36]. Below figure, shows measured C_T for our experimental TENG over 5 cycles of operation. Maximum and minimum TENG capacitance ($C_{T,max}$ and $C_{T,min}$) are deduced from

the below plot by first taking a moving average with span of 2% and then finding the maxima and minima. Values obtained are $239.23pF$ and $75.97pF$, respectively.

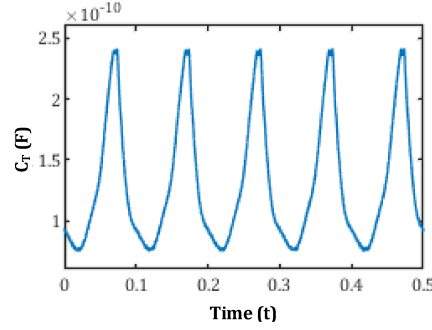


Figure 3.18 Measured time varying TENG capacitance ($C_T(t)$)

3.18 Appendix G: Measurement of TENG maximum open circuit voltage

The maximum open circuit voltage ($V_{oc,max}$) is measured by charging a capacitor unto saturation with Full Wave Rectifier (FWR) circuit and using the below relation[24],

$$V_{oc,max} = (\beta + 1)(V_{sat} + 2V_D).$$

The measured saturation voltage (V_{sat}) using electrometer (Keithley 6517) is $67.45V$. At saturation, negligible current flows through the FWR circuit and hence the diode drop (V_D) can be neglected, giving $V_{oc,max} \approx (\beta + 1)V_{sat} = 279.92V$ for the experimentally determined $\beta = 3.15$.

3.19 Appendix H: Measurement methods

To measure the TENG voltage, an op-amp based voltage follower circuit was employed. The time-varying voltage plot was obtained through an oscilloscope, which was then collected through the National Instruments Data Acquisition Card and Labview program.

For measuring the load current as well as implementing a battery load, an op-amp based scheme of Fig. 3.19 below was used. Due to this op-amp based scheme, the load voltage as seen by the circuit (namely, the voltage of the negative input terminal of the op-amp) remains

constant at V_B irrespective of the load current, as desired. The output voltage of op-amp (V_o) was recorded using an oscilloscope, which was then processed to obtain load current waveform as $I_o(t) = \frac{V_B - V_o(t)}{R_F}$. The per-cycle energy is then simply the integration of this charging current over an operation cycle times the load voltage V_B . The pre-biasing current I_{P1} and I_{P2} waveforms, shown in Fig. 4.8 were obtained using a current sense amplifier (Texas Instruments INA293).

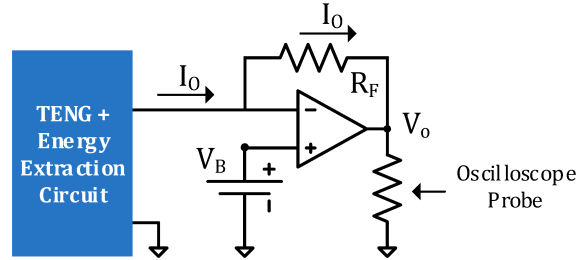


Figure 3.19 Circuit for load current measurement and implementing constant voltage load

CHAPTER 4. SELF-PROPELLED PRE-BIASED SYNCHRONOUS CHARGE EXTRACTION CIRCUIT FOR TRIBOELECTRIC NANOGENERATOR

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4.1 Abstract

Triboelectric Nanogenerators (TENGs) are suitable for harvesting ambient mechanical energy to increase the battery life of Internet of Things (IoT) devices. Energy Extraction Circuits (EECs) are required as an interface between TENG and the onboard battery load to rectify and improve the energy transfer efficiency. Here, for the first time, a novel ‘Self-propelled Pre-biased Synchronous Charge Extraction (spSCE)’ EEC is presented with theoretical analysis as well as experimental results. The proposed EEC offers a universal plug-and-play solution for *any* TENG operating under *any* ambient vibration, owing to its self-propelled switching feature. In addition, its inbuilt pre-biasing (pre-charging of TENG capacitor at the operation extremes) action enhances the net transduced energy from the mechanical source beyond the per-cycle energy limit for any non-pre-biasing EEC set by the existing Synchronous Charge Extraction (SCE) circuit. Accounting for the energy costs of spSCE actions, our experiments validated 119.7% (respectively, 163.7%) energy gain over the SCE circuit at a load of 5V (respectively, 15V).

4.2 Introduction: Motivation and objectives

Ambient micro energy harvesting is a promising green solution to prolonging the battery life of Internet of Things (IoT) devices. Energy harvesters that transduce from solar, thermal,

chemical, electromagnetic, and mechanical energy have been developed for the same[1]. Among those, mechanical energy harvesters have a universal appeal owing to the ready availability of motion energy in a wide variety of forms such as wind/water flow, machine/structure vibration, human body motion, etc.[1, 2]. Amidst the choice of various mechanical to electrical energy transducers, the Triboelectric Nanogenerator (TENG) has received significant recent interest for its versatility of material choices and fabrication methods [3, 4]. Further, since TENG can capture mechanical energy from different forms of reciprocating motions such as lateral (vibration), bending and, stretching through its multiple possible operating modes [3, 4, 5], they are suitable for harnessing energy from sources ranging from ocean waves to human body motion [3, 4, 6].

TENGs rely on the triboelectric phenomenon wherein any two different materials under repeated contact develop surface charge with opposite polarity. Relative contact-separation motion between these layers then induces emf (through electrostatic induction) across the attached pair of electrodes that can be connected to an external circuit to extract electrical energy [3]. A typical TENG implementation has a parallel-plate capacitor structure with a pair of electrodes and dielectrics of different materials over each electrode (or a dielectric layer on top of one of the electrodes) operating in contact-separation mode. For a self-powered IoT sensing application, the integrated TENG charges the on-board energy storage (battery/capacitor), which then powers the complete IoT system, for example, machine health monitoring in [7]. In such a system, an Energy Extraction Circuit (EEC) interfacing TENG source with load is additionally required to address the following: TENG has AC output and requires rectification for charging DC loads such as on-board battery or capacitor. Also, there is a need for source to load impedance matching to account for TENG's typically time-varying capacitive internal impedance, which leads to low energy transfer efficiency when load is directly connected to the TENG.

A Full Wave Rectifier (FWR) is the simplest EEC one can use. To improve the charging efficiency of the FWR circuit, strategies such as use of an optimized load battery voltage [8], optimized capacitor load [9], and transfer of energy to a switched intermediate capacitor and extraction from it at an optimized voltage [10, 11] have been devised. TENG's operational

parameters, namely, TENG capacitance at the operation extremes (minimum and maximum separation of the TENG plates) and its open-circuit voltage, however, vary as per the fluctuations in the ambient mechanical source (for example, bridge vibrations change as the traffic changes). Hence to operate at the optimal point, EECs require either manual tuning or a complex closed-loop control circuit with several active components, requiring external power, reducing TENG's net energy output.

In addition to FWR and the aforementioned optimizations around it, several switched EECs with mechanical or electronic switching, synchronous to the TENG operation extremes, have also been proposed [12]. In particular, [5] proposed a Cycle for Maximized Energy Output (CMEO) using a parallel synchronous switch that can attain the highest possible energy output under a simple-minded closing of the switch to allow the flow of charges from one plate to the other via the load at each extremity of plate separation. Under ideal conditions, the CMEO energy output limit is realizable at any load using Synchronous Charge Extraction (SCE) circuit, which was introduced earlier in the context of piezoelectric transducers [13, 14, 15], and later shown in the triboelectric context in [16, 17, 18, 19]. To attain an optimized SCE operation, its serial switch's "on" period must be synchronized and tuned to the TENG characteristics and operation, and an auto-tuned design that is universally applicable to any TENG and any source vibration does not exist: The existing implementations in the literature use pre-set/ hard-coded switching periods that are not universally tuned [16, 17, 18, 19].

Accordingly, in this work, we study both in theory and experiment, a novel EEC termed 'Self-propelled Pre-biased Synchronous Charge Extraction (spSCE)' for TENG with the following salient features:

- Self-propelled switching with automatic tuning of the switch-on period, making it a universal plug-and-play EEC, i.e., applicable for any TENG and any operating condition of ambient vibration.

- Inbuilt pre-biasing (pre-charging of TENG capacitor at each operation extreme) to yield per-cycle energy output beyond the CME0 limit realized using SCE by increasing the net energy transduced from the mechanical source.
- An innovative low-power control circuit for synchronous switching (with only one active component) that employs the proposed depletion type MOSFET (as opposed to a typical enhancement type MOSFET) switch. This scheme is measured to consume 161.2% lesser per-cycle energy than its SCE counterpart.
- Experimental validation showing 119.7% per-cycle net energy gain measured over the SCE circuit at battery load of 5 V, which rises to 163.7% at battery load of 15 V.

The use of pre-biasing the TENG to potentially increase the energy output beyond the CME0 limit can alternatively be achieved via LC circuit oscillation as in the case of a parallel or series synchronous switched harvesting on inductor (P-SSHI or S-SSHI) EECs, as presented in our earlier works [20, 21] and in [22, 23]. However, the P-SSHI or S-SSHI circuit's energy output exceeds the CME0 limit only for a specific load voltage range [21]. In contrast, the presented EEC delivers higher energy than CME0 at all possible load voltages. Another approach for pre-biasing is by way of “charge pump”, i.e., by feeding back a fraction of the TENG output charge stored on a bank of intermediate (flying) capacitors, switched between series and parallel modes [24, 25, 26]. This method, however, crosses the CME0 output typically at very high load voltage (few tens to hundreds of volts). Hence, this method is also not universally optimized across all loads, and suited more for a capacitor load (that has rising voltage) as opposed to a fixed voltage battery load of few volts, or requires an additional switched circuit stage between the charge pump and the end load [26]. Our previous work also proposed a pre-biasing scheme for TENG using the load battery itself that always delivers higher energy output than the CME0 [19], but requires a manually tuned and comparatively complex control circuit (with thirteen active components). In contrast, the presented EEC requires only one active component and is self-tuned for any TENG and any ambient vibration. Additionally, the pre-biasing level in the

proposed spSCE can be any multiple of the load battery, whereas, in pSCE of [19], it was limited to be twice the load battery. The proposed spSCE circuit architecture has been studied previously for piezoelectric energy harvesters [27], here, for the first time, it is introduced for TENG, where its analysis methodology, results, gains, etc. are entirely different as compared to piezoelectric harvesting. This difference fundamentally stems from the different circuit models of the two transducers: piezo has a variable current source in parallel to a *fixed* capacitor while tribo has a variable voltage source in series to a *time-varying* capacitor. To tackle the varying nature of TENG capacitor in the analysis, we introduce a smart discretization approach, and in experiments, introduce a switch control circuit different from that used in piezo setting.

In this paper, we first summarize the TENG circuit model. Also, the SCE circuit's operation, its per-cycle energy output, and challenges associated with different possible approaches for its control circuit are briefly discussed to serve as a reference for comparison with the proposed spSCE circuit. Next, the proposed spSCE circuit operation is mathematically analyzed, and its per-cycle energy output is derived. The energy gain of spSCE over the SCE circuit is mathematically shown to be always positive and increasing with the value of load battery voltage. Finally, for experimental validation, both the spSCE and the SCE circuits are implemented employing a standard contact-separation mode TENG. Their measured per-cycle energy output and control circuit energy consumption are compared to quantify the energy gain. At the end, the conclusions are presented.

4.3 Background and Preliminaries

4.3.1 TENG Circuit Model

Fig. 4.1(a) shows the cross-section view of a contact separation TENG, consisting of a dielectric (Teflon) tape atop an Aluminum electrode to form the bottom fixed plate together with an upper moving Aluminum electrode plate. External periodic mechanical excitation drives the upper plate in a vertical reciprocating motion relative to the stationary bottom plate. The repeated contact of the two plates generates equal and opposite triboelectric surface charge, $\pm\sigma A$.

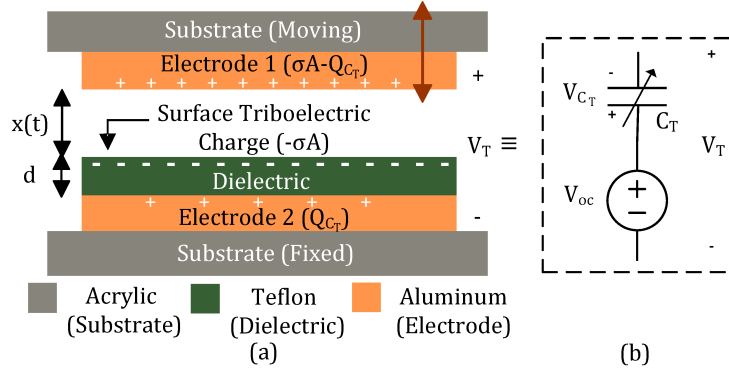


Figure 4.1 (a) Cross section view of a contact-separation TENG and (b) Equivalent circuit model of TENG.

This static surface charge induces open circuit voltage, V_{oc} , between the two electrodes that is linearly proportional to their separation:

$$V_{oc}(t) = \frac{\sigma x(t)}{\epsilon_0}. \quad (4.1)$$

Here, ϵ_0 is the electrical permittivity of air, and $x(t)$ is the distance between the two plates (air gap) that varies periodically between zero and a certain maximum value termed x_{max} . Further, the TENG forms a variable parallel plate capacitor with an air gap $x(t)$ along with a dielectric of thickness d between the two electrodes. Letting A denote the contact surface area of the plates, and ϵ_d the relative permittivity of the dielectric layer, the capacitance $C_T(t)$ is given by:

$$C_T(t) = \frac{\epsilon_0 A}{x(t) + \frac{d}{\epsilon_d}}. \quad (4.2)$$

When connected with an external circuit, the electrodes draw equal and opposite conduction charges, $\pm Q_{C_T}(t)$ (adding to the fixed triboelectric $\pm \sigma A$ charge) to generate additional voltage $V_{C_T}(t)$ across those. Accordingly, the overall TENG voltage $V_T(t)$ is given by the superposition of the two voltages:

$$V_T(t) = V_{oc}(t) - V_{C_T}(t) = \frac{\sigma x(t)}{\epsilon_0} - \frac{Q_{C_T}(t)}{C_T(t)}. \quad (4.3)$$

The above TENG operating equation leads to the circuit model shown in Fig. 4.1(b)[3]. One cycle of TENG operation commences with the two plates in contact, i.e., $x = 0$ (termed State I) and rises to reach maximum separation of $x = x_{max}$ (termed State II) to complete the first half-cycle,

followed by return to the initial position $x = 0$ in the second half-cycle. TENG electrical parameters V_{oc} and C_T at these two states are listed in Table 4.1. For ease in subsequent analysis, we denote the ratio of maximum to minimum capacitance to be: $\beta = \frac{C_{T,max}}{C_{T,min}}$.

Table 4.1 TENG parameters at the operation extremes

Operation State	Airgap (x)	Capacitance (C_T)	Open circuit voltage (V_{oc})
State I	$x_{min} = 0$	$C_{T,max} = \frac{\epsilon_0 A}{d_{eff}}$	$V_{oc,min} = 0$
State II	x_{max}	$C_{T,min} = \frac{\epsilon_0 A}{x_{max} + d_{eff}}$	$V_{oc,max} = \frac{\sigma x_{max}}{\epsilon_0}$

4.3.2 Synchronous Charge Extraction (SCE) Circuit

SCE circuit is obtained by serially connecting a full wave rectifier to a flyback converter as shown in Fig. 4.2(a). Serial switch S is normally open, and the TENG's built-up energy is efficiently transferred to the primary inductor L_P at States I and II by closing the switch S for quarter the period of L_P - C_T oscillator (Refer Fig. 4.2 (b) and (c)). Upon reopening the switch, the stored magnetic energy in the inductor core is subsequently transferred to the load. Here, based on previous works [16, 17, 18, 19], we summarize the SCE circuit operation, its per-cycle energy output, and different existing implementations of the control circuits for operating switch S , serving as motivation for our proposed spSCE circuit.

4.3.2.1 Circuit operation

The SCE circuit operation can be understood by following the TENG voltage $V_T(t)$ waveform (blue in color) of Fig. 4.7(a). Starting with State I, with the two plates in contact (i.e., $x = 0$ and both the TENG voltage V_T and charge on the TENG capacitor Q_{C_T} equal to zero), as the two plates separate with the Switch S open, V_T reaches its highest value of $V_{oc,max}$ at State II of maximum separation. Next, to extract energy, the switch S is closed, simplifying the SCE circuit to a L_P - $C_{T,min}$ oscillator (Fig. 4.2(c)). The current in the oscillator loop, I_{L_P} rises sinusoidally and reaches its peak value at the end of one-fourth the L_P - $C_{T,min}$ oscillator time-period, denoted

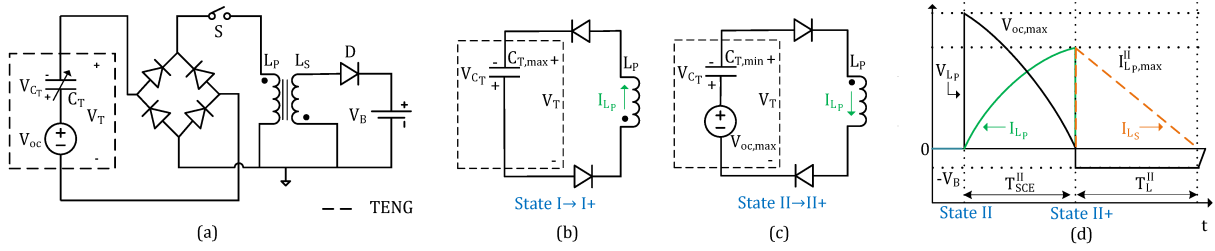


Figure 4.2 SCE Circuit: (a) Diagram, simplified circuit during energy extraction with Switch S turned on at (b) State I and (c) State II. (d) Primary inductor current: I_{LP} , voltage: V_{LP} , and secondary inductors current: I_{LS} during switching at State II for the SCE circuit.

T_{SCE}^{II} . At this point, denoted State II+, the energy transferred to L_P is at its peak value of $\frac{1}{2}L_P(I_{LP,max}^{II})^2$ and switch S is reopened, forcing a sharp cut-off of I_{LP} in the primary loop (Fig. 4.2(d)). The negative voltage developed on the coupled inductors due to this current fall is conducive for current flow in the secondary side, and the load battery is charged through the diode D . T_{SCE}^{II} equaling one-fourth the L_P - $C_{T,min}$ resonator cycle is given by:

$$T_{SCE}^{II} = \frac{\pi}{2\omega_{SCE}^{II}} = \frac{\pi\sqrt{L_PC_{T,min}}}{2}; \quad \omega_{SCE}^{II} = \frac{1}{\sqrt{L_PC_{T,min}}}, \quad (4.4)$$

where ω_{SCE}^{II} is the resonance frequency of the oscillator. At T_{SCE}^{II} , V_{CT} rises to $V_{oc,max}$ and overall TENG voltage, V_T falls to zero. With the start of the second half-cycle, the upper plate starts to descend, and V_T increases in value with negative polarity to reach its peak negative value at State I (Refer Fig. 4.7(a)). Next, switch S is closed for one-fourth the L_P - $C_{T,max}$ oscillator time-period T_{SCE}^I to extract energy, with the circuit simplified to as shown in Fig. 4.2(b). Similar to the switching action at State II (shown in Fig. 4.2(d)), the primary inductor current rises to its maximum value, while the voltage across it falls to zero in T_{SCE}^I , which is when the switch S is re-opened to trigger the load current flow in the secondary inductor. Note that,

$$T_{SCE}^I = \frac{\pi}{2\omega_{SCE}^I} = \frac{\pi\sqrt{L_PC_{T,max}}}{2} = \sqrt{\beta}T_{SCE}^{II}. \quad (4.5)$$

Thus, the required switch-on duration at State I is larger by a factor of $\sqrt{\beta}$ compared to that at State II due to a change in C_T from its minimum to maximum value. The switch-on periods (T_{SCE}^I and T_{SCE}^{II}) are designed to be small compared to the TENG operating time period.

4.3.2.2 Per-Cycle Energy Output

For a TENG operating with time period T , the energy extracted per-cycle, E_{cycle} can be obtained from integrating the power over a cycle [5]:

$$E = \int_0^T V_T I_T dt = \int_0^T V_T dQ_{C_T}. \quad (4.6)$$

Thus, the per-cycle energy equals the area enclosed by the V_T - Q_{C_T} cycle as plotted in Fig. 4.7(b) (the areas marked ① and ② enclosed by the blue curve). The area ① corresponds to the energy extracted at the end of the first half-cycle by closing switch S at State II (E_{SCE}^I), which equals the triangular area under the II-II+ sloping line and is given by:

$$E_{SCE}^I = \frac{1}{2} \times C_{T,min} V_{oc,max} \times V_{oc,max}. \quad (4.7)$$

Similarly, the area ② in Fig. 4.7(b) corresponds to the energy extracted at the end of the second half-cycle (E_{SCE}^{II}), which equals the triangular area above the I-I+ sloping line and is given by:

$$E_{SCE}^{II} = \frac{1}{2} \times C_{T,min} V_{oc,max} \times \frac{V_{oc,max}}{\beta}. \quad (4.8)$$

The combined energy output over a full cycle is the sum:

$$E_{SCE} = E_{SCE}^I + E_{SCE}^{II} = \frac{1}{2} \left(1 + \frac{1}{\beta} \right) C_{T,min} V_{oc,max}^2. \quad (4.9)$$

It can be seen that a useful feature of the SCE circuit is that its per-cycle energy output, E_{SCE} is independent of the load voltage due to its decoupling with the source (primary vs. secondary side currents, I_{LP} and I_{LS} are never simultaneously non-zero).

4.3.2.3 Switching Control Circuit Alternatives

For the SCE switching action, a dedicated control circuit is required to detect the two extrema of States I and II and issue the gate pulses to a MOSFET switch of desired durations T_{SCE}^I and

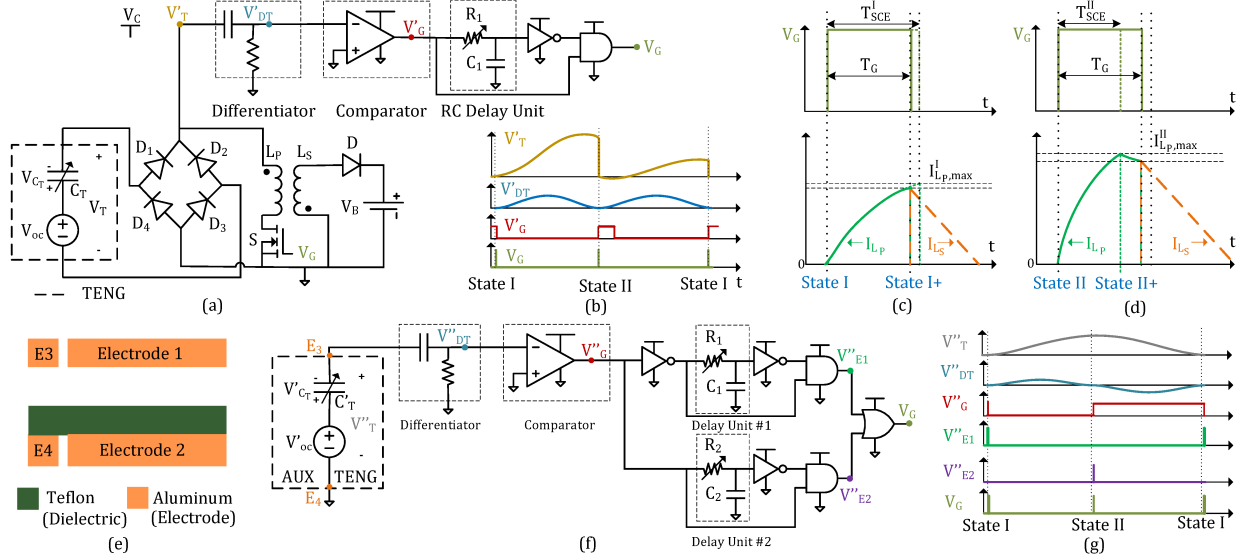


Figure 4.3 Existing SCE circuit with fixed timing: (a) Implementation taken from [16, 17, 18], (b) Its control circuit waveforms, and schematics showing effect of sub-optimal gate pulse width on primary inductor current, I_{LP} , during energy extraction at (c) State I and (d) State II. Existing SCE circuit with optimal timing implementation taken from [19]: (e) Cross section view of Auxiliary TENG (Aux-TENG) built in parallel with the main TENG, (f) Its control circuit implementation, and (g) Waveforms.

T_{SCE}^{II} , respectively. Next, we discuss the pros and cons of various existing means of implementing the switch control logic. There are three possible scenarios based on the exerted timing control.

Fixed Timing: Fig. 4.3(a) shows the simplest implementation that has a fixed “hard-wired” switch-on period, as in the case of [16, 17, 18]. Referring to the schematic waveforms of Fig. 4.3(b), the rectified TENG voltage (V_T') is fed to a CR differentiator converting voltage peaks at States I and II to zero crossings (V_{DT}'), which triggers state change of a comparator (V_G'), whose one input is tied to ground. The rising edges of the comparator signal (V_G') at States I and II trigger a pulse (V_G) for the gate of N-MOS with its pulse-width set by the time charging constant ($\tau = R_1 C_1$) of the RC delay unit.

From the above SCE analysis, it is known that the width of the gate pulse (switch on duration) required at States I and II are different and are related by Eq. (4.5). Thus, a limitation

of this implementation is that the switch on duration (T_G) is the same at both States I and II, set by a common tuning handle R_1 so that $T_{SCE}^{II} < T_G < T_{SCE}^I$. Thus, during energy extraction at State I, the switch is prematurely opened before the primary inductor current I_{LP} reaches its maxima of $I_{LP,max}^I$ (Refer Fig.. 4.3(c)) leading to sub-optimal energy extraction (lower than E_{SCE}^{II}) as the energy delivered to the load is proportional to the square of the peak inductor current. While at State II, the switch is on longer than T_{SCE}^{II} , beyond which the inductor voltage V_{LP} fails to turn negative (in polarity) due to the full wave rectifier, and I_{LP} can no longer maintain the sine curve (Refer Fig.. 4.2(d)). The current now circulates through the new path of $LP - S - D_3 - D_2$ and decays from its peak value due to parasitic resistance of LP and the switch-on resistance of S (present in practical scenario) in the loop till the switch is opened after T_G . This again results in sub-optimal energy extraction during State II-II+ (lower than E_{SCE}^I). Thus, T_G is tuned to a value obeying $T_{SCE}^{II} < T_G < T_{SCE}^I$ optimizing the total output of $E_{SCE} = E_{SCE}^I + E_{SCE}^{II}$. This effect of pulse width tuning on the total energy output of the SCE circuit has been experimentally studied previously in [18].

In practical applications, the plate separation values (x_{max} and x_{min}) change depending on the variations in the external mechanical input, and hence the required T_{SCE}^I and T_{SCE}^{II} values vary. Thus, this implementation suffers from sub-optimal energy extraction due to its inability to auto-tune the switching times to the TENG variability. Note when restricted to a “Free-standing” mode, TENG has fixed capacitance ($\beta = 1$)[5], it holds that $T_{SCE}^I = T_{SCE}^{II}$, and the “fixed timing” implementation will turn out to be optimal. However, even in this case, the switch-on period requires an initial manual tuning as per the given TENG’s capacitance.

Optimized Timing: Our previous work proposed a novel implementation for optimal energy extraction [19]. The basic idea is to create two separate tuning handles (RC delay units), which are dedicated to switching at States I and II. When the input signal to the control circuit is tapped from the rectified output, the State information is perturbed (States I and II are indistinguishable); hence, an electrically isolated auxiliary TENG (Aux-TENG) with a fraction of the main TENG’s area is in-built to operate in parallel with the main TENG (Refer Fig. 4.3(e))

and provide an unperturbed input signal to the control circuit (as in Fig. 4.3(f)). The control circuit operation is similar to the Fixed Timing case and can be understood by following the schematic waveforms of Fig. 4.3(g). The product R_1C_1 is tuned for pulse width of T_{SCE}^I as signal V_{E1}'' , whereas the T_{SCE}^{II} period for signal V_{E2}'' is realized by tuning the R_2C_2 product. These signals are disjuncted (via OR operation) to control the NMOS switch (V_G).

It is clear that while this implementation can achieve optimal energy extraction, it still does not adjust to operation variability since the timings are still “hard-wired”. The requirement of Aux-TENG is another undesired feature.

Optimized & Self-tuned Timing: For an optimized and self-tuned timing, in addition to the voltage peak detector (Differentiator + Comparator) to start the switch-on period, either a comparator to detect TENG’s zero voltage or a current sensor in series with the primary inductor to monitor its maxima and end the switch-on period is required. A simple-minded implementation is shown in Fig. 4.10 of Appendix 4.9. However, this adds power-hungry components such as a latch, current amplifier, comparator, etc. So, while optimality and self-tunability are realized, there are added complexity and energy cost.

Motivated by these, we propose using a circuit architecture that achieves optimal self-tuned operation with a simpler control circuit (only one active component).

4.4 Proposed spSCE circuit and its Analysis

Fig. 4.4(a) shows the proposed spSCE (self-propelled Synchronous Charge Extraction) circuit. It consists of a pair of switched inductors in parallel, L_{P1} and L_{P2} , sharing a coupled secondary inductor L_S with their turns ratio kept identical at, $N : 1$; $N = \sqrt{\frac{L_{P1}}{L_S}} = \sqrt{\frac{L_{P2}}{L_S}}$. L_{P1} (resp., L_{P2}) branch is serially connected to NMOS switch E_N (resp., PMOS switch E_P) and is used to extract energy at State II (resp., State I). The extracted energy is subsequently transferred to the load battery (with voltage V_B) via L_S as detailed in the next section. NMOS and PMOS gates are tied together and triggered by the control-circuit output V_G . The control-circuit is simply a voltage

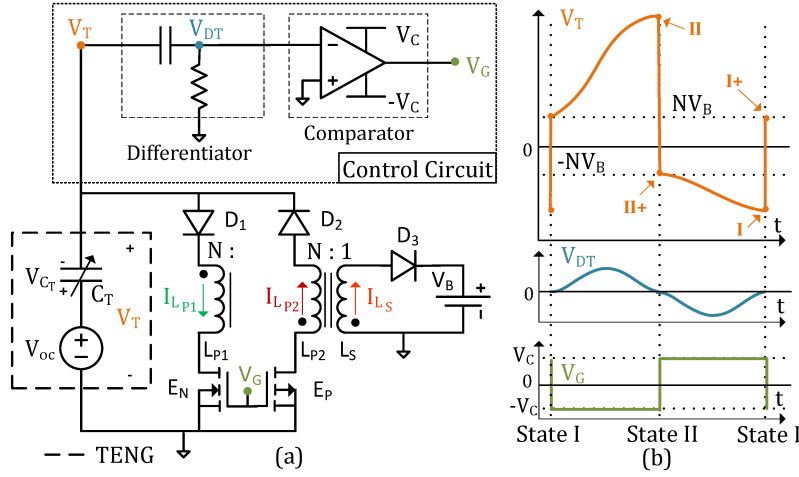


Figure 4.4 (a) Proposed spSCE circuit and its control circuit. (b) Schematic waveforms of TENG voltage, $V_T(t)$, and other control circuit waveforms.

extrema detector, consisting of a CR differentiator that converts the TENG voltage V_T peaks at States I and II into zero crossings (see V_{DT} plot Fig. 4.4(b)) that toggle the output of the comparator V_G between the control circuit supply voltages: $-V_C$ and V_C as shown in Fig. 4.4(b).

The self-tuned switching operation of the spSCE circuit can be understood by following the operation cycle diagram of Fig. 4.6(a) and the TENG voltage waveform $V_T(t)$ in Fig. 4.4(b) for one steady-state operation cycle. The switches E_N and E_P are normally off and TENG operates in open circuit condition starting from its initial state of two plates together to reach its maximum voltage at State II (top left in Fig. 4.6(a)). The control circuit detects the peak and changes its output to $+V_C$, enabling the N-MOS E_N and forming the L_{P1} - $C_{T,min}$ oscillator (similar to SCE), leading to rise in current through L_{P1} , while no current flows in the secondary loop due to reverse biased diode D_3 (top right in Fig. 4.6(a)). However, unlike the SCE circuit, the TENG voltage continues to fall beyond zero until reaching $-NV_B$, when the secondary loop diode D_3 gets forward biased (note as per the turns ratio of $N:1$, the voltage at the anode of diode D_3 reaches $+V_B$). This triggers current flow in the secondary inductor while the primary inductor current drops to zero, automatically turning off the switch E_N . At this point, the open circuit operation has resumed and continues until encountering the negative TENG voltage peak

at State I (refer Fig. 4.4(b) and corresponding circuit state shown in bottom right of Fig. 4.6(a)), and dual to State II above, the control circuit output toggles to $-V_C$, enabling the PMOS switch E_P to transfer built-up energy from $C_{T,max}$ to L_{P2} (through L_{P2} - $C_{T,max}$ oscillator as shown in bottom left of Fig. 4.6(a)). Again, dual to the State II case, E_P is automatically turned off when the TENG voltage reaches $+NV_B$ due to the forward biasing of D_3 . Thus, both at States I and II, energy is extracted from TENG via self-propelled switching.

Next, we analyze the circuit by way of a smart discretization approach (as opposed to a continuous pathwise analysis) to derive the values of the TENG voltage V_T and the capacitor charge Q_{C_T} at the two discrete TENG operation extremes, States I and II, to then use them to derive the per-cycle energy output E_{spSCE} . This avoids the need to deal with the time-varying nature of the capacitance as the plates move—only charge conservation during the moving phase and the capacitance values at the two extreme positions are required for the analysis.

4.4.1 Circuit operation and analysis

spSCE circuit operates with either of the switches, E_P or E_N enabled at States I ($x = 0$) and II ($x = x_{max}$), respectively. As with the SCE circuit, we use the notations States I and I+ (resp., States II and II+) to mark the pre vs. post switching voltages and currents at $x = 0$ (resp., $x = x_{max}$). Unlike the SCE circuit, spSCE shows one or more transient cycles prior to the steady-state operation as seen from the V_T waveform of Fig. 4.7(a) (under the ‘orange’ curve).

We start our circuit analysis from the first cycle of operation. Starting from the resting position, the operation commences with the two TENG plates in contact, i.e., $x = 0$ and TENG voltage, $V_T = 0$. Initially, as the two plates separate, both the switches, E_N and E_P , are off. TENG operates in open circuit condition and $V_T(t) = V_{oc}(t)$ increases. The control circuit senses the rising V_T and feeds the differentiated voltage (of positive polarity) to the comparator’s negative input (with positive input tied to ground) to produce the gate signal $V_G = -V_C$ (Refer Fig. 4.4(b)). The NMOS switch E_N continues to remain off since the gate voltage is negative ($V_G = -V_C$). The PMOS switch E_P also remains off since the diode D_2 serially connected to it is

reverse biased by V_T . The open circuit state continues until the two plates are maximally apart. Here, V_T reaches (local) peak voltage of $V_{oc,max}$ and starts to decline (Refer Fig. 4.7(a)), causing the sign of differentiated voltage to change, toggling the control circuit output from $-V_C$ to V_C , and turning on E_N , while E_P continues to remain off for D_2 remains reverse-biased by V_T . The spSCE circuit simplifies to a L_{P1} - $C_{T,min}$ oscillator as shown in Fig. 4.6(c). In this configuration, the differential equation governing TENG capacitor voltage V_{C_T} can be written as:

$$\frac{d^2 V_{C_T}(t)}{dt^2} + \frac{V_{C_T}(t)}{L_{P1} C_{T,min}} - \frac{V_{oc,max}}{L_{P1} C_{T,min}} = 0; t \geq 0. \quad (4.10)$$

With initial condition $V_{C_T}(0) = 0$ and L_{P1} taken equal to L_P (as in the SCE circuit for easy comparison), we obtain:

$$V_T(t) = V_{oc,max} - V_{C_T}(t) = V_{oc,max} \cos(\omega_{SCE}^{II} t). \quad (4.11)$$

The oscillator resonance frequency of ω_{SCE}^{II} has been defined earlier in Eq. (4.4). The inductor L_{P1} voltage $V_{L_{P1}}$ equals V_T , and also begins to reduce from its peak value of $V_{oc,max}$ following the cosine curve as plotted in Fig. 4.5(a). Note from Fig. 4.4(a) that the primary inductor L_{P1} is serially connected to the TENG via a single diode and hence, $V_{L_{P1}}$ can assume negative voltage value and continue following V_T past its zero crossing, unlike the SCE architecture (Fig. 4.2(a)), where the FWR restricts primary inductor to positive voltage drops only. The primary and secondary inductors have a turns ratio of N , and hence, for $t > T_{SCE}^{II}$, diode D_3 , connected serially with the secondary inductor L_S , is reverse biased until the secondary voltage, $V_{L_S}(t) = \frac{V_{L_{P1}}(t)}{N} > -V_B$. As shown in Fig. 4.5(a), the load charging commences when the inductor voltage $V_{L_{P1}} = V_T$ reaches $-NV_B$. The secondary voltage V_{L_S} remains at $-V_B$, and so the primary side voltage $V_{L_{P1}}$ remains at $-NV_B$ causing its rate of change to become zero, thereby forcing the primary side current $I_{L_{P1}}$ to be also zero. Owing to the turns ratio, the secondary current spikes up to N times that of the primary current just prior to the moment it was forced zero, charging the battery while decaying linearly (since from circuit of Fig. 4.4(a), $L_S \frac{d}{dt}(I_{L_S}) + V_B = 0 \Rightarrow \frac{d}{dt}(I_{L_S}) = -\frac{V_B}{L_S}$). When the primary current drops to zero, E_N is automatically switched off (in a self-propelled manner) and State II+ is reached, with the

following values for TENG voltage and capacitor charge:

$$V_T^{II+} = -NV_B \Rightarrow Q_{C_T}^{II+} = C_{T,min}(V_{oc,max} + NV_B). \quad (4.12)$$

Thus, aside from the self-propelled switch off, the added advantage of the proposed switching control circuit is that it automatically pre-biases the TENG to N times the load voltage ($V_T^{II+} = -NV_B$), unlike the case of SCE circuit where V_T is set to zero at State II+.

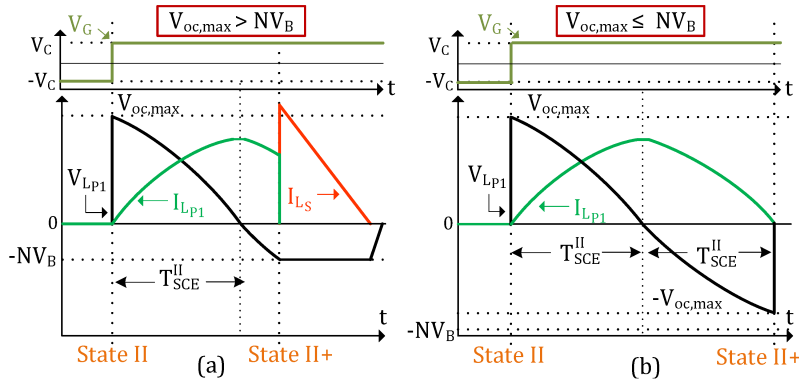


Figure 4.5 Primary inductor current: $I_{L_{P1}}$, voltage: $V_{L_{P1}}$, and secondary inductor current: I_{L_S} for spSCE circuit during switching at State II of the first operation cycle in case of (a) $V_{oc,max} > NV_B$ (b) $V_{oc,max} \leq NV_B$.

Remark 5 Note that if the turns ratio N and load voltage V_B do not satisfy $V_{oc,max} > NV_B$, after E_N is enabled at State II, the reverse-biasedness of D_3 shall continue even till the TENG voltage becomes the minimum possible ($V_T(t) = V_{L_{P1}}(t) = -V_{oc,max}$), i.e., till the end of half the L_{P1} - $C_{T,min}$ resonator cycle, and there shall be no load battery charging (Refer Fig. 4.5(b)).

Beyond this point in time, the current through the primary inductor that follows a sine curve tends to reverse its direction, but the diode D_1 blocks that, switching-off E_N and reaching State II+. In that case, the spSCE circuit shall undergo a multiple number of transient cycles depending on the value of NV_B relative to $V_{oc,max}$ where the TENG voltage buildup occurs without charging the battery and eventually entering the steady-state operation, where the battery charging takes place. This general scenario is analyzed in Appendix 4.10, where the number of transient cycles m

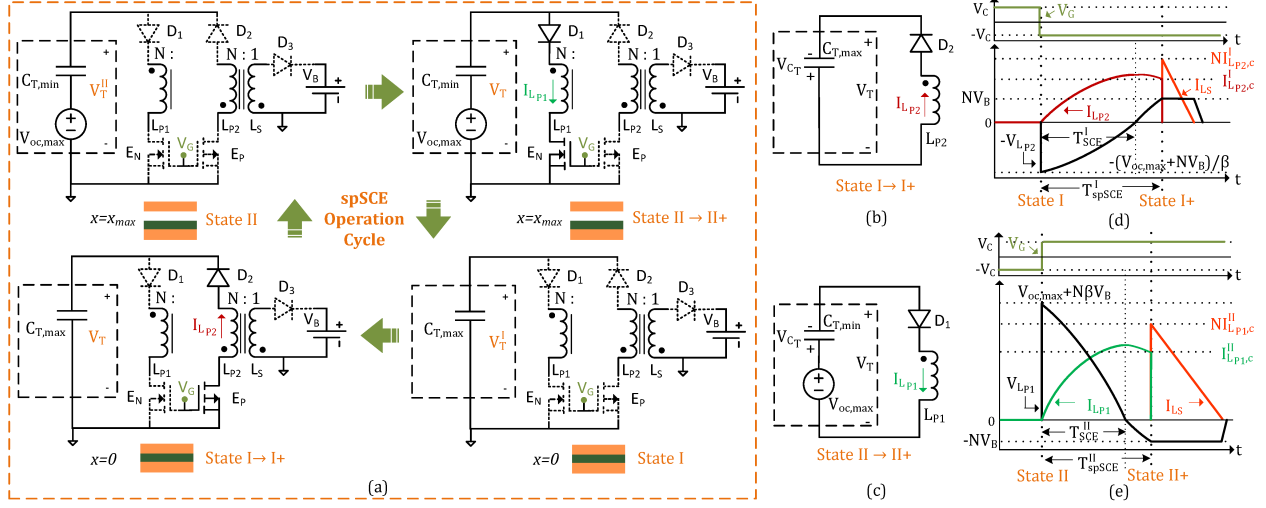


Figure 4.6 spSCE circuit:(a) Operation cycle, (b) Simplified circuit during energy extraction at (b) State I with E_P enabled and at (c) State II with E_N enabled. Primary inductor current: $I_{L_{P2}}/I_{L_{P1}}$, voltage: $V_{L_{P2}}/V_{L_{P1}}$, and secondary inductor current: I_{L_S} during switching at (d) State I/ (e) State II.

is derived (Eq. (4.24)), which can be expressed using the ceiling function as below:

$$m = \left\lceil \frac{1}{2} \left(1 + \frac{NV_B}{V_{oc,max}} \right) \right\rceil. \quad (4.13)$$

However, this situation ($m > 1$) is practically not very likely: Typical TENG's maximum open-circuit voltage to battery voltage ratio $\left(\frac{V_{oc,max}}{V_B}\right)$ is of the order of 50 or higher, while the turns ratio N is typically no larger than 10. Hence, the common practical implementations will likely satisfy the condition $V_{oc,max} > NV_B$ and here, we continue to analyze this case with one transient cycle as shown in Fig. 4.7(a) (under 'orange' curve). Interested readers may refer the TENG waveform of Fig. 4.12 in Appendix 4.11 for $V_{oc,max} \leq NV_B$ showcasing multiple transient cycles.

As the upper plate continues to descend in the second half-cycle beyond State II+, the TENG again operates in open circuit condition since E_N is off by reverse-biased diode D_1 and PMOS E_P is off by gate voltage V_G remaining pegged at $+V_C$. At the end of the second half-cycle (State I), the two plates are in contact, yielding $V_{oc} = V_{oc,min} = 0$ and $C_T = C_{T,max}$ (bottom right in

Fig. 4.6(a)). Additionally, since the charge is preserved, $Q_{C_T}^I = Q_{C_T}^{II+}$:

$$V_T^I \stackrel{(4.3)}{=} 0 - \frac{Q_{C_T}^I}{C_{T,max}} = -\frac{Q_{C_T}^{II+}}{C_{T,max}} \stackrel{(4.12)}{=} -\frac{(V_{oc,max} + NV_B)}{\beta}. \quad (4.14)$$

The control circuit senses this V_T minima and toggles V_G from V_C back to $-V_C$, enabling E_P this time (bottom left in Fig. 4.6), and the TENG circuit is reduced to a L_{P2} - $C_{T,max}$ oscillator (Fig. 4.6(b)). Dual to State II operation described above, as schematized in Fig. 4.6(d), V_T follows an inverted cosine curve and rises from its minima, flips its polarity at quarter the oscillator cycle, and continues to rise until the load charging commences at $V_T = -V_{L_{P2}} = NV_B$, when the E_P is automatically switched off and State I+ is achieved with:

$$NV_B = V_T^{I+} = -\frac{Q_{C_T}^{I+}}{C_{T,max}} \Rightarrow Q_{C_T}^{I+} = -N\beta C_{T,min} V_B. \quad (4.15)$$

We denote the E_P 's switch-on time as T_{spSCE}^I , that satisfies: $T_{SCE}^I < T_{spSCE}^I < 2T_{SCE}^I$, and is dependent on the voltage NV_B . Since $T_{spSCE}^I > T_{SCE}^I$, the energy extraction at State I is not optimal as the battery charging begins past the $I_{L_{P2}}$ peak (Refer red curve of Fig. 4.6(d)).

However, the pre-biasing action more than compensates for it, leading to a net increase in the energy extracted at the next extraction epoch, namely, at State II, as analytically proved in the following section.

Remark 6 During State I to I+, with E_P enabled, the inductor voltage $V_{L_{P2}}$ following cosine curve can rise to a maximum flipped value of $-V_T^I = \frac{(V_{oc,max} + NV_B)}{\beta}$ by the end of half the resonator cycle ($2 \times T_{SCE}^I$). In case of $V_B \geq \frac{V_{oc,max}}{N(\beta-1)}$, no load charging shall take place. For the sake of completeness, this case is also analyzed in Appendix 4.11.

Continuing the operation analysis (refer Fig. 4.7(a)), on reaching State II ($x = x_{max}$) with $Q_{C_T}^{II} = Q_{C_T}^{I+}$, we have:

$$V_T^{II} = V_{oc,max} - \frac{Q_{C_T}^{II}}{C_{T,min}} = V_{oc,max} + N\beta V_B. \quad (4.16)$$

Note the increment of $N\beta V_B$ in V_T^{II} due to pre-biasing action at State I compared to its SCE counterpart. As before, a change in the state of V_G on detection of peak voltage V_T^{II} enables conduction through E_N to form the L_{P1} - $C_{T,min}$ oscillator. Referring to Fig. 4.6(e), past the

quarter resonance cycle (T_{SCE}^{II}), when $V_{LP1} = V_T$ reaches $-NV_B$ value (after T_{spSCE}^{II}), secondary loop diode D_3 starts to conduct, freezing the secondary and primary side voltages (to V_B and $-NV_B$, respectively) and causing a (self-propelled) zeroing of the primary inductor current I_{LP1} from its value of $I_{LP1,c}^{II}$. This further leads to rise of secondary inductor current I_{LS} to $N \times I_{LP1,c}^{II}$. This marks State II+, and with E_N switched-off, V_T^{II+} is pre-biased to $-NV_B$ and Q_{CT}^{II+} is the same as derived in Eq. (4.12), completing the analysis of one steady-state operation cycle.

4.4.2 Per-Cycle Energy Output

As with the case of the SCE circuit, per-cycle energy output will be obtained using the V_T - Q_{CT} plot. The steady-state values of V_T and Q_{CT} derived for the spSCE circuit at States I, I+, II, and II+ above are used to obtain the plot of Fig. 4.7(b). The energy extracted at the end of the first half-cycle, E_{spSCE}^I is equal to the net area enclosed by the extraction step, namely, State II to II+ line, and the Q_{CT} axis, i.e., the net area ① + ③ + ⑤ - ⑥ in Fig. 4.7(b) and is given by,

$$E_{spSCE}^I = \frac{1}{2} \times C_{T,min}(V_{oc,max} + N\beta V_B) \times (V_{oc,max} + N\beta V_B) - \frac{1}{2} \times NC_{T,min}V_B \times NV_B. \quad (4.17)$$

Here, the area of the triangular region ⑥ is subtracted as V_T is negative for the corresponding part of II-II+ line turning the $V_T dQ_{CT}$ product negative (refer Eq. (4.6)). Similarly, energy extracted at the end of the second half-cycle, E_{spSCE}^{II} is the net area enclosed by the State I-I+ line, i.e., the net areas ② + ④ + ⑥ - ⑤ in Fig. 4.7(b) and can be calculated as,

$$E_{spSCE}^{II} = \frac{1}{2} \times C_{T,min}(V_{oc,max} + NV_B) \times \frac{(V_{oc,max} + NV_B)}{\beta} - \frac{1}{2} \times N\beta C_{T,min}V_B \times NV_B. \quad (4.18)$$

Adding the above two energy components of the two half-cycles, it follows that the per-cycle energy output E_{spSCE} is the total area enclosed by the spSCE curve (areas ①+②+③+④ in Fig. 4.7(b)):

$$E_{spSCE} = E_{spSCE}^I + E_{spSCE}^{II} = \frac{1}{2} C_{T,min} \left[(V_{oc,max} + N\beta V_B)^2 + \frac{(V_{oc,max} + NV_B)^2}{\beta} - (1 + \beta)(NV_B)^2 \right] \quad (4.19)$$

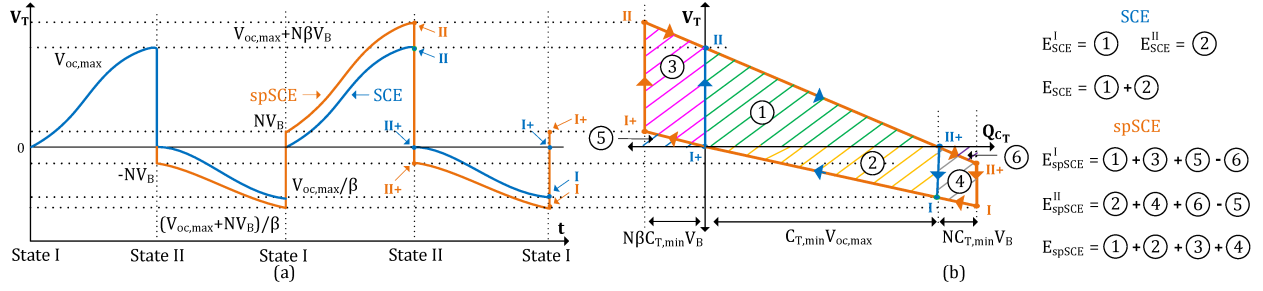


Figure 4.7 (a) TENG voltage waveform plot (blue under SCE vs. orange under spSCE), and (b) TENG “Charge vs. Voltage” plot for SCE (areas 1-2) and spSCE (areas 1-4) circuits.

Comparing with the SCE circuit output form (Eq. (4.9)), the above derived spSCE circuit’s output can be rewritten as:

$$E_{spSCE} = E_{SCE} + \frac{1}{2} C_{T,min} V_B \left[2 \left(\beta + \frac{1}{\beta} \right) V_{oc,max} + N^2 (\beta - 1) \left(\beta - \frac{1}{\beta} \right) V_B \right]. \quad (4.20)$$

Since $\beta \geq 1$, it is clear from the above equation that $E_{spSCE} > E_{SCE}$, and the additional harvested energy can be visualized from Fig. 4.7(b) as the additional area enclosed by the spSCE operation ($\textcircled{3} + \textcircled{4}$) beyond the SCE trapezoidal area ($\textcircled{1} + \textcircled{2}$). Also, since E_{SCE} is independent of the load voltage (see Eq. (4.9)), it follows from Eq. (4.20) that E_{spSCE} is an increasing function of the load voltage V_B . In other words, the energy output and gain of spSCE over SCE continues to rise with increasing V_B . Fundamentally, the gain over SCE is due to spSCE’s pre-biasing at the start of each half-cycle (by $\pm NV_B$) that increases the TENG’s electrical damping, enhancing the net transduced mechanical energy [19].

Remark 7 As derived above, the spSCE circuit’s output increases at higher battery load voltage, and as also stated in **Remark 5** and derived in Appendix 4.10, this may require a buildup of the TENG voltage to NV_B level through transient cycles. This can indeed be achieved in the ideal setting of no parasitic losses. However, in practice, there exists a limit to how far the TENG voltage can be raised before it saturates due to the parasitic resistive losses, which we briefly quantify here. In the case of $NV_B \geq V_{oc,max}$ with multiple transient cycles, referring to

Fig. 4.5(b), during State II to II+ operation, L - $C_{T,min}$ oscillator circuit ensures a perfect flip of voltage ($V_T^{II+} = -V_T^{II}$) in half the oscillation cycle. However, the series resistance of the primary inductor as well as the switch on resistance present in the oscillator loop (refer Fig. 4.14(b)) reduce the voltage swing to render $V_T^{II+} = -\alpha^{II}V_T^{II}$, where $0 < \alpha^{II} < 1$ is the “normalized” resonator quality factor with its value determined by the resistance, inductance, and the resonance frequency of the oscillator loop (refer Eq. (4.34)). Similarly, $0 < \alpha^I < 1$ determines the voltage swing of the oscillator loop during State I to I+: $V_T^{I+} = -\alpha^IV_T^I$. These imperfect swings lead to saturation of V_T over the transient buildup cycles, upper bounding its steady-state value (see Fig. 4.14(c) for visualization and the derivation of Eq. (4.38)), thereby limiting the allowable load voltage to a finite value:

$$V_B = \left[\frac{\alpha^{II}(1 + \alpha^I)}{(1 - \alpha^I\alpha^{II})} \right] \frac{V_{oc,max}}{N}. \quad (4.21)$$

4.4.3 Design with Single Polarity Power Supply

For ease of explanation, the spSCE circuit operation was discussed above with commonly used enhancement type PMOS (E_P) and NMOS (E_N) as switches. An enhancement type NMOS requires gate voltage higher than its positive threshold voltage, while an enhancement type PMOS requires gate voltage lower than its negative threshold voltage to switch on and, both are *normally off*, i.e., they remain switched off at zero gate voltage. Hence, the control circuit (comparator) of spSCE circuit requires a dual power supply with $-V_C$ (Low) and $+V_C$ (High) voltages (Refer Fig. 4.4(a) and (b)) to switch on PMOS and NMOS at States I and II, respectively. This dual power supply requirement can be relaxed by the innovation of introducing depletion type PMOS or NMOS in the spSCE circuit architecture. A depletion type PMOS (resp., NMOS) remains *normally on* and is switched off by pulling gate voltage (V_G) to V_C (resp., $-V_C$). With enhancement type PMOS (E_P in Fig. 4.4(a)) replaced by a depletion type PMOS and E_N retained as enhancement type NMOS, spSCE circuit operation can be achieved with gate voltage V_G toggling between 0 and V_C . Then, the control circuit shall require only a single voltage polarity power supply. Similarly, a combination of enhancement type PMOS and depletion type

NMOS allows operation with $-V_C$ and 0 states. All these three possible spSCE circuit implementations based on the required control circuit supply voltages are listed in Table 4.2.

Table 4.2 spSCE Circuit implementations and their control circuit supply requirements

Implementations	PMOS	NMOS	High	Low
Dual supply	Enhancement	Enhancement	V_C	$-V_C$
Single Positive supply	Depletion	Enhancement	V_C	0
Single Negative supply	Enhancement	Depletion	0	$-V_C$

4.5 Experimental Implementation

4.5.1 TENG Setup and Characterization

For experimental verification of the proposed circuits, the TENG was implemented as shown in Fig. 4.1 with Aluminum tape as the two electrode layers and Teflon tape of thickness $127 \mu m$ as the dielectric layer. The contact area between the upper moving plate (electrode 1) and the lower fixed plate (dielectric + electrode 2) is $112.5 cm^2$. For TENG operation, a programmed stepper motor moves the upper plate in reciprocating fashion at $10 Hz$ frequency with an amplitude of $x_{max} = 1.64 mm$. The overall setup picture is provided as Fig. 4.15 in Appendix 4.13.

The key parameters for TENG characterization: minimum and maximum TENG capacitances ($C_{T,min}$ and $C_{T,max}$), and the maximum open circuit voltage ($V_{oc,max}$), for our setup, were experimentally measured and are summarized in Table 4.3. For the TENG capacitance measurement, the phase response method described in [24] was used. The measured $C_T(t)$ is plotted in Fig. 4.17 of Appendix 4.14 from which the $C_{T,min}$ and $C_{T,max}$ values were extracted. The maximum open circuit voltage ($V_{oc,max}$) was measured with the aid of a full wave rectifier circuit as previously carried out in [19, 21] and described in Appendix 4.15.

4.5.2 Circuit Implementations

The proposed spSCE circuit along with the SCE circuit were implemented over PCB using off-the-shelf components for energy output measurement and comparison.

Table 4.3 Measured TENG Parameters

Maximum open circuit voltage: $V_{oc,max}$	282.88 V
Minimum TENG capacitance: $C_{T,min}$	76.35 pF
Maximum TENG capacitance: $C_{T,max}$	241.12 pF
TENG capacitance ratio: β	3.16

4.5.2.1 SCE Circuit

The SCE circuit with fixed as well as optimal switch-on period were implemented as shown in Fig. 4.3(a) and Fig. 4.3(f), respectively. For the fixed timing case, the capacitor C_1 was fixed at 1 pF, while the resistance R_1 was tuned to 750 k Ω , corresponding to a switching pulse width of $\sim 5.8 \mu s$, to offer maximized energy output of the fixed timing architecture. For the optimal timing implementation, an auxiliary TENG with a contact area of 22.5 cm² (1/5th area of main TENG) was fabricated to provide an input signal to the control circuit (refer Fig. 4.3(e) and Fig. 4.15). The switching pulse width for State I (T_{SCE}^I) was tuned to $\sim 6.8 \mu s$ using $R_1 = 820 \text{ k}\Omega$ ($C_1 = 1 \text{ pF}$), while that for State II (T_{SCE}^{II}) was tuned to $\sim 1.8 \mu s$ using $R_2 = 300 \text{ k}\Omega$ ($C_2 = 1 \text{ pF}$) (see Fig. 4.3(g)). The control circuit's supply voltage, V_C , and the measured per-cycle energy consumption, $E_{control}$ for both the implementations are provided in Table 4.4. The PCB implementation of the fixed-timing and the optimal-timing SCE circuits are shown in Fig. 4.16.

4.5.2.2 spSCE Circuit

The spSCE circuit of Fig. 4.4(a) is implemented with enhancement type PMOS and NMOS. A depletion type NMOS is used for single negative supply implementation. The PCB implementation of the spSCE circuits with coupled inductors' turns ratio $N = 1$ with Murata 1026C (1 : 1 : 1) and $N = 2$ with Pulse PH9400 (2 : 2 : 1) are shown in Fig. 4.16. The spSCE output and control circuit consumption are listed in Table 4.4.

Table 4.4 Net energy output for circuit implementations at $V_B = 10\text{ V}$

SCE Circuit Implementations	E_{SCE} (μJ)	Supply (V)		E_{control} (μJ)	$E_{\text{SCE,net}}$ (μJ)
		Low	High		
Fixed Timing	0.883	0	3	0.219	0.664
Optimal Timing	1.061	0	3	0.256	0.805
spSCE Circuit Implementations	E_{spSCE} (μJ)	Supply (V)		E_{control} (μJ)	$E_{\text{spSCE,net}}$ (μJ)
		Low	High		
Dual Supply (N=1)	1.471	-3	3	0.262	1.209
Single Supply (N=1)	1.379	-3	0	0.098	1.281
Single Supply (N=2)	1.839	-3	0	0.098	1.741

N: Turns ratio of the coupled inductors

4.6 Results and discussion

For our experimental spSCE and TENG with its parameters listed in Table 4.3, the measured TENG voltage V_T , load current I_{L_S} , and the control voltage V_G waveforms in steady-state at battery voltage $V_B = 10\text{ V}$ under the turns ratio $N=2$ and $N=1$ are shown in Fig. 4.8(a) and (b), respectively. As predicted from our derivation, due to the pre-biasing, the maximum TENG voltage in both the half-cycles, i.e., at States I and II, is higher (in magnitude) for $N = 2$ than for $N = 1$, which in turn is higher than its SCE counterpart (Fig. 4.8(c)). Fig. 4.8(d) and (e) show the zoomed-in view of load current, I_{L_S} , and control voltage, V_G at State II for the $N=2$ and $N=1$ implementations, respectively. The change of V_G from -3V to 0V enables the depletion type NMOS, and the rise of secondary loop current I_{L_S} after the switch-on period is observed, which subsequently linearly decays, charging the load battery. Similarly, for the SCE circuit, Fig. 4.8(f) shows the rise of the load current I_{L_S} triggered by the fall of the gate signal V_G at State II. Similar plots are observed for State I.

4.6.1 Performance Comparison

4.6.1.1 Energy Output

The measured per-cycle energy outputs using the fixed-timing and the optimal-timing SCE circuits at $V_B = 10\text{ V}$ battery load are listed in Table 4.4. It is calculated as the product of load

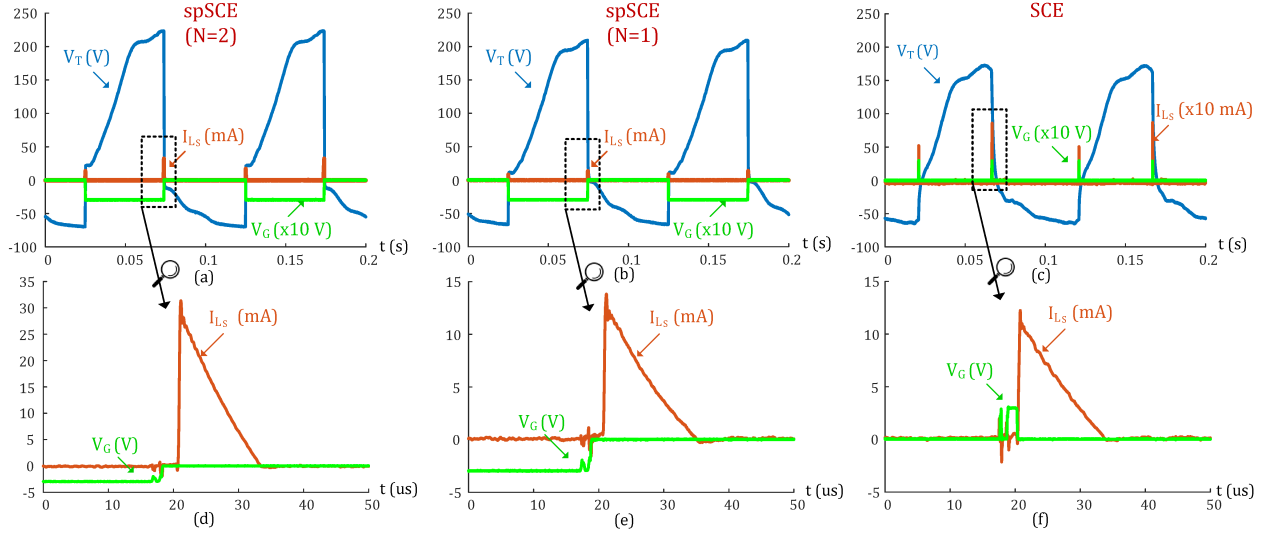


Figure 4.8 Measured TENG voltage: V_T , load current: I_{LS} , and control voltage: V_G waveforms at 10V battery load for (a) spSCE with turns ratio $N=1$, (b) spSCE with turns ratio $N=2$, and (c) SCE (Optimal Timing) circuits. Zoomed-in view of I_{LS} and V_G at State II for (d) spSCE ($N=1$), (e) spSCE ($N=2$), and (f) SCE (Optimal Timing) circuits.

voltage and integration of the measured current (i.e., the net accumulated charge) flowing through the load battery over one cycle. Per-cycle energy consumed by their respective control circuits, $E_{control}$ are nearly constant across the load voltage range and are deducted from E_{SCE} to obtain their net energy output, $E_{SCE,net}$. In our experiments, optimal-timing SCE implementation delivers 20.2% (178 nJ) higher energy compared to the fixed-timing implementation (refer Table 4.4). So from hereon, we use the optimal-timing SCE implementation with higher energy output for comparison with the spSCE circuit implementations.

For the case of $N=1$, among the two spSCE circuit implementations (dual vs. single supply) listed in Table 4.4, due to lower $E_{control}$, the net per-cycle energy output, $E_{spSCE,net}$ of the single supply implementation has a gain of 6% (72 nJ). This validates the proposed innovation of employing a depletion type MOSFET to enable single supply implementation, demonstrating that it not only eases the supply voltage polarity requirement, but also significantly reduces the energy

consumption. Hence, the preferred single supply implementation was further used in the spSCE circuit with $N=2$.

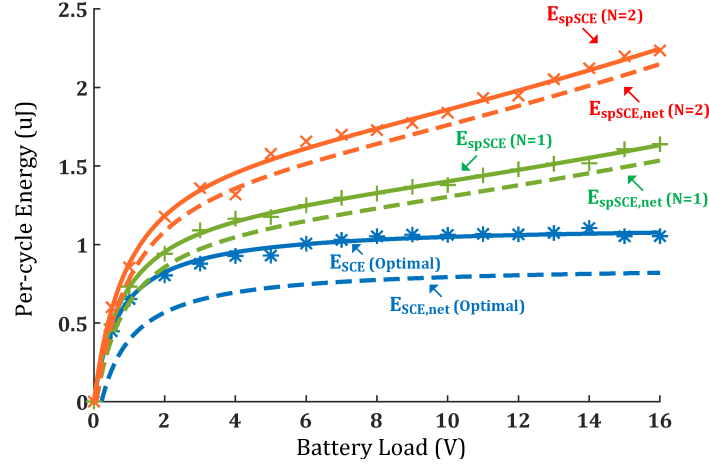


Figure 4.9 The comparison of measured per-cycle gross spSCE circuit energy output: E_{spSCE} with that of SCE: E_{SCE} against the load voltage: V_B . The $E_{spSCE,net}$ and $E_{SCE,net}$ are the net energy output post deduction of respective control circuit consumption.

Next, we compare the measured per-cycle energy output of the single supply spSCE circuit with $N=1, 2$, and the optimal-timing SCE circuit, over a load battery range of $0 - 16\text{ V}$ in Fig. 4.9. The net energy output of these implementations obtained by deducting their respective control circuit energy consumption are also co-plotted in Fig. 4.9 for visual confirmation of the minimal energy loss in the control circuit. The observed increasing trend of E_{spSCE} with increasing V_B validates the theoretical development of Sec. 4.4. Also, a higher pre-biasing due to $N=2$ consistently fetches a higher gain over $N=1$, and both these spSCE cases are consistently superior over the SCE. The energy gains of 34.2% ($0.402\text{ }\mu\text{J}$) at $V_B = 5\text{ V}$ and 36.8% ($0.592\text{ }\mu\text{J}$) at $V_B = 15\text{ V}$ over the spSCE circuit with $N=1$ were observed. The gains were even higher with respect to SCE: 69.7% ($0.648\text{ }\mu\text{J}$) at $V_B = 5\text{ V}$, and 108.9% ($1.146\text{ }\mu\text{J}$) at $V_B = 15\text{ V}$. Owing to the spSCE's innovative control circuit, which uses a single active component (namely. the

comparator), its $E_{control}$ is less than half of that for the SCE circuit (refer Table 4.4), rendering even higher net energy gains: 119.7% (0.806 μ J) at $V_B = 5V$ and 163.7% (1.304 μ J) at $V_B = 15V$.

4.6.1.2 Power Density

The net power density figures of the two SCE (fixed- vs. optimal-timing) and the two spSCE ($N=1$ vs. $N=2$) implementations computed from our validation experiments at 10 Hz operational frequency and 10 V load are listed in Table 4.5. The proposed spSCE circuit achieves more than a two-fold improvement in power density over the SCE circuit. Also, it should be noted that the reported values are for our initial PCB implementation; the power density can be significantly improved by reducing the circuit area through further optimization of design and selection of components.

Table 4.5 Experimental net power density of SCE and pSCE circuits at 10V battery load

Circuit	PCB Area (cm ²)	Power Density (uW/cm ²)	PCB+TENG Area (cm ²)	Power Density (uW/cm ²)
SCE (Fixed)	5.955	1.115	118.46	0.056
SCE (Optimal)	8.300	0.970	143.3 ^a	0.056
spSCE (N=1)	5.023	2.550	117.52	0.109
spSCE (N=2)	5.530	3.149	118.03	0.148

^a includes auxiliary TENG area

4.6.1.3 Efficiency

A measure of energy conversion efficiency is the performance against the “Cycle for Maximized Energy Output (CMEO)” [5], that sets the upper limit on the energy that can be harvested without any active feedback (pre-biasing) of the already harvested energy into the TENG transducer. This CMEO limit is given by $E_{CMEO} = \frac{1}{2} \left(1 + \frac{1}{\beta}\right) C_{T,min} V_{oc,max}^2$, and is attained by the optimized timing SCE architecture under ideal setting (refer Eq. (4.9)). Using the CMEO as a reference, the conversion efficiency of an EEC is defined as $\eta = \frac{E_{cycle}}{E_{CMEO}} \times 100\%$ as has been used in previous works, such as [8, 17]. While the ideal setting (no parasitic losses) SCE efficiency is 100%, its measured value is only 26.38%. In comparison, the spSCE with $N=2$ has a

measured efficiency of 54.66% for a 15V load, while it is even higher at 161.26% under ideal setting. The spSCE achieves such high improvements due to its in-built active pre-biasing feature, which is designed to increase with the increase in load voltage or by simply using a higher turns ratio N (as derived in Sec. 4.4.2). The proposed spSCE can further be compared with other EECs in the literature by referring to the efficiency survey table provided in our previous work [19].

4.6.2 Impact of Non-idealities

The non-idealities that affect the overall performance include diode voltage drops, leakage currents, diode/switch/ inductor resistances, etc. While the ideal SCE output is supposed to be constant across load voltages, it is not so in practice due to non-idealities as seen by the concave shape of the E_{SCE} curve at lower load voltages in Fig. 2.1, which is primarily caused by the parasitic non-zero diode drop, V_D (across the diode connected in series with the secondary inductor marked as diode ‘D’ in Fig. 2(a)). The derivation of E_{SCE} considering V_D (see Eq. (4.43) of Appendix 4.16) introduces a multiplication factor $\left(\frac{V_B}{V_B+V_D}\right)$ to the ideal SCE circuit’s energy output. With a typical V_D of $\sim 0.7V$, we observe the concave curve for E_{SCE} at low V_B and flat response for $V_B \gg V_D$ in Fig. 2.1. Similar behavior is observed for the spSCE circuit, too, due to the diode voltage drop across D_3 during the energy extraction.

Both SCE and spSCE circuits operate generally in open-circuit conditions other than the brief periods at States I and II. The leakage currents during the off periods through the non-ideal switches lead to lower TENG voltage amplitudes at States I and II, reducing the extracted energy. In case of the SCE circuit, for example, the TENG voltage at State II is expected to be equal to measured $V_{oc,max} = 282.88 V$, but the leakage reduces the measured peak to 179.61 V (refer Fig. 4.8(c)). Besides the mentioned diode drops and leakage currents non-idealities, on-resistance of the MOSFET switches, and the limited quality factors of the inductors owing to their parasitic resistances reduce the output compared to the theoretically expected value. Specifically, as derived in Eq. (4.21), the limited inductor quality factor places an upper bound on the maximum attainable TENG voltage/pre-biasing beyond which no added energy gain can be expected.

4.7 Conclusion

This work proposed a novel energy extraction circuit (EEC), a ‘self-propelled pre-biased synchronous charge extraction’ (spSCE) for Triboelectric Nanogenerator (TENG). The proposed circuit realizes efficient energy extraction via an external inductor, switched synchronously with the TENG operational extremes (TENG plates fully separated vs. fully contracted). The desirable self-propelled feature refers to the automated tuning of the switching start and end epochs as per any given TENG’s operating conditions, as against the existing Synchronous Charge Extraction (SCE) circuit implementations that require a manually tuned control circuit and hence are not adaptive to the vibrations they respond to. Further, it is analytically derived that the in-built pre-biasing feature of the spSCE circuit leads to an increase in the net per-cycle transduced mechanical energy, boosting the energy output beyond the SCE’s limit of CMEO (Cycle for Maximized Energy Output). The turns ratio N of the used coupled inductors serves to boost the effective battery voltage by a factor N raising the pre-biasing level by that same factor. It is formally derived that the spSCE circuit outperforms the SCE circuit at any load voltage, and its gain continues to rise with the rising effective load voltage.

The theoretically expected gain in energy output was validated by the experimental implementation of the spSCE, as well as the SCE circuit for comparison. The self-propelled switching control circuit of spSCE is found to consume 161.2% smaller per-cycle energy compared to the one currently used for SCE. The low energy consumption of spSCE’s control circuit is attributed to its simple single active component design and the innovative use of depletion type MOSFET (against typically used enhancement type MOSFET) for switching in the spSCE circuit. The proposed circuit’s higher energy output, yet lower control circuit energy consumption when compared to the SCE circuit, led to a measured net gain of 119.7% at $V_B = 5V$, that rose to 163.7% at $V_B = 15V$. We hope that the presented spSCE EEC with simpler implementation and boosted energy output shall pave the way towards its wide-scale adoption in motion energy harvesting applications.

4.8 References

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4.9 Appendix A: SCE circuit’s Optimal & Self-tuned Timing implementation

Fig. 4.10(a) shows a possible implementation to achieve both optimal and self-tuned/self-propelled operation. The control circuit is designed to trigger the gate pulse by detecting the TENG voltage (V_T') maxima at extremes (States I and II) and end the pulse on detecting primary inductor current (I_{LP}) maxima. The operation can be understood by following the schematic waveforms of Fig. 4.10(b). The top pulse generating arm of Fig. 4.10(a) is triggered at the rectified TENG voltage (V_T') maxima and acts as in the sub-optimal implementation described previously. The R_1C_1 product is set to output a narrow pulse (V_S') and set the SR latch output (V_G) to the high state of V_C . For monitoring I_{LP} , the voltage across a small valued resistor, R_S in series with L_P is measured using a current sense amplifier (V_I'), which acts as an input for the bottom pulse generating arm. The zoomed-in view of schematic waveforms during State II to II+ is shown in the right half of Fig. 4.10(b). At the peak of I_{LP} (corresponding V_I' peak), the zero crossing of the differentiated signal (V_{DI}') triggers a narrow pulse (V_R') set by R_2C_2 product to reset the SR latch output (V_G) to zero state and end the gate pulse. Similar

operation ensures that the required pulse width of T_{SCE}^I is obtained at State I. This dynamic control of gate pulse ensures both optimal and self-tuned operation.

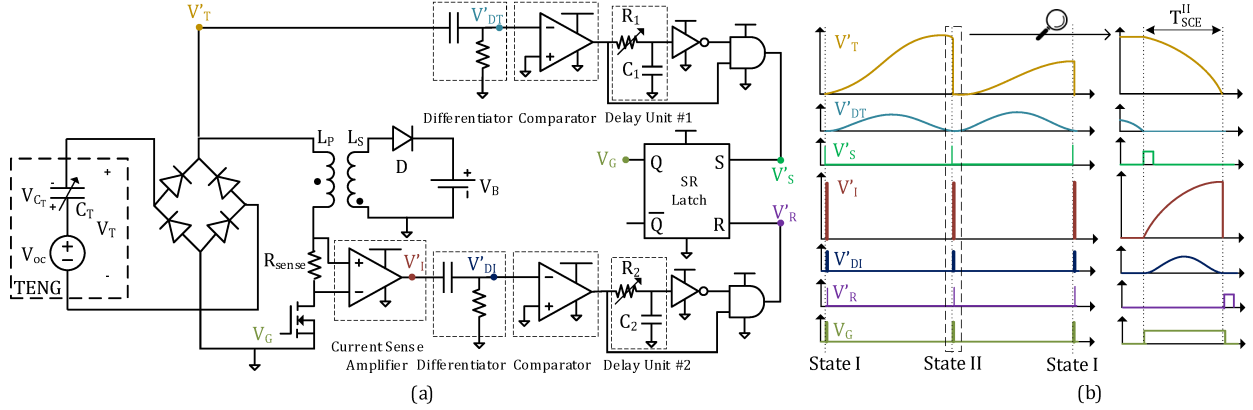


Figure 4.10 SCE circuit optimal and self-tuned (a) implementation and (b) Its control circuit waveforms.

4.10 Appendix B: Transient analysis for arbitrary effective load voltage: NV_B

Unlike the SCE circuit, starting from rest, the spSCE circuit shows a finite number of transient cycles depending on the effective value of load battery NV_B relative to $V_{oc,max}$ where the TENG voltage buildup occurs without charging the battery, and eventually entering the steady-state operation, where the battery charging takes place. To keep track of multiple transient cycles we use the notations, $V_{T,k}$ and $Q_{C_T,k}$ to denote the TENG voltage and capacitor charge in the k^{th} cycle, respectively. Starting from the rest, operation commences with the two TENG plates in contact, i.e., $x = 0$ and TENG voltage, $V_{T,1}^I = 0$. Initially, as the two plates separate, both the N-MOSFET E_N and P-MOSFET E_P are off. TENG operates in open circuit condition and $V_T(t) = V_{oc}(t)$ increases (Refer Fig. 4.12(a)). The open circuit state continues until the two plates are maximally apart ($x = x_{max}$), i.e., State II is reached when $V_{T,1}^{II}$ reaches (local) peak voltage of $V_{oc,max}$ and starts to decline (Refer Fig. 4.12(a)), causing the sign of differentiated voltage to change, toggling the control circuit output from $-V_C$ to V_C , and turning on E_N , while

E_P continues to remain off. The spSCE circuit simplifies to a L_{P1} - $C_{T,min}$ oscillator. In this configuration, the differential equation governing TENG capacitor voltage V_{C_T} can be written as:

$$\frac{d^2 V_{C_T}(t)}{dt^2} + \frac{V_{C_T}(t)}{L_{P1}C_{T,min}} - \frac{V_{oc,max}}{L_{P1}C_{T,min}} = 0; t \geq 0. \quad (4.22)$$

With initial condition $V_{C_T}(0) = V_{C_{T,1}}^{II} = 0$ and L_{P1} taken equal to L_P , we obtain:

$$V_T(t) = V_{oc,max} - V_{C_T}(t) = V_{oc,max} \cos(\omega_{SCE}^{II} t). \quad (4.23)$$

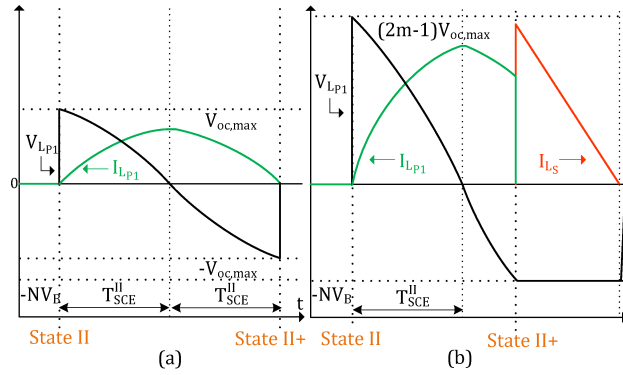


Figure 4.11 Primary Inductor Current $I_{L_{P1}}$, Voltage $V_{L_{P1}}$, and Secondary Inductor Current I_{L_S} for spSCE circuit during switching at State II of (a) first cycle and (b) m^{th} cycle.

The inductor L_{P1} voltage $V_{L_{P1}}$ equals V_T , and also begins to reduce from $V_{oc,max}$ peak following the cosine curve as plotted in Fig. 4.11(a). The primary and secondary inductors have a turns ratio of N , and hence, for $t > T_{SCE}^{II}$, diode D_3 , connected serially with the secondary inductor L_S , is reverse biased until the secondary voltage, $V_{L_S}^{II}(t) = \frac{V_{L_{P1}}^{II}(t)}{N} > -V_B$. For the generality of treatment where the transient period continues beyond one cycle to a finite number of cycles as determined later in our analysis, we let the reverse-biasedness of D_3 continue even till the TENG voltage becomes the minimum possible ($V_T = V_{L_{P1}} = -V_{oc,max}$), i.e., till the end of half the L_{P1} - $C_{T,min}$ resonator cycle. This results in load battery charging as clear from Refer Fig. 4.11(a). Beyond this point in time, the current through the primary inductor loop that follows a sine curve (recall that the inductor voltage follows a cosine curve, and so its current

follows a sine curve), tends to reverse its direction, but that is blocked by the diode D_1 , switching-off E_N and marking State II+. In the process, V_T has flipped in polarity from $V_{oc,max}$ to $-V_{oc,max}$ through the said E_N switch-on at State II of the first transient cycle. So using Eq. (4.3) with $V_{T,1}^{II+} = -V_{oc,max}$, we have:

$$V_{T,1}^{II+} = -V_{oc,max} \Rightarrow V_{C_T,1}^{II+} = 2V_{oc,max} \Rightarrow Q_{C_T,1}^{II+} = 2C_{T,min} V_{oc,max}.$$

As the upper plate continues to descend in the second half cycle beyond State II+, with the TENG again operating in the open circuit condition (since E_N is off), the charge on the TENG capacitor remains constant at $Q_{C_T,1}^{II+}$, while the value of $C_T(t)$ rises (since x decreases) and hence proportionately the value of $V_{C_T}(t)$ falls from the value of $2V_{oc,max}$ (conversely, $-V_{C_T}(t)$ increases from $-2V_{oc,max}$). However, the magnitude of $V_{oc}(t)$ also decreases with decrease in x and hence the cumulative effect on TENG voltage, $V_T(t) = V_{oc}(t) - V_{C_T}(t)$ decides if the $V_T(t)$ rises from $-V_{oc,max}$ to a more negative value as in the case plotted in Fig. 4.12(a) with $1 < \beta < 2$ or to a less negative value as in the representative case plotted in Fig. 4.12(d) with $\beta > 2$. On the other hand, the P-MOSFET switch E_P remains off due to V_G remaining pegged at V_C (since the threshold voltage of E_P is negative), whereas the N-MOSFET switch E_N also remains off due to the reverse biased diode D_1 , preserving the TENG capacitor charge. At the end of the second half-cycle (State I), the two plates are in contact, yielding $V_{oc} = V_{oc,min} = 0$ and $C_T = C_{T,max}$. Additionally from charge conservation, $Q_{C_T,2}^I = Q_{C_T,1}^{II+}$, and hence:

$$V_{T,2}^I = V_{oc,min} - \frac{Q_{C_T,2}^I}{C_{T,max}} = 0 - \frac{Q_{C_T,1}^{II+}}{C_{T,max}} = -\frac{2V_{oc,max}}{\beta}.$$

The control circuit senses this V_T minima and toggles V_G from V_C back to $-V_C$, enabling E_P this time, and the TENG circuit is reduced to a L_{P2} - $C_{T,max}$ oscillator. Dual to the operation at State II of the first cycle described above, V_T follows an inverted cosine curve and rises from its minima, flips its polarity at quarter the resonator cycle, and continues to rise until the end of half the resonator cycle ($2 \times T_{SCE}^I$) reaching maximum value of $\frac{2V_{oc,max}}{\beta}$. We again allow this for the generality of treatment so that the transient period does not end at one cycle. This continuation of the transient period occurs beyond the first cycle if the turns ratio is such that $\frac{2V_{oc,max}}{\beta \times N} < V_B$,

so that dual to the case of State II, Diode D_3 remains reverse biased and again no load battery charging occurs via the secondary inductor L_S . After $2 \times T_{SCE}^I$, diode D_2 blocks the reversing current $I_{L_{P2}}$, switching-off E_P and reaching State I+. Since V_T value is flipped so is Q_{CT} value: $V_{T,2}^{I+} = -V_{T,2}^I = \frac{2V_{oc,max}}{\beta}$ and $Q_{CT,2}^{I+} = -Q_{CT,2}^I = -2C_{T,min}V_{oc,max}$. Since both the switches remain off between State I+ and State II, it also holds that, $Q_{CT,2}^{II} = Q_{CT,2}^{I+}$. We are now returned to State II at the start of its 2nd transient cycle, and can infer from above:

$$V_{T,2}^{II} = V_{oc,max} - \frac{Q_{CT,2}^{II}}{C_{T,min}} = 3V_{oc,max}.$$

Following the above line of iterative reasoning, the TENG voltage at State II and State I for the k^{th} transient cycle can be expressed as:

$$V_{T,k}^{II} = (2k-1)V_{oc,max}; \quad V_{T,k}^I = -2(k-1)\frac{V_{oc,max}}{\beta}.$$

Note that for any $k \geq 1$, $V_{T,k}^{II} > |V_{T,k}^I|$ since $2k-1 > \frac{2(k-1)}{\beta} \Leftrightarrow \beta > \frac{2(k-1)}{2k-1}$, where the last inequality is true since $\beta \geq 1$ while $\frac{2(k-1)}{2k-1} < 1$. The above voltage buildup across the transient cycles continues, with no charging of the load battery (at either State I or State II), until say the m^{th} cycle when the following condition is met:

$$\left[\frac{V_{T,m}^{II}}{N} \geq V_B \right] \vee \left[\frac{|V_{T,m}^I|}{N} \geq V_B \right] \Leftrightarrow \left[\frac{V_{T,m}^{II}}{N} \geq V_B \right],$$

where the last equivalence follows from the fact that $V_{T,k}^{II} > |V_{T,k}^I|$ for any $k \geq 1$. Then the number of transient cycles m can be expressed using the ceiling function as below:

$$\frac{V_{T,m}^{II}}{N} = \frac{(2m-1)V_{oc,max}}{N} \geq V_B \Leftrightarrow m = \left\lceil \frac{1}{2} \left(1 + \frac{NV_B}{V_{oc,max}} \right) \right\rceil. \quad (4.24)$$

The inductor voltage $V_{L_{P1}}$ and current $I_{L_{P1}}$ during State II to II+ of the m^{th} cycle are plotted in Fig. 4.11(b). The inductor voltage $V_{L_{P1}} = V_T$ falls from $(2m-1)V_{oc,max}$ until reaching $-NV_B$, when diode D_3 is forward biased leading to a sharp rise in the secondary inductor current I_{L_S} and switches off the current through the primary loop. Subsequently, I_{L_S} gets discharged into the battery load V_B . Accordingly, at State II+:

$$V_{T,m}^{II+} = -NV_B \Rightarrow V_{CT,m}^{II+} = V_{oc,max} + NV_B \Rightarrow Q_{CT,m}^{II+} = C_{T,min}(V_{oc,max} + NV_B). \quad (4.25)$$

This completes the analysis of the transient period.

4.11 Appendix C: Steady-State Analysis for arbitrary effective load voltage:

$$NV_B$$

4.11.1 Steady-state operation

Past the initial m transient cycles, spSCE circuit enters steady-state operation with the same voltage and current profile in each cycle and supplying the same energy to the load battery per cycle. The TENG voltage at the start of the $(m + 1)^{th}$ cycle at State I is given as:

$$V_{T,ss}^I = V_{T,m+1}^I \stackrel{(4.3)}{=} V_{oc,min} - \frac{Q_{C_T,m+1}^I}{C_{T,max}} = 0 - \frac{Q_{C_T,m}^{I+}}{C_{T,max}} \stackrel{(4.25)}{=} -\frac{(V_{oc,max} + NV_B)}{\beta}. \quad (4.26)$$

As discussed above, at this point, the switch E_P is on and the circuit forms the L_{P2} - $C_{T,max}$ oscillator. The inductor voltage $V_{L_{P2}}$ follows a cosine curve, and can rise to a maximum flipped value of $-V_{T,ss}^I = \frac{(V_{oc,max} + NV_B)}{\beta}$ by the end of half the resonator cycle ($2 \times T_{SCE}^I$). During this process, it is possible that the secondary side voltage exceeds V_B (thereby forward biasing D_3 and allowing load battery charging) in case the following condition is met:

$$V_B < V_{L_S}^I = \frac{V_{L_{P2}}^I}{N} = \frac{-V_{T,ss}^I}{N} = \frac{(V_{oc,max} + NV_B)}{N\beta} \Leftrightarrow \frac{V_{oc,max}}{N(\beta - 1)} > V_B. \quad (4.27)$$

Steady State Case A $\left(\frac{V_{oc,max}}{N(\beta-1)} > V_B\right)$: The steady state values for TENG voltage and charge in this case have been derived in the manuscript as Eq. (4.12), (4.14), (4.15), and (4.16). The TENG voltage waveform with one transient cycle ($m = 1$) is plotted in Fig. 4.7(a), while that with multiple transient cycles ($m > 1$) is plotted in Fig. 4.12(a).

Steady State Case B $\left(\frac{V_{oc,max}}{N(\beta-1)} \leq V_B\right)$: As noted in Case A, the battery charging occurs at the end of both the half-cycles, but the same is not true in Case B, where as described below, the battery charging occurs only at the end of first half-cycle. The TENG voltage at the start of the steady-state cycle from State I ($V_{T,m+1}^I = V_{T,ss}^I$) is given by Eq. (4.26), and its waveform for Case B is plotted in Fig. 4.12(d). By definition of the two Cases, in contrast to the Case A, the condition of Eq. (4.27) is not met in Case B, and as shown in Fig. 4.12(e), the primary inductor

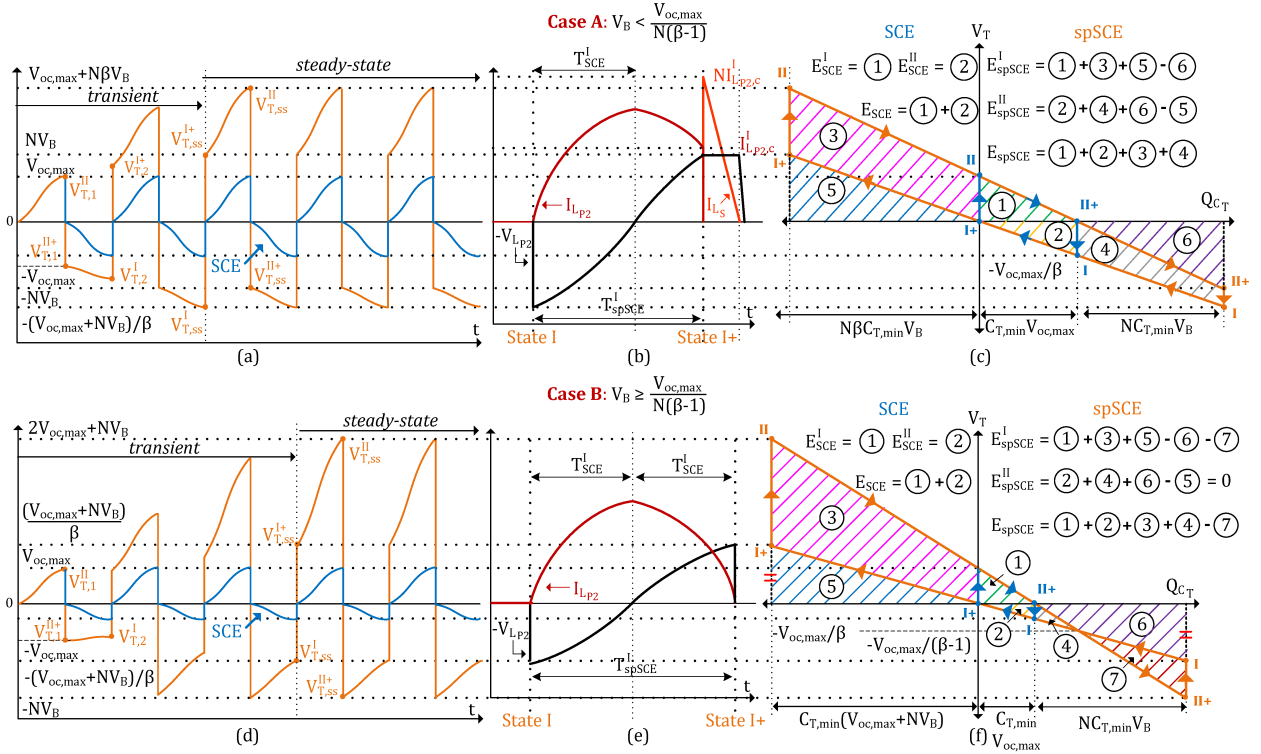


Figure 4.12 For spSCE circuit Case A/Case B: (a)/(d) TENG voltage waveform plot (orange in color); (b)/(e) Primary Inductor Current I_{LP2} , Voltage V_{LP2} and, Secondary Inductor Current I_{LS} during switching at State I under steady state; (c)/(f) TENG "Charge vs. Voltage" plot (orange in color). For SCE circuit: (a)/(d) TENG voltage waveform plot (blue in color) and (c)/(f) TENG "Charge vs. Voltage" plot (blue in color).

voltage V_{LP2} continues to rise from $-\frac{(V_{oc,max} + NV_B)}{\beta}$ until its maximum flipped value of $\frac{(V_{oc,max} + NV_B)}{\beta}$ is achieved at $2 \times T_{SCE}^I$. Then, the reversing primary inductor current I_{LP2} is blocked by reverse biased diode D_2 . In the process, no energy is delivered to the load and at State I+, we have:

$$V_{T,ss}^{I+} = -V_{T,ss}^I \left(= -\frac{Q_{CT,ss}^{I+}}{C_{T,max}} \right) = \frac{(V_{oc,max} + NV_B)}{\beta} \Rightarrow Q_{CT,ss}^{I+} = -C_{T,min}(V_{oc,max} + NV_B). \quad (4.28)$$

Next, with the plate separation continuing, the TENG reaches State II ($x = x_{max}$) while operating in open circuit condition so that $Q_{C_T,ss}^{II} = Q_{C_T,ss}^{I+}$, to yield:

$$V_{T,ss}^{II} = V_{oc,max} - \frac{Q_{C_T,ss}^{II}}{C_{T,min}} = 2V_{oc,max} + NV_B. \quad (4.29)$$

The rest of the operation cycle is similar as in Case A: a peak in $V_{T,ss}^{II}$ is detected to automatically switch on E_N to cause the inductor voltage $V_{L_{P1}} = V_T$ to fall from $V_{T,ss}^{II} = 2V_{oc,max} + NV_B$ to $-NV_B$ as shown in Fig. 4.13(b), forward biasing diode D2, charging the battery, freezing the secondary and hence primary side voltages, zeroing the primary side current, and auto switching off E_N . As in Case A, owing to the turns ratio, the secondary current spikes up to N times that of the primary current prior to the moment it became zero, and it decays linearly charging the battery. Also, at State II+, $V_{T,ss}^{II+} = -NV_B$ and $Q_{C_T,ss}^{II+}$ are the same as stated in Eq. (4.25), resetting the operation cycle.

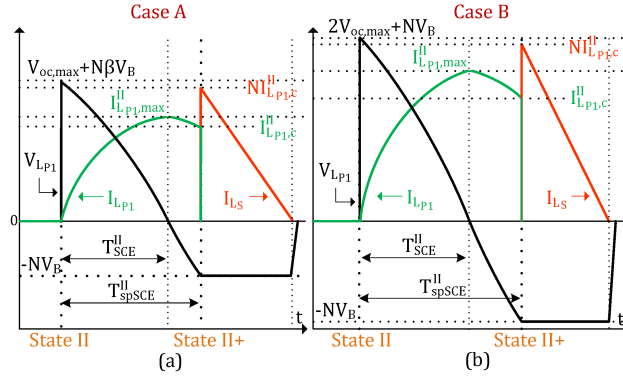


Figure 4.13 Steady-state Primary Inductor Current $I_{L_{P1}}$, Inductor Voltage $V_{L_{P1}}$, and Secondary Inductor Current I_{L_S} for the spSCE circuit during switching at State II under (a) Case A and (b) Case B load voltages.

Note for Case B, although the battery charging occurs only at State II but not at State I (in contrast to Case A, where the charging occurs at both the States), since Case B occurs at a higher battery level $V_B \geq \frac{V_{oc,max}}{N\beta-1}$, it still extracts higher per cycle energy than Case A as shown in the next subsection. However, Case B offers an additional challenge: It can be observed from Fig. 4.12(d) that in Case B, the TENG voltage at State II+ is a local minima, and the TENG voltage increases post State II+ in contrast to a monotonic decrease for Case A shown in

Fig. 4.12(a). This causes the comparator of the control circuit (see Fig. 4.4(a)) to revert back to state $-V_C$ prematurely, turning on the E_P earlier than desired and altering the expected operation. But this issue of Case B is easily resolved with the use of an electrically isolated parallelly operating auxiliary TENG (refer Fig. 4.3(e)) to provide input to the control circuit, without it loading the main TENG.

4.11.2 Per-Cycle Energy Output

As with the case of the SCE circuit, per-cycle energy output will be obtained using the V_T - Q_{C_T} plot. The steady-state values of V_T and Q_{C_T} derived for the spSCE circuit at States I, I+, II, and II+ above are used to obtain the plot of Fig. 4.12(c) and Fig. 4.12(f) for Case A and Case B, respectively.

Case A: Referring to Fig. 4.12(c), the $V_T - Q_{C_T}$ plot is similar for this case as in Fig. 4.7(b) and the per-cycle energy output is given by Eq. (4.19) and restated below:

$$E_{spSCE} = E_{spSCE}^I + E_{spSCE}^{II} = \frac{1}{2} C_{T,min} \left[(V_{oc,max} + N\beta V_B)^2 + \frac{(V_{oc,max} + NV_B)^2}{\beta} - (1 + \beta)(NV_B)^2 \right] \quad (4.30)$$

Case B: Considering the V_T - Q_{C_T} plot of Fig. 4.12(f), the energy extracted during II-II+ step is equal to the areas $\textcircled{1} + \textcircled{3} + \textcircled{5} - \textcircled{6} - \textcircled{7}$ and is given by:

$$E_{spSCE}^I = \frac{1}{2} \times C_{T,min} (2V_{oc,max} + NV_B) \times (2V_{oc,max} + NV_B) - \frac{1}{2} \times NC_{T,min} V_B \times NV_B. \quad (4.31)$$

Dually, the I-I+ step encloses the net area of $\textcircled{2} + \textcircled{4} + \textcircled{6} - \textcircled{5}$ in Fig. 4.12(f). Both the end points of the I-I+ line: $\left(C_{T,min}(V_{oc,max} + NV_B), -\frac{(V_{oc,max} + NV_B)}{\beta} \right)$ and $\left(-C_{T,min}(V_{oc,max} + NV_B), \frac{(V_{oc,max} + NV_B)}{\beta} \right)$ are equidistant from origin. Hence, the two vertically opposite triangles formed by the regions $\textcircled{5}$ versus $\textcircled{2} + \textcircled{4} + \textcircled{6}$ are congruent and cancel each other, yielding zero energy output. Above is an expected result as the circuit operation of State I to I+ for Case B fails to forward bias diode D_3 resulting in no load charging (refer Fig. 4.12(e)). It follows that the per-cycle energy output E_{spSCE} is simply E_{spSCE}^I derived above in Eq. (4.31).

As with the E_{spSCE} expression of Case A in Eq. (4.20), the E_{spSCE} expression for Case B, that equals Eq. (4.31), can also be rewritten as an increment over E_{SCE} :

$$E_{spSCE} = E_{SCE} + \frac{1}{2} C_{T,min} V_{oc,max} \left[\left(3 - \frac{1}{\beta} \right) V_{oc,max} + 4N V_B \right], \quad (4.32)$$

which again shows that the SpSCE output is always higher than that for SCE since $\beta \geq 1$ implies $\left(3 - \frac{1}{\beta} \right) > 0$. Also again, E_{spSCE} is an increasing function of V_B . It can also be easily checked that the energy outputs for the boundary condition ($V_B = \frac{V_{oc,max}}{N(\beta-1)}$) using the Case A or the Case B, Eq. (4.30) or Eq. (4.31), respectively, yield the same result.

4.12 Appendix D: Derivation of upper bound on load battery voltage for spSCE Circuit

To derive the upper bound on the load battery voltage, we repeat the analysis of transient circuit operation carried out in Appendix 4.10 with additional consideration of series parasitic resistance in the L_{P2} - $C_{T,max}$ and L_{P1} - $C_{T,min}$ resonator loops formed at State I and II, respectively.

At State II in k^{th} ($k < m$) cycle, with E_N enabled, the spSCE circuit can be simplified to that in Fig. 4.14(b). We analyze it first to obtain the relation between pre and post switching TENG voltages. The differential equation for this resonator loop obtained using KVL is given by:

$$\frac{d^2 V_{C_T}(t)}{dt^2} + \frac{R_{S1}}{L_{P1}} \frac{dV_{C_T}(t)}{dt} + \frac{V_{C_T}(t)}{L_{P1} C_{T,min}} - \frac{V_{oc,max}}{L_{P1} C_{T,min}} = 0.$$

This can be solved for TENG capacitor voltage $V_{C_T}(t)$ with initial condition as $V_{C_T}(0) = V_{C_T,k}^{II}$ to obtain:

$$V_{C_T}(t) = e^{-\frac{R_{S1}t}{2L_{P1}}} (V_{C_T,k}^{II} - V_{oc,max}) \left[\cos(\omega_d^{II} t) + \frac{R_{S1}}{2L_{P1}\omega_d^{II}} \sin(\omega_d^{II} t) \right] + V_{oc,max},$$

where ω_d^{II} is the resonance frequency given by,

$$\omega_d^{II} := \sqrt{\frac{1}{L_{P1} C_{T,min}} - \frac{R_{S1}^2}{4L_{P1}^2}}.$$

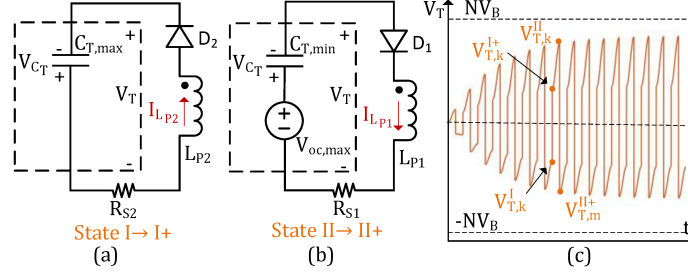


Figure 4.14 Simplified spSCE circuit during switching at (a) State I and (b) State II. TENG voltage (V_T) build up over time for load voltage higher than the upper bound.

Current in the loop reverses its direction and is blocked by diode D_1 at half the resonant time period $\left(t = \frac{\pi}{\omega_d^{II}}\right)$, i.e., at State II+:

$$V_{C_T,k}^{II+} = V_{C_T} \left(\frac{\pi}{\omega_d^{II}} \right) = -\alpha^{II} V_{C_T,k}^{II} + (1 + \alpha^{II}) V_{oc,max}, \text{ where,} \quad (4.33)$$

$$\alpha^{II} := e^{\frac{-\pi R_{S1}}{2\omega_d^{II} L_{P1}}} = e^{\frac{-\pi}{2Q_f^{II}}}, \text{ and } Q_f^{II} := \frac{\omega_d^{II} L_{P1}}{R_{S1}}. \quad (4.34)$$

Here, Q_f^{II} is the series resonator quality factor for switching at State II, and α^{II} is its “normalized” form.

The TENG voltage at the end of switching period (V_T^{II+}) can then be obtained from Eq. (4.33) and the TENG equation (4.3):

$$V_{T,k}^{II+} = V_{oc,max} - V_{C_T,k}^{II+} = -\alpha^{II} V_{T,k}^{II}. \quad (4.35)$$

On the other hand, during the switching at State I, the spSCE circuit is simplified to as shown in Fig. 4.14(a). Following the same process as above, we obtain:

$$V_{T,k}^{I+} = -V_{C_T,k}^{I+} = -\alpha^I V_{T,k}^I, \text{ where,} \quad (4.36)$$

$$\alpha^I := e^{\frac{-\pi R_{S2}}{2\omega_d^I L_{P2}}} = e^{\frac{-\pi}{2Q_f^I}}, Q_f^I := \frac{\omega_d^I L_{P2}}{R_{S2}}, \text{ and } \omega_d^I := \sqrt{\frac{1}{L_{P2} C_{T,max}} - \frac{R_{S2}^2}{4L_{P2}^2}}. \quad (4.37)$$

Next, we carry out the transient operation analysis starting from the rest. TENG operates under open circuit condition to reach State II with $V_{T,1}^{II} = V_{oc,max}$. Switch E_N is closed flipping V_T .

Using Eq. (4.35),

$$V_{T,1}^{II+} = -\alpha^{II} V_{oc,max} \Rightarrow Q_{C_T,1}^{II+} = (1 + \alpha^{II}) C_{T,min} V_{oc,max}.$$

Next, State I is achieved with open circuit condition, i.e., $Q_{C_T,2}^I = Q_{C_T,1}^{II+}$,

$$V_{T,2}^I = -\frac{Q_{C_T,2}^I}{C_{T,max}} = -(1 + \alpha^{II}) \frac{V_{oc,max}}{\beta}.$$

Using Eq. (4.36),

$$V_{T,2}^{I+} = \alpha^I (1 + \alpha^{II}) \frac{V_{oc,max}}{\beta}$$

Continuing the above process,

$$\begin{aligned} \Rightarrow V_{T,2}^{II} &= (1 + \alpha^I + \alpha^I \alpha^{II}) V_{oc,max}; \\ \Rightarrow V_{T,2}^{II+} &= -\alpha^{II} (1 + \alpha^I + \alpha^I \alpha^{II}) V_{oc,max}; \\ \Rightarrow V_{T,3}^{II+} &= -\alpha^{II} \left[\{1 + \alpha^I \alpha^{II} + (\alpha^I \alpha^{II})^2\} + \alpha^I \{1 + \alpha^I \alpha^{II}\} \right] V_{oc,max}. \end{aligned}$$

Following the above reasoning, TENG voltage in the k^{th} cycle at State II+ can be written as a sum of geometric series with common ratio $(\alpha^I \alpha^{II})$.

$$V_{T,k}^{II+} = -\alpha^{II} \left[\frac{1 - (\alpha^I \alpha^{II})^k}{1 - \alpha^I \alpha^{II}} + \alpha^I \frac{1 - (\alpha^I \alpha^{II})^{k-1}}{1 - \alpha^I \alpha^{II}} \right] V_{oc,max}.$$

For load charging to occur, $|V_{T,k}^{II+}| > NV_B$ condition should be satisfied. An upper bound to the battery voltage can be derived from the extreme case where no charging occurs even as $k \rightarrow \infty$, and with $\alpha^I \alpha^{II} < 1$, we get,

$$NV_B < \lim_{k \rightarrow \infty} |V_{T,k}^{II+}| = \left[\frac{\alpha^{II} (1 + \alpha^I)}{(1 - \alpha^I \alpha^{II})} \right] V_{oc,max}. \quad (4.38)$$

It can be shown that presence of other non-idealities such as diode voltage drop and leakage current through the off switches further reduces the upper bound.

4.13 Appendix E: Overall Experimental Setup and PCB Implementation

The overall experimental setup is shown in Fig. 4.15(a). A computer programmable stepper motor is used to move the upper electrode plate relative to the fixed bottom electrode plate (a

blow up of the same is shown in Fig. 4.15(b)). Fig. 4.15(a) also shows the implemented EEC and load. Output is measured using the oscilloscope and the data is collected through the NI's Data Acquisition Card and Labview program. The DC supply powers the control circuit so that the energy consumed by the control circuits of SCE/pSCE can be measured non-interferingly. Fig. 4.15(b) shows the main TENG (used for energy harvesting) in parallel with the auxiliary TENG required for the optimal timing implementation of the SCE circuit. Fig. 4.15(c) shows the schematic cross-section diagram of the TENG layers. The four circuits, namely, spSCE circuit with turns ratio $N = 1$, $N = 2$, SCE circuit with fixed switch timing, and SCE circuit with optimal switch timing all implemented on PCB using off-the-shelf components are shown in Fig. 4.16.

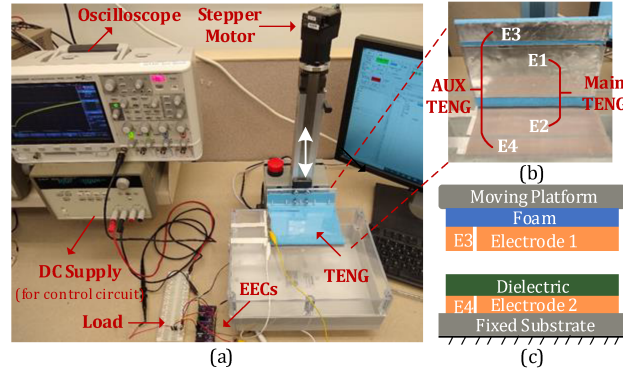


Figure 4.15 (a) Experimental Setup; (b) Disassembled view of TENG; (c) Schematic cross-section diagram of the implemented TENG showing the parallel auxilliary TENG used for driving control circuit of optimal SCE circuit.

4.14 Appendix F: Measurement of TENG's dynamic capacitance

TENG Capacitance ($C_T(t)$) is measured using the phase response method presented in [24, 28]. Below figure, shows measured C_T for our experimental TENG over 5 cycles of operation. Maximum and minimum TENG capacitance ($C_{T,max}$ and $C_{T,min}$) are deduced from the below plot by first taking a moving average with span of 2% and then finding the maxima and minima. Values obtained are 241.12 pF and 76.35 pF, respectively.

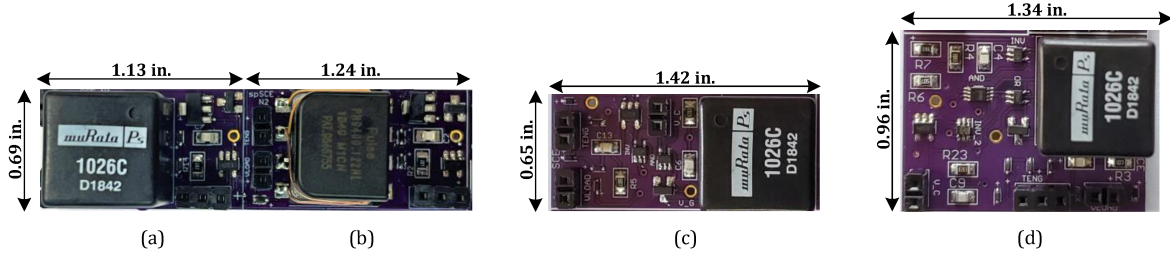


Figure 4.16 PCB implementations of the spSCE circuit with turns ratio (a) $N=1$, (b) $N=2$, (c) SCE circuit with fixed switch timing, and (d) SCE circuit with optimal switch timing.

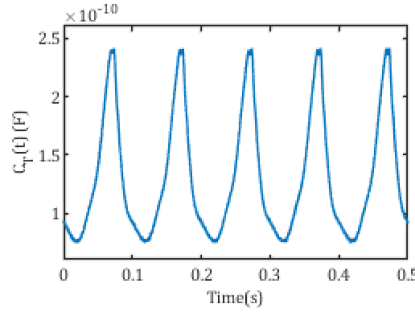


Figure 4.17 Measured time varying TENG capacitance ($C_T(t)$)

4.15 Appendix G: Measurement of TENG's maximum open circuit voltage

The maximum open circuit voltage ($V_{oc,max}$) is measured by charging a capacitor (of any value) until saturation using a Full Wave Rectifier (FWR) circuit as EEC and using the below relation [9, 21],

$$V_{oc,max} = (\beta + 1)(V_{sat} + 2V_D).$$

The measured saturation voltage (V_{sat}) using Keitley 6517 electrometer is 68.0 V. At saturation, negligible current flows through the FWR circuit and hence the diode drop (V_D) can be neglected, giving $V_{oc,max} \approx (\beta + 1)V_{sat} = 282.88$ V for the experimentally determined $\beta = 3.16$.

4.16 Appendix H: Alternate derivation of SCE circuit's per-cycle output energy

Here, energy delivered to the load at the end of the first half-cycle (E_{SCE}^I) is derived first. For energy extraction, the Switch S is closed with circuit simplified to as shown in Fig. 4.2(c). This resultant circuit is a $L_p - C_{T,min}$ oscillator and the differential equation governing the TENG capacitor voltage, $V_{C_T}(t)$ can be written as:

$$\frac{d^2 V_{C_T}(t)}{dt^2} + \frac{V_{C_T}(t)}{L_P C_{T,min}} - \frac{V_{oc,max}}{L_P C_{T,min}} = 0; t \geq 0; V_{C_T}(0) = 0.$$

Above can be solved for $V_{C_T}(t)$ with the initial condition as $V_{C_T}(0) = V_{C_T}^{II} = 0$ to obtain:

$$V_{C_T}(t) = V_{oc,max}(1 - \cos(\omega_{SCE}^{II}t)); \omega_{SCE}^{II} = \frac{1}{\sqrt{L_P C_{T,min}}}, \quad (4.39)$$

where ω_{SCE}^{II} is the resonance frequency of the oscillator. Then, by using KVL (Kirchhoff's Voltage Law) in the oscillator loop and Eq. (4.3), the voltage drop across L_p ($V_{L_P}(t) = V_{oc,max} - V_{C_T}(t)$) is equal to the TENG voltage ($V_T(t)$). The current in the loop (I_{L_P}) starts from a null value (initial condition) and leads the voltage waveform ($V_T = V_{L_P}(t)$) by phase of 90 degrees as plotted in Fig. 4.2(c). Based on Eq. (4.39), it can be deduced as,

$$I_{L_P}(t) = C_{T,min} \frac{dV_{C_T}(t)}{dt} = (C_{T,min} \omega_{SCE}^{II} V_{oc,max}) \sin(\omega_{SCE}^{II}t) \quad (4.40)$$

The switch S is opened after one-fourth the $L_P - C_{T,min}$ oscillation cycle, i.e., after the duration, $T_{SCE}^{II} = \frac{\pi}{2\omega_{SCE}^{II}}$, when I_{L_P} reaches its maxima of $I_{L_P,max}^{II}$ and hence the transferred energy to the inductor is at its peak of $\frac{1}{2}L_P(I_{L_P,max}^{II})^2$.

$$I_{L_P}(T_{SCE}^{II}) = I_{L_P,max}^{II} = C_{T,min} \omega_{SCE}^{II} V_{oc,max} \quad (4.41)$$

It is to be noted that during this period ($0 < t < T_{SCE}^{II}$), no current flows through the secondary loop because diode D is reverse biased. Opening switch S leads to a sharp cut-off of I_{L_P} in the primary loop (Refer Fig. 4.2(d)). The negative voltage developed on the coupled inductors due to this current fall is conducive for current flow in the secondary side, and I_{L_S} rises to a maximum of

$I_{LP,max}^{II}$ (taking coupling coefficient as 1 with $L_P = L_S$), which then is discharged through the diode D into the load battery.

Considering voltage drop of V_D across the diode D , using KVL in the secondary loop gives,

$$L_S \frac{dI_{LS}(t)}{dt} + V_B + V_D = 0 \Leftrightarrow I_{LS}(t) = -\frac{(V_B + V_D)}{L_S} t.$$

I_{LS} decays linearly from peak value of $I_{LP,max}^{II}$ to zero during the charging duration, say T_L^{II} (Refer Fig. 4.2(d)), which can be computed by integrating the above equation:

$$\int_{I_{LP,max}^{II}}^0 dI_{LS}(t) = \int_0^{T_L^{II}} \left(-\frac{(V_B + V_D)}{L_S} \right) dt$$

$\Rightarrow T_L^{II} = \frac{I_{LP,max}^{II} L_S}{(V_B + V_D)}$. (4.42) The energy delivered to the battery load is total charge flowing over the time T_L^{II} times the battery voltage,

$$E_{SCE}^I = V_B \int_0^{T_L^{II}} I_{LS}(t) dt = V_B \int_0^{T_L^{II}} \left(-\frac{(V_B + V_D)}{L_S} t \right) dt.$$

Substituting the value of T_L^{II} from Eq. (4.16) gives,

$$E_{SCE}^I = \frac{1}{2} \left(\frac{V_B}{V_B + V_D} \right) L_S \left(I_{LP,max}^{II} \right)^2 = \frac{1}{2} \left(\frac{V_B}{V_B + V_D} \right) L_P \left(I_{LP,max}^{II} \right)^2.$$

Plugging value of $I_{LP,max}^{II}$ from Eq. (4.41) and that of ω_{SCE}^{II} from Eq. (4.39), we get,

$$E_{SCE}^I = \frac{1}{2} \left(\frac{V_B}{V_B + V_D} \right) L_P \left(C_{T,min} \omega_{SCE}^{II} V_{oc,max} \right)^2 = \frac{1}{2} \left(\frac{V_B}{V_B + V_D} \right) C_{T,min} V_{oc,max}^2.$$

Similar analysis can be performed to find the energy delivered to the battery load at end of the second half-cycle to get,

$$E_{SCE}^{II} = \frac{1}{2} \left(\frac{V_B}{V_B + V_D} \right) C_{T,max} \left(\frac{V_{oc,max}}{\beta} \right)^2 = \frac{1}{2\beta} \left(\frac{V_B}{V_B + V_D} \right) C_{T,min} V_{oc,max}^2.$$

Then, the per cycle energy delivered to the load shall be,

$$E_{SCE} = E_{SCE}^I + E_{SCE}^{II} = \frac{1}{2} \left(\frac{V_B}{V_B + V_D} \right) \left(1 + \frac{1}{\beta} \right) C_{T,min} V_{oc,max}^2. \quad (4.43)$$

Thus, the derivation of E_{SCE} with the consideration of diode voltage drop (V_D) introduces the additional multiplication factor of $\frac{V_B}{V_B + V_D}$ to the ideal E_{SCE} of Eq. (4.9).

CHAPTER 5. HIGH VOLTAGE TRIBOELECTRIC ENERGY HARVESTING USING MULTI - SHOT ENERGY EXTRACTION IN 70V BCD PROCESS

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Express Briefs

5.1 Abstract

Triboelectric Nanogenerators (TENG) suitable for mechanical energy harvesting typically have ultra-high open-circuit voltage in several hundreds of volts, challenging the energy extraction circuit (EEC) design required for charging load battery/capacitor. Here, we present a novel multi-shot switched EEC that extracts energy in multiple discrete steps to regulate the TENG voltage below the breakdown limit of the technology (70 V in our case), making it suitable for Integrated Circuit (IC) implementation. The proposed strategy maintains high TENG voltage just below the breakdown limit to offer a high electrostatic retardation, enhancing the work done against it by the mechanical source in the form of transduced electrical energy. Mathematical derivation of the circuit's output shows a constant transduction power at all load voltages, fully eliminating Maximum Power Point (MPP) Tracking and saving power for the same. The design and simulation of the proposed EEC in TSMC 0.18 μm BCD process achieve a maximum power conversion efficiency of 63.3% and a 1.91x gain over even an *ideal* conventional Full Wave Rectifier (FWR) circuit at its optimal MPP load (gain will be higher for a real FWR implementation).

5.2 Introduction

Triboelectric Nanogenerators (TENGs) have received significant recent interest for harvesting ambient mechanical energy to prolong the battery-life of low-powered Internet of Things (IoT) devices. TENGs enjoy the advantage of wide material choice and versatile operating modes over other types of ambient mechanical energy transducers [1].

In practical applications, an Energy Extraction Circuit (EEC) is required to rectify the TENG's AC output to charge a DC load. Also, during the cyclic operation of TENG, the EEC architecture/operation together with load-voltage affect the TENG voltage/charge, influencing the TENG's electrostatic retardation force. The work done by the ambient mechanical force against this electrostatic retardation is the transduced electrical energy (denoted $E_{T,cycle}$ per cycle), and so the choice of EEC and load-voltage determine the transduced energy or equivalently, the average output power ($P_T = E_{T,cycle} \times f_e$, with f_e denoting the average source frequency). The Power Conversion Efficiency (PCE) is the fraction of P_T power delivered to the load (P_L), i.e., $PCE = P_L/P_T$. To this end, several EEC architectures have been explored in the literature and their corresponding optimal loads have been derived to enhance P_T and PCE [2][3].

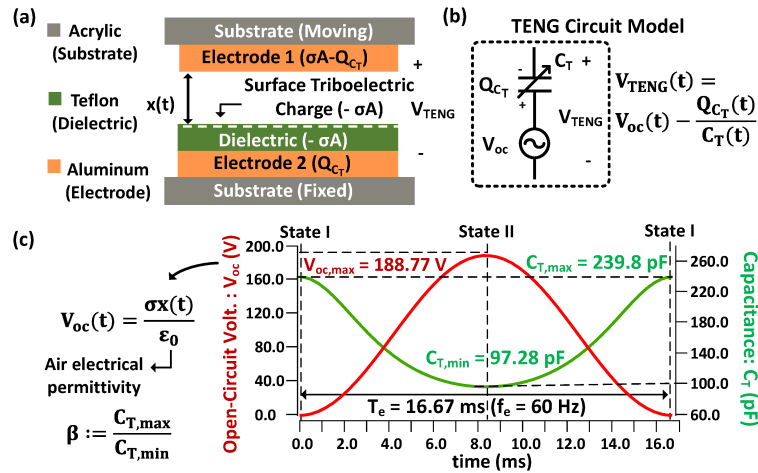


Figure 5.1 (a) Cross-section schematic of a standard contact-separation TENG, (b) its lumped circuit model, and (c) the plot of TENG parameters used for simulation in this work.

For normalized comparison of an EEC, the standard Full Wave Rectifier (FWR) circuit acts as the reference. FWR's MPP analysis shows that the P_T is maximized for load voltage, $V_{L,MPP}^{FWR} = \frac{V_{oc,max}}{2(\beta+1)}$ [4], where $V_{oc,max}$ denotes TENG's maximum open-circuit voltage and is achieved when the two plates of the contact-separation TENG (shown in Fig. 5.1(a)) are maximally apart (State II in Fig. 5.1(c)); the TENG capacitance (C_T) also varies during the operation, and the parameter β denotes the ratio of maximum to minimum TENG capacitances achieved respectively at State I (plates in contact) and State II (plates maximally separated). For a TENG with experimentally measured parameters as in [4], and used in this work (see Fig. 5.1(c) for values), the FWR MPP load is calculated as 27.2 V. The corresponding time-varying TENG voltage waveform simulated under *ideal conditions* is shown in purple in Fig. 5.2(a). The transduced per-cycle energy ($E_{T,cycle}$) of the ideal FWR EEC can be visualized as the area enclosed by the TENG voltage-charge (V_T - Q_{C_T}) plot shown in purple in Fig. 5.2(b). The corresponding transduced power at $f_e = 60$ Hz (typical excitation frequency for a machine health monitoring IoT) is listed in Fig. 5.2(c) and serves as a baseline for comparison with the proposed architecture of this work.

5.2.1 EEC ICs for TENG and our Contribution

Only a handful of EECs have been designed on-chip for TENG, such as [5, 6, 7, 8], primarily due to the challenge with its high voltage. In [5], a FWR followed by a switched capacitor charge pump (SCCP) is implemented in 65 nm CMOS technology. However, the operating voltage is restricted by their used technology to 2.5 V, and hence the typically high MPP load ($V_{L,MPP}^{FWR} = \frac{V_{oc,max}}{2(\beta+1)}$) cannot always be achieved. Thus, this implementation's P_T shall actually be smaller than that of the load-optimized FWR listed in Fig. 5.2(c).

The two half-cycles in TENG operation, i.e., separation (State I→II) and retraction (State II→I) of the TENG plates, are asymmetric due to the varying TENG capacitance (refer green curve in Fig. 5.1(c)). Hence, [6, 7] implemented a dual-output rectifier (DOR) followed by a dual-input buck converter in 70 V, 0.18 μ m BCD node that offers a separate MPP load for each

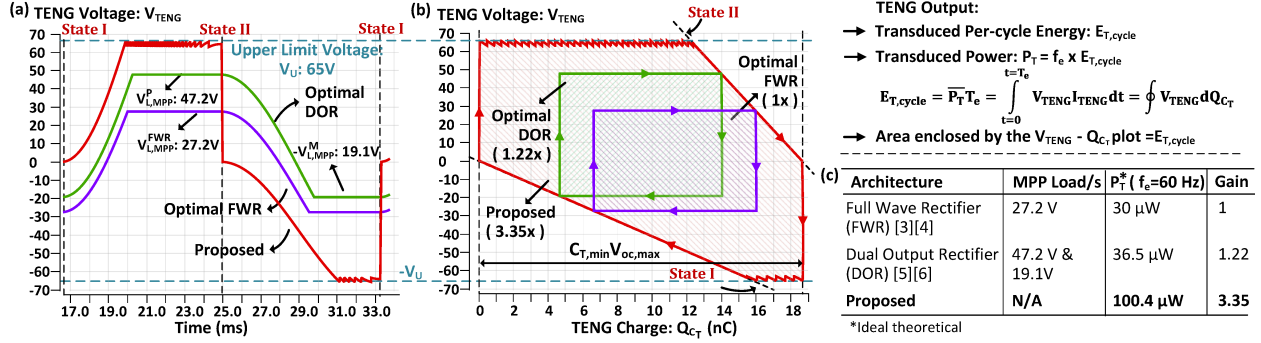


Figure 5.2 (a) The time-varying TENG Voltage (V_{TENG}) waveforms of load-optimized FWR, load-optimized DOR, and the proposed circuit for one periodic operation cycle; (b) corresponding TENG Voltage- Charge ($V_T - Q_{CT}$) plots. (c) Calculated transduced power (P_T) for the circuits under ideal implementation.

half-cycle. The two MPP loads (denoted $V_{L,MPP}^P$ and $V_{L,MPP}^M$) calculated for our test TENG with this approach are marked in the green curve of Fig. 5.2(a). Also, its transduced $E_{T,cycle}$ is co-plotted in green in Fig. 5.2(b) and its corresponding P_T is tabulated in Fig. 5.2(c).

We note that other techniques such as parallel synchronized switching harvesting on inductor (P-SSHI), that pre-bias (pre-charge) the TENG, can exceed the load-optimized FWR output, with [8] reporting an experimental gain of 1.62x over the FWR in 70 V, 0.18 μ m BCD process. However, similar to FWR, P-SSHI's P_T also shows a parabolic power response to the load-voltage with optimal load typically equal to several times the $V_{oc,max}$ [4], making it challenging to implement on-chip. Another alternative is Synchronous Charge Extraction (SCE) circuit [9] that is CMEQ (Cycle for Maximized Energy Output) [10] optimal guaranteeing at least a 4x gain over load-optimized FWR, but only under no constraint on operational voltage, making it again impractical for chip implementation. In this context, we propose an optimal voltage-constrained SCE approach with a multi-shot operation.

The main *contributions* of this work are 1) A new multi-shot energy extraction method that optimizes the transduced power (P_T) within the given voltage-constraint (IC technology's breakdown voltage); 2) Mathematical derivation of the per-cycle transduced energy (equivalently, power) that turns out to be independent of load-voltage, obviating the need for separate MPP

tracking (unlike FWR, Parallel/Series-SSHI circuits [4]); 3) Circuit implementation in 70 V BCD process achieving net PCE of 63.3%, a 1.91x gain over even an ideal load-optimized FWR.

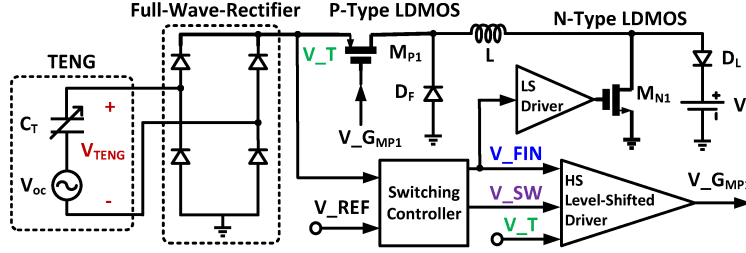


Figure 5.3 Schematic block diagram of the top architecture.

5.3 Proposed Circuit Operation and analysis

The proposed circuit architecture shown in Fig. 5.3 functions with the High-Side (HS) PMOS switch M_{P1} and Low-Side (LS) NMOS switch M_{N1} being normally off, and are enabled only for brief periods to extract the stored charge (equivalently, energy) from the TENG. The circuit operation commences with the two TENG plates together (State I in Fig. 5.1(c)), and as they separate, the TENG voltage rises in open-circuit condition (the ‘red’ curve in Fig. 5.2(a)). On reaching the upper limit voltage (V_U), selected as 65 V for a safety margin of 5 V from the breakdown voltage, as sensed by a comparator, the controller closes the HS PMOS switch for a brief period to start the “buck” action, transferring a part of the energy to the inductor L and load battery V_L , thereby reducing the voltage below but close to V_U . Subsequently, on opening the PMOS switch, the remaining stored energy on L is moved to the load via the freewheeling diode, D_F . This partial energy extraction is executed repeatedly at each instance the rectified V_{TENG} reaches V_U ($=65$ V) limit, and hence the name “multi-shot”, signified by the “see-saw” portion of the red-curve in Fig. 5.2(a). The rationale for maintaining ~ 65 V rather than extracting all the built-up energy (and letting TENG voltage fall to zero) is to maintain a higher electrostatic retardation to enhance the net transduced energy. Eventually, when the two TENG

plates are maximum apart, i.e., at the end of the first half-cycle (State II), the peak value prior to the continued dropping voltage is sensed by a peak detector circuit, closing the PMOS as well as the NMOS switch for sufficient time ($\geq 1/4^{th}$ the $LC_{T,min}$ oscillator time-period) to extract the energy until the voltage falls to zero. Subsequently, with the start of the second half-cycle (Fig. 5.2(a)), V_{TENG} rises in negative polarity and, post its rectification by the FWR, undergoes the same-as-before multi-shot energy extractions to regulate the voltage at V_U . Finally, at the end of the operation cycle (State I), all the energy on C_T is extracted, resetting the TENG for a new cycle. Note since the TENG capacitance is small, varying between $C_{T,min} = 97.28$ pF and $C_{T,max} = 239.8$ pF, and the inductor L is chosen to be $400 \mu\text{H}$, the switch-on times ($\sim \pi\sqrt{LC_T}/2 \leq 0.5 \mu\text{s}$) are negligible compared to the TENG operation time ($T_e = 16.67$ ms). The proposed multi-shot operation can also be understood visually from the red V_T - Q_{C_T} plot of Fig. 5.2(b) as the strategy to maximize the enclosed area (equivalently transduced per-cycle energy) with the constraint of 65 V as the upper limit. From the same plot, the per-cycle transduced energy for the proposed circuit can be derived as, $E_{T,cycle} =$

$$\begin{cases} C_{T,min} V_U \left[2V_{oc,max} - \frac{1}{2}(1+\beta)V_U \right], & V_U \leq \frac{V_{oc,max}}{\beta} \\ C_{T,min} V_U \left[V_{oc,max} - \frac{1}{2}V_U \right] \\ + \frac{1}{2\beta} C_{T,min} V_{oc,max}^2, & \frac{V_{oc,max}}{\beta} < V_U < V_{oc,max} \\ \frac{1}{2} \left(1 + \frac{1}{\beta} \right) C_{T,min} V_{oc,max}^2. & V_U \geq V_{oc,max} \end{cases} \quad (5.1)$$

For this work, the first case applies as $V_U = 65$ V is less than $V_{oc,max}/\beta = 76.43$ V, and as per it, the calculated $E_{T,cycle}$ is $1.674 \mu\text{J}$ which corresponds to P_T of $100.4 \mu\text{W}$ at $f_e = 60$ Hz. From Fig. 5.2(c), this translates to a 3.35x gain over the load-optimized FWR (in ideal conditions). Fig. 5.4(a) plots $E_{T,cycle}$ as a function of TENG's $V_{oc,max}/V_U$ with demarcation between the above-defined three cases under $\beta = 2.47$ (as per the TENG used in this work). Also from the inset of Fig. 5.4(a), note the three distinct V_{TENG} waveforms: The multi-shot operation occurs only during the first-half cycle in the second case, while the third case equals the SCE circuit case [9] (when $V_U \geq V_{oc,max}$, the switching occurs only at the extremes as in a normal SCE circuit[9]).

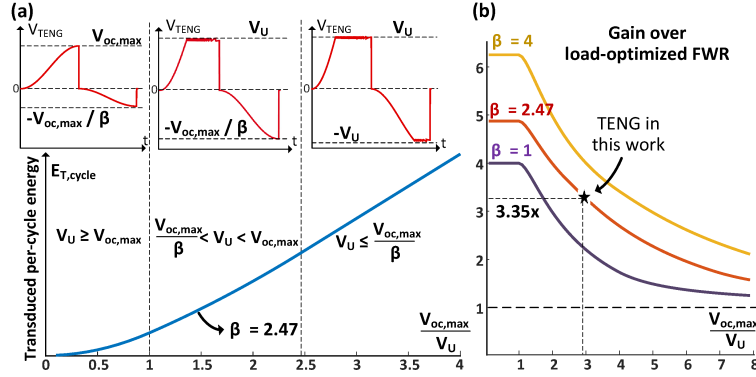


Figure 5.4 (a) Transduced per-cycle energy vs. ratio of maximum open-circuit voltage to breakdown voltage: $V_{oc,max}/V_U$ at max. to min. TENG capacitance ratio, $\beta = 2.47$. (b) Gain over load-optimized FWR at $\beta = 1, 2.47$, and 4 vs. $V_{oc,max}/V_U$.

Further, from the above equations, it is evident that the transduced energy (equivalently, power) is independent of the load-voltage, another novelty of the proposed circuit, obviating the need for a separate MPP circuit (thereby avoiding its overhead loss).

The gain of proposed circuit over load-optimized FWR obtained by dividing the $E_{T,cycle}$ of Eq. (1) with optimized FWR's output, E_{MPP}^{FWR} [4] is as below:

$$\text{Gain} = \frac{E_{T,cycle}}{E_{MPP}^{FWR}}, \text{ where } E_{MPP}^{FWR} = \frac{C_{T,min} V_{oc,max}^2}{2(1 + \beta)}, \quad (5.2)$$

and is plotted in Fig. 5.4(b) for three different values of β over a range of $V_{oc,max}/V_U$ values. The gain is always greater than 1 for any set of TENG parameters.

5.4 Proposed Circuit Implementation

The proposed circuit shown in Fig. 5.3 comprises of on-chip 70 V rated diodes, a P-Type LDMOS for the HS switch, a N-Type LDMOS for the LS switch, and a 400 μH inductor with ESR of 1 Ω . The circuit is designed for handling the expected $\sim 100 \mu\text{W}$ power level. The top-level simulated waveforms for one operation cycle are shown in Fig. 5.5(b).

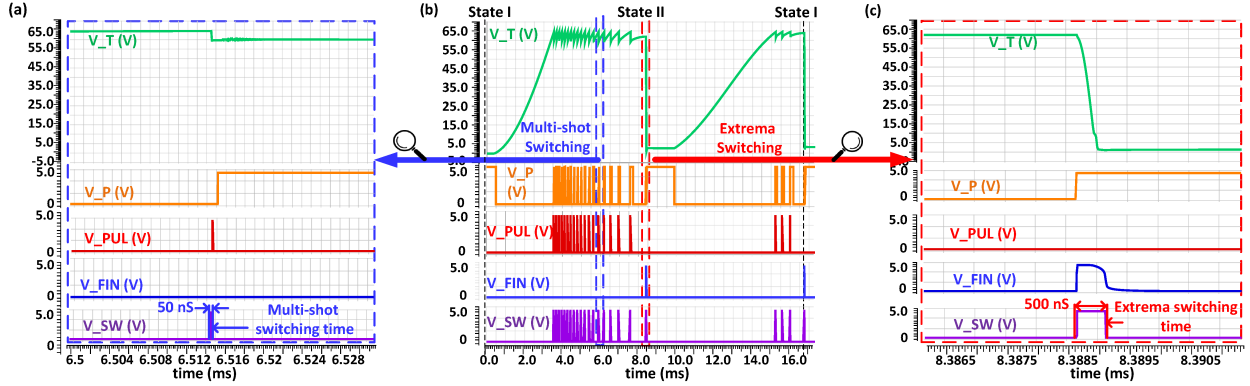
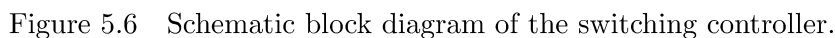


Figure 5.5 (a) Zoomed-in view of various control signals and the rectified TENG voltage (V_T) during one of the multi-shot switching step. (b) Various controller signals and V_T during one operation cycle. (c) Zoomed-in view of various control signals and V_T during the extrema switching at State II.

5.4.1 Switching Controller

The role of switching controller in Fig. 5.3 is to generate two types of gate voltage pulses: *multi-shot operation* switching pulses on sensing V_U ($=65$ V) and the *extrema-detection* switching pulses at the two TENG operation extrema of States I and II. As shown in Fig. 5.6, rectified TENG voltage (V_T) is scaled down using a voltage divider and fed to a comparator whose output (V_C) on sensing 65 V, triggers Pm, the pulse generator unit (Fig. 5.6). The required multi-shot operation switching signal (V_{PUL}) with a fixed pulse-width of ~ 50 ns is generated by setting the RC values of Pm and is passed on as the controller's output (V_{SW}). Fig. 5.5(a) shows the zoomed-in view of one of the multi-shot switching instances with the fall of V_T from 65 V to ~ 60 V due to this switching step.

For the switching at the two extrema of States I and II, a peak detector circuit inspired from [11] and modified to suit the current application is used. The zoomed-in view of this switching process is shown in Fig. 5.5(c). The peak detector triggers the required switching pulse (V_{FIN}) with a width sufficient for the TENG voltage (V_T) to reach zero at both States I and II. For our TENG parameters, it is set to ~ 500 ns using the pulse generator unit Pe (Fig. 5.6). Note that the transition of V_T from 65 V to 60 V during multi-shot switching creates a local maxima that



The level-shifted driver shown in Fig. 5.7(a) is utilized to switch the HS PMOS M_{P1} (see Fig. 5.3) since its source terminal is connected to the floating V_T signal. As in Fig. 5.7(a), for the multi-shot switching, the transistor M_{N6} is enabled to raise the gate signal level through the V_T fed resistor divider R3-R4. The divider ratio is chosen to pull down the gate (V_GMP1) ~ 5 V lower than V_T to fully turn on M_{P1} as V_T transitions from 65 V to 60 V. However, the extrema switching requires the V_T to fall fully to zero. This leads to the $|V_{gs}|$ set by the fixed R3-R4 divider falling short of fully turning on M_{P1} at a low V_T value (refer ‘blue’ waveform in Fig. 5.7 (b)), in turn, increasing the PMOS conduction losses. Hence, to achieve “adaptive divider ratio” during extrema switching, an auxiliary path is designed as shown in Fig. 5.7(a): Here using a comparator, V_T falling below 10 V is detected and the resistor R5 is activated (using V_SW2 signal) to increase the $|V_{gs}|$ for M_{P1} . The comparator here is enabled only during the extrema switching to reduce its average quiescent power consumption. The zoomed-in view of this switching process at State I is shown in Fig. 5.7(b). The size of M_{P1} and the driver design have been optimized for maximum PCE.

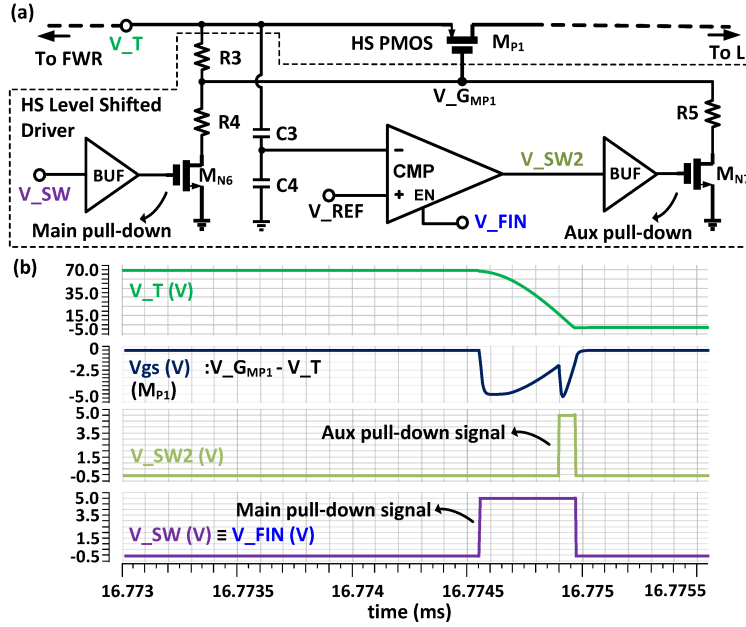


Figure 5.7 (a) High-Side Level-Shifted driver circuit diagram and (b) zoomed-in view of switching signals and the V_{gs} voltage of M_{P1} during the extrema switching at State I.

5.5 Simulation Results

The presented circuit for triboelectric ambient energy harvesting is for *low frequency* ($f_e = 60$ Hz) and *low power* (in microwatts) operation and hence, any added parasitics in the post layout simulations are expected to have a negligible impact. For validating this, we layout the most *critical circuit blocks*, namely, peak detector, comparators in the controller, and the HS level-shifted switch driver, and report the post-layout simulation results for the TENG with parameters marked in Fig. 5.1(c). The proposed circuit transduced $P_T = 90.33 \mu\text{W}$ of power and delivered $P_L = 66.66 \mu\text{W}$ to the load at PCE of 73.79% (for the load-voltage of $V_L = 20$ V as listed in Fig. 5.8(b)). Note that the mathematically calculated P_T of $100.4 \mu\text{W}$ is for idealized implementation corresponding to a constant $V_U = 65$ V during the multi-shot operation. It is intuitive from the V_T - Q_{CT} plot of Fig. 5.2(b) that in real implementation with a finite multi-shot switching ripple voltage of ~ 5 V, transitioning between 65 V and 60 V as in Fig. 5.5(b), the area under the V_T - Q_{CT} is gets diminished leading to a lower P_T . Note the trade-off of increasing P_T by

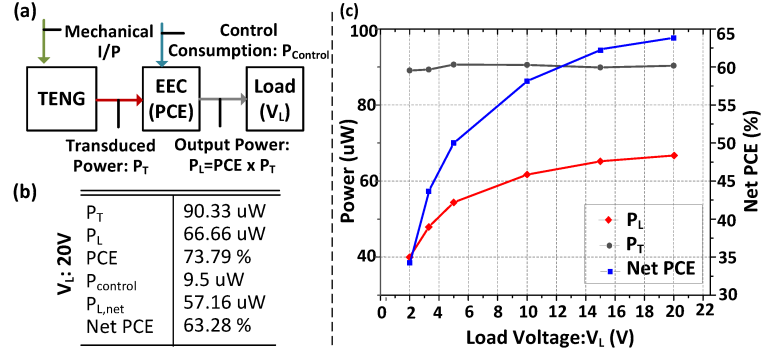


Figure 5.8 (a) Overall power flow diagram. (b) List of simulated EEC performance metrics at 20V load-voltage (V_L). (c) Plot of simulated transduced power (P_T), load (output) power (P_L) and Power Conversion Efficiency (PCE) against load voltage (V_L).

a reduction in the V_T ripple is in the form of higher switching loss due to an increased number of switching instances that eventually reduce P_L .

The flat response of the transduced power (P_T) to the varying load voltage (see Fig. 5.8(c)) validates the mathematized load-voltage agnostic power extraction behavior of the proposed EEC. The mild dependence of the output power (P_L) on V_L at lower values of V_L seen in Fig. 5.8(c) is primarily due to the voltage drop across the two diodes (D_F and D_L) of $2V_D \approx 1.5$ V that reduces the P_L by roughly the factor of $\frac{V_L}{V_L + 2V_D}$, which manifests more significantly at lower V_L .

All of the active controller circuit components are powered at 5 V supply voltage and consume an overall power of $P_{control} = 9.5 \mu\text{W}$, yielding the net output power of $P_{L,net} = 57.16 \mu\text{W}$ with net PCE of 63.28%. The operation with output voltage in the range of 2-20 V is verified as in Fig. 5.8(c); however, it can be set up to V_U . Note the presented battery charging application does not require voltage regulation as also in [6, 7], but if demanded by the application, a second stage inductive or capacitive switched-converter can be integrated for output voltage regulation. With the DC-DC converter's expected efficiency of 85%, the output power with regulated voltage can be expected to be $48.58 \mu\text{W}$, offering an end-to-end PCE of 53.78%.

A comparison with prior chip-level designs for TENG energy extraction is provided in Table 5.1. Note since the goal is to maximize the power extracted from the given transducer, the *Transduced Power Gain* over the standard FWR circuit is the key figure of merit for a normalized comparison. The proposed implemented circuit achieves a net 1.91x Transduced Power Gain over even the *ideal* FWR's P_T of 30 μW at its MPP load (gain shall be higher with respect to a real FWR owing to the MPPT overhead consumption and the parasitic losses). When compared to the methods of [6] and [7], the net 1.91x gain is also higher than even their ideal-circuit theoretical gain of 1.22x (refer Fig. 5.2(c)), clearly showing the superiority of the proposed method over [6] and [7].

Table 5.1 Performance comparison with reported ICs for TENG

Ref/Parameter	JSSC'19 [6]	JSSC'20 [7]	TCAS-I'20 [8]	This Work ^[a]
Process	0.18 μm 70V BCD	0.18 μm 70V BCD	0.18 μm 70V BCD	0.18 μm 70V BCD
Energy Extraction Method	Dual output rectifier with MPPT	Dual output rectifier with integrated MPPT	P-SSHI	Multi-shot SCE
MPPT Requirement	Yes	Yes	Yes	No
Operation freq. [Hz]	50	40 - 60	1 - 5	60
# Off-chip LR components	1L (1 mH)+ 4R (30 $\text{G}\Omega$)	1L (10 mH)	2L (1 mH)	1L (0.4 mH)
Input Voltage [V]	3.5 - 70	< 70	12 - 70	< 70
Transduced ^[b] (Input) Power [μW]	4.5 - 20.7	3.9 - 10.5	2214	90.33
Output Voltage [V]	2 - 5 ^[c]	2.8 - 3.3 ^[c]	2	2 - 20 ^[c]
Net Output ^[b] Power [μW]	10.95	4.22	772	57.16
Peak Net PCE [%]	54.5	84.7	32.71 ^[d]	63.28
Transduced Power Gain over FWR	1.11 $\times$ ^[a]	N/A	1.62 $\times$	> 1.91 $\times$

[a] Simulation Results; [b] At Peak PCE; [c] Unregulated; [d] Including the output voltage regulation stages.

5.6 Conclusion

This paper presents an IC design in a 70 V BCD process of a universally optimized voltage-constrained synchronous charge extraction (SCE) energy extraction circuit (EEC) for the Triboelectric Nanogenerator (TENG) transducers. The proposed strategy addresses the challenge of TENG's high open-circuit voltage nature by extracting energy in multiple short bursts (termed “multi-shot” operation) at the upper (breakdown) voltage limit of the given IC technology. Additionally, the constant level of transduced power of the proposed EEC design, regardless of the load-voltage, automatically offers MPP tracking, unlike the case of other EECs such as FWR, P-SSHI, S-SSHI, etc. Mathematical derivation of the proposed EEC's transduced power revealed a 3.35x gain over the load-optimized FWR circuit using our test TENG parameters at an operating upper limit of 65 V. The simulation of the proposed EEC in TSMC 70 V BCD process showed a net output of 57.16 μW at 20 V load, achieving a net PCE of 63.28% that translates to a 1.91x gain over even an ideal load-optimized FWR circuit (gain will be higher with respect to a real FWR implementation).

5.7 References

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CHAPTER 6. GENERAL CONCLUSION

Triboelectric Nanogenerator (TENG), a class of kinetic ambient energy harvesters, is a promising technology for enabling ‘maintenance-friendly’ extended battery-life or self-powered, battery-free Internet of Things (IoT) sensors. Its major advantage is that all materials have triboelectric properties, offering the flexibility of design, fabrication, and operation mode to suit the application. In practical applications, a rectifying Energy Extraction Circuit (EEC) is further required to interface the TENG having AC output with the IoT’s onboard DC storage (battery/capacitor). The choice of EEC architecture/operation also determines the TENG’s per-cycle energy output, and the design of advanced EECs beyond the basic Full Wave Rectifier (FWR) circuit provides a generalized approach for boosting the energy output of any given TENG. In that context, this research proposed and developed multiple novel synchronously switched EEC architectures that enhance the energy extracted from TENG beyond that achieved by the standard FWR. This work covered the following *seven* circuit architectures as TENG EEC candidates,

- Standard Full Wave Rectifier circuit (FWR) (*reference circuit for comparison*)
- Synchronous Switched Harvesting on Inductor (SSHI) class of circuits:
 - Parallel-SSHI
 - Series-SSHI
- Synchronous Charge Extraction (SCE) class of circuits:
 - Standard SCE
 - Pre-biased SCE (pSCE)
 - Self-propelled Pre-biased SCE (spSCE)
 - Multi-Shot SCE (MS-SCE)

wherein, other than the Standard FWR and Standard SCE, rest of all the architectures were proposed as TENG EECs for the first time.

6.1 Key Contributions

The main contribution of this research is developing a generalized self-tuned approach for enhancing the per-cycle energy output of any given TENG operating under any given ambient input condition by using the developed synchronous switched energy extraction circuits. The research developments covered in this dissertation have been disseminated through the following publications:

Journal publications:

- [J1] **M. Pathak** & R. Kumar, “Synchronous Inductor Switched Energy Extraction Circuits for Triboelectric Nanogenerator”, *IEEE Access*, Vol. 9, 2021.
- [J2] **M. Pathak** & R. Kumar, “Synchronous Pre-biasing of Triboelectric Nanogenerator for Enhanced Energy Extraction”, *IEEE Transactions on Power Electronics*, Vol. 37, Issue 10, 2022.
- [J3] **M. Pathak** & R. Kumar, “Self-propelled Pre-biased Synchronous Charge Extraction Circuit for Triboelectric Nanogenerator”, *IEEE Journal of Emerging and Selected Topics in Power Electronics*, Early Access, 2022.
- [J4] **M. Pathak**, S. Xie, C. Huang, & R. Kumar, “High-Voltage Triboelectric Energy Harvesting using Multi-Shot Energy Extraction in 70V BCD Process”, *IEEE Transactions on Circuits and Systems II: Express Briefs*, Vol. 69, Issue 5, 2022.

Conference publications:

- [C1] **M. Pathak** & R. Kumar, “Modeling and analysis of energy extraction circuits for triboelectric nanogenerator based vibrational energy harvesting”, *Proc. SPIE Energy Harvesting and Storage: Materials, Devices, and Applications VIII*, Vol. 10663, 2018.
- [C2] **M. Pathak** & R. Kumar, “Pre-Biased Synchronous Charge Extraction for Triboelectric Nanogenerator”, *Proc. IEEE Sensors*, 2019.

The key contributions of the above works are summarized below.

The first set of work [J1][C1] proposed the use of Parallel and Series Synchronous Switched Harvesting on Inductor (P-SSHI and S-SSHI) circuits as energy extraction circuits (EECs) for TENG, which involve switching at the TENG voltage output extrema to obtain manifold energy gain over the standard Full Wave Rectifier (FWR) circuit with following key contributions,

- The closed-form equations for the per-cycle energy output of both the P-SSHI and S-SSHI circuits at a given battery load are derived for the first time. In addition, the upper limit on battery load, optimal battery load, effect of TENG parameters (determined by construction and operation of the given TENG), and circuit non-idealities on the per-cycle output have been captured in the models to guide the design of these EECs.
- Validation of the presented analytical models by way of a close match with those experimentally measured and PSpice simulated per-cycle energy output at different battery loads showed that the analytical models can be used to assess TENG EEC performance once the TENG parameters have been measured.
- Comparison of P-SSHI, S-SSHI, and the standard FWR circuit in a common framework to bring forward their respective pros and cons.

The SSHI circuits achieved the intended goal of superior performance over the standard FWR circuit with experimental implementation showcasing the P-SSHI and S-SSHI circuit's gain of 1.18 and 8.59 over the standard FWR circuit at the load voltage of 15 V, respectively. Their energy outputs showed a parabolic response providing an optimal battery load voltage and an upper bound. This nature may warrant the additional need for an integrated, second-stage DC/DC converter with a closed-loop Maximum Power Point Tracker (MPPT) circuit to maintain operation at the optimal load voltage as the input ambient vibration conditions vary.

In the next set of works [J2] [C2], the Synchronous Charge Extraction (SCE) class of circuits that uses a flyback transformer to isolate the source and load sides are studied. The key advantage of the SCE circuit is its constant transduced energy, irrespective of the load voltage,

providing MPPT-free operation. Building upon the SCE architecture, a pre-biased SCE (pSCE) EEC is proposed that always outperforms SCE and its energy output continues to grow with the load voltage. The key contributions of these works are,

- The fundamentals of pre-biasing (pre-charging) the TENG at the start of the operation cycle to enhance the per-cycle extracted energy are presented. It is shown that the increase in output energy due to pre-biasing in the first half-cycle of TENG operation (separation of the TENG plates) is attributed to the increase in the transduced energy from the mechanical source due to the addition of extra charges on the plates, leading to more mechanical work against the induced electrostatic attraction. In contrast, the gain in the second half-cycle (retraction of plates) is due to a reduction in the TENG electrical (potential) energy that is dissipated back into the environment (retraction motion being in the same direction as electrostatic attraction).
- The energy gain due to pre-biasing is mathematically formulated, and the optimum pre-biasing voltage (equivalently charge) is derived.
- A novel Energy Extraction Circuit (EEC) termed as “Pre-biased Synchronous Charge Extraction (pSCE)” is introduced to realize synchronous pre-biasing of TENG using the load battery itself and subsequently achieve enhanced energy extraction from TENG. Its energy output and conditions on pre-biasing voltages for net-benefit over the SCE circuit are derived.
- The experimental implementation is performed for the proposed pSCE circuit that shows a 6.65-fold gain over the standard FWR and 1.45 over the SCE circuit for a 5V battery load. A quantitative comparison with the EECs in prior works has also been tabulated.

A drawback with pSCE lies in its complex control requiring TENG-specific manual tuning and 13 active (power-consuming) components. The next proposed architecture termed Self-propelled pSCE (spSCE) reported in [J3] addressed this challenge by offering self-tuned pSCE operation with a simple control circuit having only one active component and the following salient features:

- Self-propelled switching with automatic tuning of the switch-on period, making it a universal plug-and-play EEC, i.e., applicable for any TENG and any operating condition of ambient vibration.
- Inbuilt pre-biasing (pre-charging of TENG capacitor at each operation extreme) to yield per-cycle energy output beyond the SCE circuit by increasing the net energy transduced from the mechanical source.
- An innovative low-power control circuit for synchronous switching (with only one active component) that employs the proposed depletion type MOSFET (as opposed to a typically used enhancement type MOSFET) switch. This scheme is measured to consume 161.2% lesser per-cycle overhead energy than its SCE counterpart.
- Experimental validation showing 119.7% per-cycle net energy gain measured over the SCE circuit at battery load of 5 V, which rises to 163.7% at battery load of 15 V.

Next, we report a novel on-chip suitable energy extraction technique, Multi-Shot SCE (MS-SCE) [J4] with the following contributions,

- A new multi-shot energy extraction method that optimizes the transduced power within the given voltage-constraint (IC technology's breakdown voltage);
- Mathematical derivation of the per-cycle transduced energy (equivalently, power) that turns out to be independent of load-voltage, obviating the need for separate MPP tracking (unlike FWR, Parallel/Series-SSHI circuits);
- Circuit implementation in 70 V BCD process achieving net PCE of 63.3%, a 1.91x gain over even an ideal optimal FWR (operating at its MPP).

The developed MS-SCE framework for energy extraction is shown to be universally-optimal, as in always providing higher energy output than the standard optimal FWR for any given TENG under any operation condition and scalable, as in it can be used for optimized energy extraction in any voltage-rated IC technology.

In summary, this research makes significant contributions in developing energy extraction circuits for interfacing Triboelectric kinetic energy harvester that shall guide the choice and design of future academic and commercial energy harvester integrated IoT applications.

6.2 Future Directions

The accomplished research has generated insights for designing interfacing circuits that maximize the energy extracted from any given Triboelectric Nanogenerator (TENG). Some of the directions in which this work can be extended are,

- Here presented Energy Extraction Circuits (EECs) have been tested in-lab using an experimental TENG for proof-of-concept validation. For prototyping a complete TENG-powered IoT system, the developed EECs need to be integrated and tested with a field-deployable TENG. A starting application can be harnessing the machine body vibrations for self-powered machine health monitoring IoT.
- A cold-start circuit can be integrated with the self-propelled pre-biased SCE (spSCE) circuit to make it suitable for battery-less IoT systems. Since spSCE action requires overhead power, during the startup, a parallel *passive* full wave rectifier circuit pathway can be used to charge the storage capacitor until it reaches a threshold voltage and starts providing for the spSCE control.
- The on-chip designed EEC, Multi-Shot SCE, has been validated through simulation. Its tapeout and testing can be pursued to determine the chip area and experimental efficiency.
- TENGs are high-voltage and low-charge sources, and leakage through off-state Silicon MOSFET switches in the EEC is found to be a major source of parasitic energy loss. Other switching technologies with high-rated voltage and low leakage charge can be explored.
- For sensors deployed in environments where in addition to ambient kinetic energy, other forms of energy such as light/thermal/RF are available, a multi-input-modality charging interface integrating the advanced EEC for all kinds of transducers can be developed.

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