Systems for electromigration study under frequency effect and non-uniform thermal effect: design, fabrication, and testing

by

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The student author, whose presentation of the scholarship herein was approved by the program of study committee, is solely responsible for the content of this dissertation.
The Graduate College will ensure this dissertation is globally accessible and will not permit alterations after a degree is conferred.

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DEDICATION

To my family, friends who held me up over the years with their endless love

Deeply grateful to God for blessing me with this life

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ABSTRACT

The semiconductor industry has made great strides in recent times. On-chip integrated circuits are built using many discrete CMOS (complementary metal oxide semiconductor) devices that perform various functional operations. Today, an entire multicore processor can be built on a single piece of silicon. This massive downscaling has been possible due to miniaturization of the silicon MOS transistor in very large scare scale integration (VLSI). Any IC's lifetime is a function of both device and interconnect wear out.

The conventional approach to ensuring product's thermal reliability involves conducting accelerated aging tests, exposing a product to elevated temperatures and voltages (also known as a stress test or High Temperature Operating Life (HTOL) test) for a duration that estimates the product's entire lifespan under normal usage conditions by the customer.

Electromigration (EM) is the transport of conductor metal atoms caused by the momentum transfer from the conducting electrons. As device sizes shrink, it becomes possible to increase the number of devices per unit area, enhancing device density and causing higher current density within the device, which in turn raises operating temperatures non-uniformly within the ICs. Further, the need for high-speed operation results in a higher frequency switching that has its own ramifications towards heating pattern. These factors collectively contribute to making electromigration a significant challenge for the reliability of contemporary ICs.

Before working on new test structures to detect EM failure under high frequency and non-uniform heating effect, an elaborative literature review is pursued to understand the complex electromigration physics and to understand the previous work which are done to study EM failure under low to high frequency effect. We have designed novel test chips fabricated using Intel's 22FFL process technology to assess EM impact on failure rate of high current densities on Cu-based metallurgies. We have demonstrated the ability for these circuits to characterize direct

current (DC), unidirectional pulsed DC as well as bidirectional pulsed AC stress EM effects up to GHz frequencies. Heater structure design enables localized thermal stress up to 300 ^{o}C and is compatible with high-speed CMOS logic infrastructure. Time dependent modulation of the EM effects is studied on 90p Cu alloy metallurgy and results are presented for the first time.

The demand of increased accelerated temperature with a spot heating capability motivated us to pursue a novel method of laser based electromigration testing. This approach facilitates the analysis of thermal effects in two keyways: (1) it confirms the adequacy of the test temperature with high precision, and (2) it assesses the temperature-related aging and susceptibility of specific IP blocks within the silicon. Our method provides both high spatial precision and rapid testing, as a few days of laser-induced temperature stress reproduces the effects of multiple years of regular usage, while the rest of the chip remains unaffected and continues to operate normally. As per our knowledge, this is the first time a non-uniform temperature based electromigration effects are made possible and the corresponding results are depicted.

CHAPTER 1. GENERAL INTRODUCTION

1.1 Background

In semiconductor world, the CMOS devices face reliability issues such as bias temperature instability (BTI), hot carrier injection (HCI), time-dependent dielectric breakdown (TDDB), soft error rate (SER) which create increased circuit delay, soft break down, hard failure of the devices. Whereas back-end metal interconnects face the electromigration and thermal migration failures.

Electromigration (EM) refers to the movement of metal atoms within a conductor, driven by the momentum transfer from the electron flow. When electric field is applied, current flows through a metal interconnect, and two forces are exerted on its metal ions, the first force is the electrostatic force caused by the electric field in the same direction of electric field, and the second force is the wind force generated by the momentum transfer between the conducting electrons and metal ions in the metal line in the direction of electron. When resulting force is higher than activation energy, then metal ions start to diffuse from negatively biased cathode node to positively biased anode node of the interconnect, after a significant diffusion, a void creates at cathode and hillock generates at anode [1], [2]. This phenomenon is called electromigration (EM), which is described elaborately in chapter 2.

The semiconductor industry has advanced significantly in recent years. On-chip integrated circuits are constructed using numerous discrete CMOS (complementary metal oxide semiconductor) devices that carry out various functional tasks. Nowadays, a complete multicore processor can be fabricated on a single silicon chip. This substantial reduction in size has been achieved through the miniaturization of silicon MOS transistors in very large-scale integration (VLSI). The lifespan of any integrated circuit is influenced by the wear and tear of both the devices and the interconnects.

The increase in number of devices significantly increases the current density. This, in turn, has heightened the risk of BEOL (Back-End-of-Line) connectivity failures and consequently shortened the lifespan due to electromigration (EM).

1.2 Motivation for this work

Despite decades of research on electromigration (EM) in the context of technology scaling, its behavior under unidirectional pulsed DC, bidirectional pulsed AC currents, and under non-uniform heat conditions remains not fully understood.

With the rise of high-speed applications in circuits, any delay caused by increased metal interconnect resistance due to electromigration (EM) significantly impacts product performance. Additionally, the combination of high-density currents and increased joule heating in advanced technologies like FinFET (Fin Field-Effect Transistor) has sparked renewed interest in studying pulsed DC and pulsed AC EM, particularly for high-speed circuits. Three main challenges to pursue high frequency-based EM study are, stressing interconnect at 1) high frequency 2) high temperature, and 3) high current. As per our knowledge, this is the first work to report GHz frequency effect in EM failure. To achieve this, an on- die ring oscillator (ROSC) is used which can generate MHz to GHz on chip frequencies. For low frequency (kHz to MHz range) test, an off-chip phase locked loop (PLL) circuit is used. Both on-die, and off-die frequencies are inserted through same digital logic circuit to stress the metal interconnect. The other challenge is, to sustain the CMOS circuit functionalities, the ambient temperature cannot cross more than 120 ^{o}C, hence an on-die stable heater is required with a standoff distance from the active circuit to generate the accelerated heat locally to stress the metal interconnect.

To achieve high current during stress, an innovative test chip is designed with digital logic circuit and large sized current driver, also the metal interconnect is protected from parasitic capacitance effect during stress.

Fortunately, this work could overcome all the challenges and the novel test chips could generate the EM failure trend with respect to DC to GHz frequencies. Design details and tests results are described in chapter 3.

Other than current density, electromigration failure depends on the temperature. The equipment utilized for stressing products, such as tester cards and reference design PCB (printed circuit board), have a finite capacity for power delivery. An increased power demand during stress testing can strain these power delivery systems. This issue restricts the highest possible temperature that can be used for stress conditions. Also, no mechanism exists to perform non-uniform or spot heating that arise in practical settings.

To understand the non-uniform localized temperature effect on EM failure, a laser-based test is performed. To our knowledge, this is the first reported laser based electromigration failure result, which show EM failure depends on the laser location, as thermal migration has a key role to play when the stress temperature in non-uniform. The detailed laser-based EM failure work is explained in chapter 4.

1.3 Thesis Organization

This thesis is organized with following four chapters, chapter 2, chapter 3 and chapter 4 represent the work submitted to three journals.

Chapter 2 describes the in-depth survey of the several papers on electromigration and various aging phenomena, this literature survey is submitted as a review paper in a journal. The chapter begins with a brief overview of reliability failures in integrated circuits (ICs) and provides an in-depth discussion on electromigration (EM) failures in metal interconnects. For the latter, we begin by reviewing the fundamentals of electromigration. In addition to discussing the widely used Black's model and Blech's model for characterizing EM failures, we also summarize more advanced models by Kirchheim and Korhonen. These advanced models are particularly relevant

for modern high-speed IC applications, as they account for the opposing forces on EM during the on and off periods of pulsed inputs. We also cover techniques to mitigate the effects of EM and mention industry-based tools used to detect EM issues during the design phase.

Chapter 3 describes the design, fabrication and testing of novel test chips which are uniquely capable to generate pulsed DC and AC stress over a wide frequency range, from DC to 100 kHz to 1 GHz for detecting EM failure of an interconnect. The test chip is fabricated using Intel's 22FFL technology. Additionally, a thin film resistor (TFR) on-die heater is incorporated to provide stable and consistent thermal conditioning up to approximately 300 °C. The unique testing capability is described. The frequency-dependent EM mean time to failure (MTTF) trend is experimentally demonstrated. It is a collaborative work between Intel corporation and Iowa state university.

Chapter 4 describes very first non-uniform heat based electromigration data. The non - uniform heat is generated by using continuous wave-based laser on an EM test structure (metal interconnect) fabricated using Intel's 22FFL technology. The laser is focused on metal-via junction and on the metal strip. The EM failure mode signatures show dependency on the heating locations. The void generations captured by TEM (transmission electron microscopy) images confirm the EM failure locations. EM test structure, laser set up, physics behind testing, silicon data, TEM images are presented. It is a collaborative work between Intel corporation and Iowa state university.

1.4 References

[1] J. Lienig, "Electromigration and Its Impact on Physical Design in Future Technologies," ISPD, Mar. 24–27, 2013, pp. 33-40.

[2] J. Lienig et al., "Toward Security Closure in the Face of Reliability Effects," ICCAD Special Session Paper, ICCAD, Munich, Germany, Nov. 2021, pp. 1-9.

CHAPTER 2. ELECTROMIGRATION: A REVIEW, WITH OVERVIEW OF OTHER IC FAILURES

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2.1 Abstract

Electromigration (EM) is the transport of conductor metal atoms caused by the momentum transfer from the conducting electrons. As the integrated circuits (ICs) are shrinking in size, resulting in the continuous downsizing of interconnect cross-sections, the new challenges are encountered, particularly in the form of electromigration (EM) in circuit interconnections. It is widely recognized that the risks associated with electromigration due to the decreasing size of structures will become more pronounced in the future. Consequently, there has been a substantial surge in the adoption of electromigration-conscious design strategies over the past few years. To ensure the production of functional circuits in progressively smaller dimensions, a substantial boost in investment towards methodologies that enhance EM-related reliability is imperative. The important integrated circuit EM-affiliated failure mechanisms are reviewed in this paper. The fundamental physics behind the electromigration is discussed followed by the factors impacting electromigration. This review paper serves to showcase the importance of complex electromigration physics as the semiconductor industry is moving towards high-speed and shrinking-size applications. Also, it outlines the high frequency effects and various solution approaches and tools.

2.2 Introduction: Various IC Failures

The semiconductor industry has made great strides in recent times. On-chip integrated circuits are built using many discrete CMOS (complementary metal oxide semiconductor) devices that perform various functional operations. Today, an entire multicore processor can be built on a single piece of silicon. This massive downscaling has been possible due to miniaturization of the silicon MOS transistor in very large scare scale integration (VLSI). Any IC's lifetime is a function of both device and interconnect wear out.

With feature size reduction, fabricating CMOS devices with high perfection becomes very challenging. During and after manufacturing of the small devices, more defects are observed, making the devices more susceptible to various in-field failures. This causes device performance to degrade over time, even failing completely pre-maturely before its intended lifetime [1]. With shrinking device size, the device characteristics incur increased variability which leads to larger spreads in delay, leakage/power, and loss of robustness [2].

In this review paper we briefly overview the reliability failures in ICs and comprehensively discuss the electromigration (EM) failure in metal interconnects. For the latter, we start with reviewing electromigration fundamentals. Along with most used Black's model and Blech's model to characterize EM failures, we also summarize more advanced models of Kirchheim and Korhonen, which are relevant for today's high speed IC applications to capture opposing forces on EM during the on- versus the off-periods of pulsed inputs. We also mention the techniques to reduce EM effect, and the industry-based EM tools to detect EM issues during design phase. A handful recent review papers on electromigration [3], [4], [5]-[10] have shared useful information on EM fundamentals, EM physics, but they did not discuss other IC failures mechanisms along with above mentioned EM related topics in a single review paper.

With nano-sized transistors, keeping high performance under low power reliability becomes a significant obstacle to further CMOS scaling as technology nodes continue to shrink. As per constant-electric field scaling principles [11], the power-supply voltage of the MOS transistor is reduced with the continued scaling down of device dimensions to retain same level of heating. Yet although an individual transistor is consuming very little power per switching, when billions of them switching at very high speed, the overall power dissipation becomes a challenge.

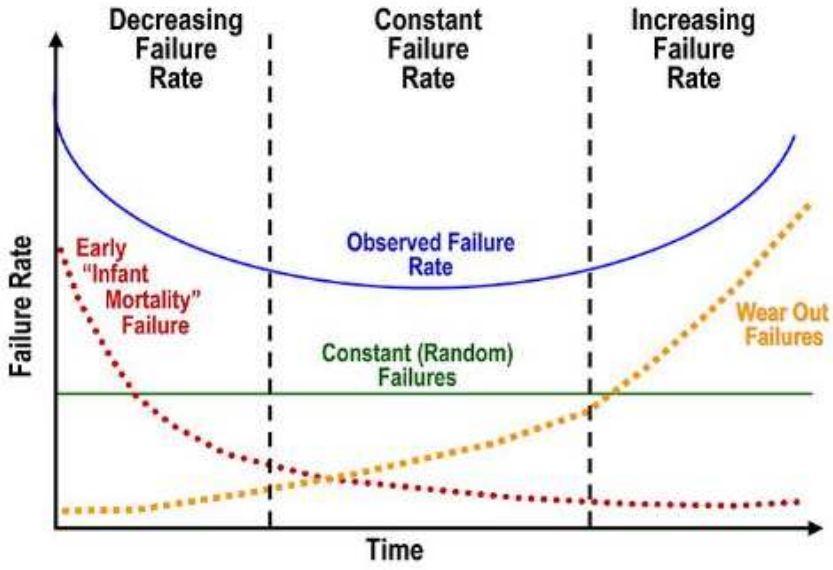


Figure 2.1. Classical bathtub failure rate curve observed in semiconductor industries [16].

Hot carriers' injection (HCI), bias temperature instability (BTI), and time dependent dielectric breakdown (TDDB) are the most prominent reliability mechanisms causing transistor aging [12], [13]. Electromigration (EM), stress migration (SM) and thermal migration (TM) are critical defect mechanisms causing metal interconnects failure [3]. Soft error rate (SER) is another distinctive defect mode for an IC under radiation environment [14]. Therefore, these mechanisms need to be studied thoroughly to obtain accurate overall reliability while designing robust circuits.

The failure rate of any integrated circuit (IC) during its lifetime is historically modeled by a “bathtub curve” [15], [16] shown in Fig. 2.1. The “bathtub” curve consists of 3 characteristic regions. The initial segment of the curve, characterized by a declining failure rate, is referred to as early failure or infant mortality failure, which is typically associated with manufacturing defects (e.g. patterning defects). Burn-In test, which is an accelerated stress-based screening, is used to filter out the ICs with congenital defects.

The central portion is known as the useful life period. In this phase, the ICs are shipped to customers, failure rate is largely constant, but certain random failures can occur due to environmental conditions (noise, radiation, current, temperature, etc.). The final segment of the curve represents wear-out failures, characterized by the highest failure rate due to acceleration of failure mechanisms.

2.2.1. Hot Carrier Injection (HCI)

In negative-channel metal oxide semiconductor (NMOS) devices, charge carriers are electrons whereas in positive-channel metal-oxide semiconductor (PMOS) devices, charge carriers are holes. As charge carriers move along the channel from the source to the drain in a device, the electric field causes carriers to gain kinetic energy and become “hot”, also creating secondary carriers through impact ionization [13], as shown in Fig. 2.2. Eventually, a few of these primary or secondary energetic carriers acquire enough energy to surpass the energy barrier between silicon (Si) and silicon dioxide (SiO_2) [17]. As a result, these high-energy carriers, known as hot carriers, are injected into the gate oxide layer. This injection leads to the accumulation of trapped charges at the interface between the silicon substrate and the gate dielectric, as well as within the bulk of the dielectric material. This phenomenon changes the device characteristics such as threshold voltage, transconductance, saturation current, and gradually the device degrades. Hot Carrier

injection (HCI) is directly associated with the channel length, the thickness of the oxide layer, and the power supply voltage of the device [18].

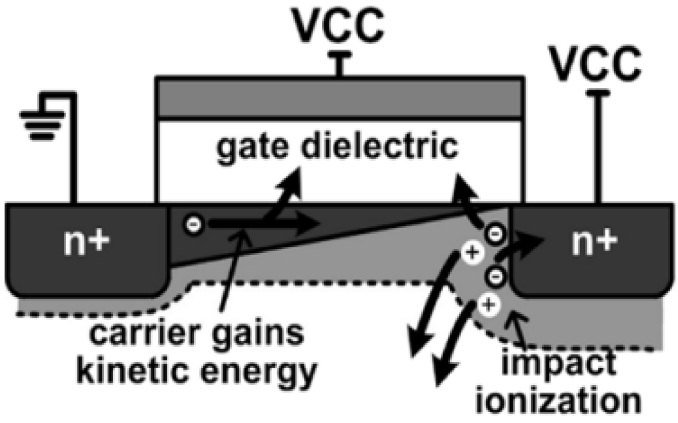


Figure 2.2. HCI mechanism in a semiconductor device (NMOS) [13].

2.2.2. Bias Temperature Instability (BTI)

The bias temperature instability in a transistor is characterized by a change in its threshold voltage (Vth) due to voltage stress. In PMOS transistors, the threshold voltage is associated with a negative gate bias, making negative bias temperature instability (NBTI) a more significant issue than positive bias temperature instability (PBTI). Conversely, for NMOS transistors, PBTI is of greater concern than NBTI.

PMOS transistor operating under negative gate bias, in the strong inversion region but with a zero or very low lateral electric field (VDS ≈ 0), holes from the PMOS transistor accumulate at the Si- SiO2 interface and eventually some of these charges get trapped in the oxide layer and/or the disruption of silicon-hydrogen (Si-H) bonds at the interface between the silicon and oxide leads to the creation of interface traps [13], [19], [20] shown in Fig. 2.3. The formation rate of these interface traps is hastened by elevated temperatures and the duration of the stress applied. The

presence of these traps results in an increase in the absolute value of the threshold voltage (Vth) for PMOS transistors. Upon removal of the stress, the PMOS device begins a "recovery" phase, during which the trapped holes begin to release, and/or the freed hydrogen species start to diffuse back toward the substrate-dielectric interface. This diffusion process allows for the annealing of the previously broken silicon-hydrogen (Si-H) bonds, which in turn reduces the absolute value of the threshold voltage. But if the shift in the threshold voltage surpasses a certain specified limit, then the device is considered to have failed [19], [20]. PBTI in NMOS devices was not found critical in silicon dioxide dielectrics but for high-κ gate stacks, PBTI became a reliability concern [21].

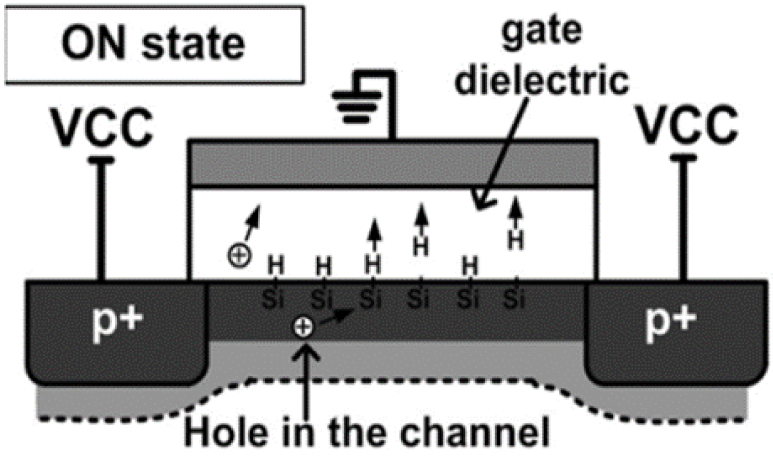


Figure 2.3. NBTI mechanism in a PMOS device [13].

2.2.3. Time Dependent Dielectric Breakdown (TDDB)

TDDB occurs when a device fails due to carrier tunneling through the gate oxide to substrate. Transistors under constant voltage stress, generate electron or hole injection into the gate oxide which form the defects, such as oxygen vacancies or traps (see Fig. 2.4). Over time, these trapped carriers combine to create a conductive pathway through the dielectric stack, ultimately

leading to the breakdown of the gate oxide. With the reduction of the gate dielectric thickness to the nanometer scale, a lower critical density of traps is sufficient to form a low-resistance robust conducting pathways allowing significant current to flow through the oxide leading overheating and irreversible damage to the dielectric layer [13], [18].

Through the introduction of high-κ dielectrics, TDDB effect is reduced, but it's still a reliability concern [22]. The most practiced test to study the TDDB behavior is "constant stress" [23], applied in the form of constant voltage lower than the breakdown voltage of the oxide, and leakage current of the transistor is monitored. The observed time to break down the oxide is called the time-to-failure for TDDB.

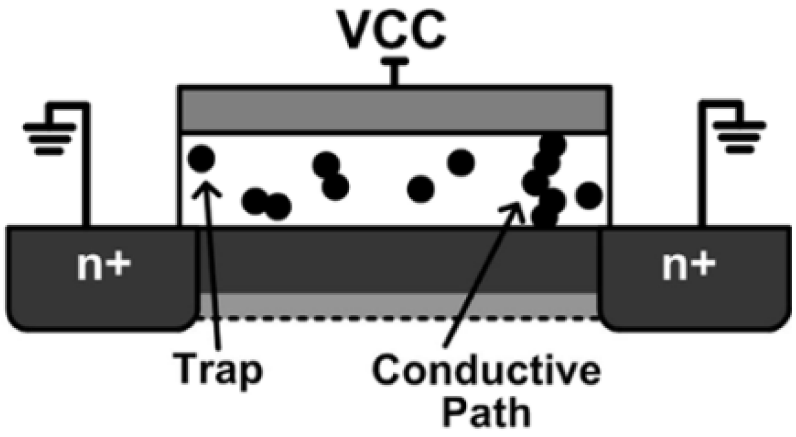
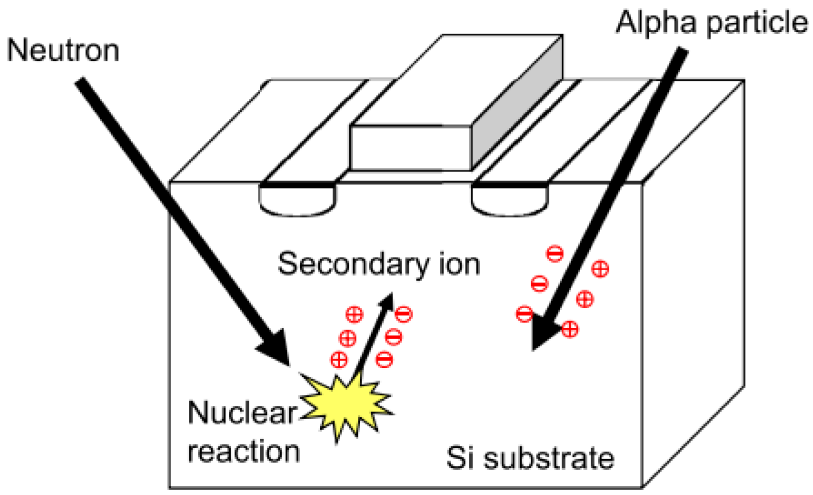


Figure 2.4. TDDB effect in devices [13].

2.2.4. Soft Error Rate (SER)

In sequential or memory elements, soft errors affect the state of the data (rather the parameter of a device). SER is caused by random radiation events occurring naturally in the terrestrial environment. When a particle of ionizing radiation hits the silicon substrate of a transistor, it generates pairs of electrons and holes. The movement of created electron-hole pairs through processes like diffusion and drift, results in the accumulation of electric charge at the drain

terminal of the transistor [24], [25]. The collected charge eventually induces a temporary disturbance at the drain node of the transistor causing a change in the data state, called soft error. A transient disturbance in a sequential circuit is referred to as a single event transient (SET), while a similar disturbance that occurs in a memory element and disrupts the stored information is known



as a single event upset (SEU). In a terrestrial environment, soft errors can occur due to alpha particles emitted from the packaging materials of electronic devices and due to neutrons, that originate from cosmic particles. Alpha particles, being a form of ionizing radiation, can directly create electron-hole pairs, as depicted in Fig. 2.5. Neutrons, in contrast, cause soft errors indirectly by interacting with the atomic nuclei of the materials in the transistor. This interaction is also illustrated in Fig. 2.5.

Figure 2.5. Neutron and alpha based SER mechanism [26].

The nuclear reaction initiated by the neutrons produces charged secondary particles such as protons, alpha particles, and heavy ions [26]. The likelihood of a circuit experiencing a soft error is influenced by several factors: the energy of the incoming particle, the precise location where the particle strikes, the geometry of the affected circuit element, and the overall design of

the circuit. The product of the power supply voltage and the capacitance of that node is defined as critical charge, Q_{crit}. SER can be prevented if Q_{crit} of the particle struck node is high [27]. Higher Q_{crit} is better to prevent the SER but it also means slower circuit and higher power dissipation. As the feature size of chips and the supply voltage are reduced, the critical charge (Q_{crit}) decreases. Thus, the significance of soft errors increases with the downsizing of the chip technology. Redundant circuits in a chip also help to avoid the SER effect.

Aside from the reliability mechanisms related to front-end failures of an IC, the back-end the back-end failure mechanisms such as electromigration as well as stress-migration and thermal-migration have impacts on the lifetime of metal interconnects, and thereby that of the IC itself.

2.3 Electromigration

In the recent scaled technology nodes, electromigration induced back-end-of-line (BEOL) connectivity failure is a matter of frequent concern. Electromigration is a failure mechanism dependent on current density, frequency, and temperature. With miniaturization of device sizes, the increment of device density is feasible, but it also causes high current density and high operating temperature of the ICs, whereas high speed poses high frequency of switching. These make electromigration become a challenging reliability issue for today's IC [28].

Digital and analog circuits operate under DC current or time varying current, creating power/heat on the device and the interconnect network, which can get very high. A proper operation of the semiconductor devices depends on the robust power distribution. When designing an interconnect/power grid, two crucial design factors are: resistive drop and EM reliability, which must be properly considered [29]. A resistive drop can assure that devices do not overheat while receiving enough voltage, whereas a strong EM reliability prevents void formation in vias and lines that would otherwise raise resistance at various nodes/interconnects of the power grid over the course of the product's lifetime. Various simulation and modeling technologies are available

for power grid design [30]. Due to its extremely high levels of redundancy and dynamic current redistribution, accurate EM measurement of an interconnect grid is not a simple operation.

Time varying currents with unidirectional pulses and bidirectional AC currents also flow through the interconnect nets and devices. Such currents are also becoming critical because of high-speed circuits usage and their rising root mean square (RMS) values [31]. A section of this paper discusses the time varying stress effects on EM.

2.3.1. EM Fundamentals

When electric field is applied, current flows through a metal interconnect, and two forces are exerted on its metal ions: The first is the electrostatic force F_{field} caused by the electric field, E, in the same direction of electric field, and the second force F_{wind} is generated by the momentum transfer between the conducting electrons and metal ions in the metal line shown in Fig. 2.6. The resulting force, F_{res} is [32]:

$$F_{res} = F_{field} + F_{wind} = e(Z_e - Z_p)E = eZ^* j\rho \quad (2.1)$$

where e is electric charge of ions, Z_p, Z_e are the valences for the wind and electrostatic force respectively. $Z^* = Z_p - Z_e$ is the effective charge number of the material, j is the current density, and ρ is the resistivity of the material. The force exerted by the electron wind is the primary force experienced by the atomic ions, leading to their migration toward the anode (positively biased). When the resulting force exceeds the activation energy (E_a) of metal interconnect, metal ions (Cu+) start to diffuse from cathode (negatively biased) to anode in the direction of F_{wind} (direction of electron motion) shown in Fig. 2.6. Over time, F_{wind} moves a significant number of interconnect material atoms from their original positions, creating voids at cathode and hillocks at anode in the metal interconnect, and eventually electrical failure [32], [33].

The resulting atomic flux, J, due to electromigration, [34] is defined as in (2.2), where F_{res} is the resulting EM force from (2.1), C_a is the concentration of diffusing atoms, D_a is atomic diffusivity, k_B is the Boltzmann constant and T is the absolute temperature:

$$J = \frac{C_a D_a}{k_B T} F_{res} = \frac{C_a D_a}{k_B T} eZ^* j\rho \tag{2.2}$$

If the material transport occurred uniformly across every part of the metal line, then the quantity of material being replenished would equal the amount being removed, leading to no net alteration in the metal line's density or thickness. However, the metal interconnects within a fabricated integrated circuit (IC) chip comprise numerous features that introduce non-uniformities. Some of the dominant reasons for inhomogeneous EM are i) varying cross section of the metal and as a result, varying current densities, ii) variability in the lattice properties, iii) preexisting impurities in the metal line, iv) temperature distribution variation, v) generated mechanical tension gradients, and vi) directional changes of current in the metal line [28].

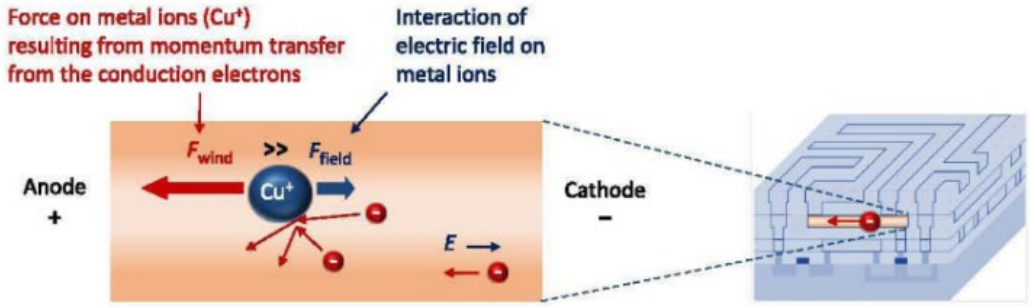


Figure 2.6. Two factors influence the metal ions (Cu) constituting the lattice of the interconnect material; EM is the result of the prevailing force, the transfer of momentum from electrons moving within the applied electric field E [33].

The presence of inhomogeneities leads to divergence in the diffusion process, which can ultimately cause the metal to deplete, forming voids, or to accumulate, leading to the creation of hillocks. Voids create open circuit and hillocks cause short circuit shown in Fig. 2.7. Whisker

formation is another crystalline, metallurgical phenomenon due to EM, causing growth of tiny, filiform hairs atop a metallic surface. Whiskers create short circuits and arcing in electronic circuits [28], [35].

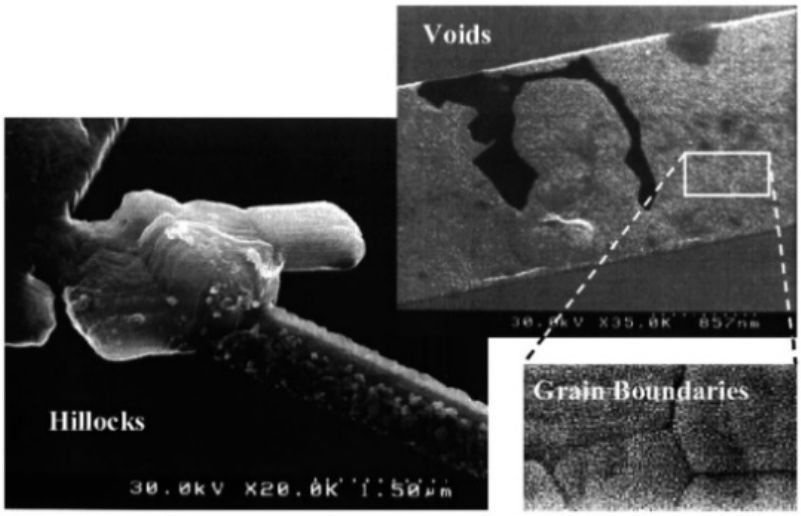


Figure 2.7. Hillock and void formations in metal interconnect due to EM (left, photography courtesy of G. H. Bernstein und R. Frankovic, University of Norte Dame) [35].

2.3.2. Grain and Surface Boundary Effects

The material selected for fabricating interconnects affects electromigration. The most critical characteristic of a conductive material that has a significant impact on electromigration is its activation energy, E_a. The activation energy is determined by the bond strength within the metal's crystal lattice structure [36]. The activation energy for the bulk diffusion (lattice diffusion) is higher than for grain-boundary diffusion and surface diffusion. Consequently, it is predominantly the grain boundaries that act as the pathways for diffusion in electromigration as shown in Fig. 2.8. Hence, the susceptibility to electromigration in the interconnect lattice is defined by the density and orientation of the grain boundaries [37]-[40].

The rate of atomic transport is significantly influenced by the grain size, which determines the extent of the grain boundary area in a metal line. The grain structure inside metal lines can differ from one location to another, a variation that originates from the metal deposition process.

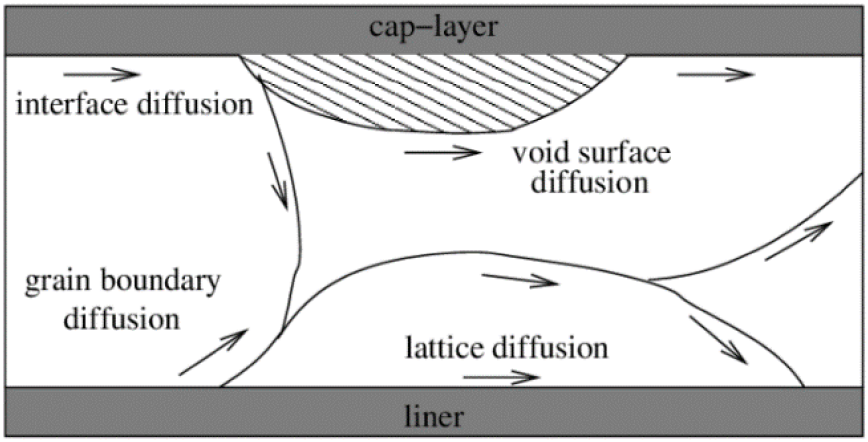


Figure 2.8. Movement of metal atoms via various diffusion paths [41].

A region with fine-grained structure provides a greater number of grain boundaries for atomic migration compared to a region with a coarse-grained structure. Therefore, an accumulation of atoms occurs when atomic migration is directed from a fine-grained region toward a coarser-grained region. Conversely, void formation occurs when atoms migrate from a coarse-grained region to a fine-grained region. The driving force behind electromigration is primarily perpendicular to the grain boundaries [28], [4].

Bamboo or near-bamboo type crystal lattices (shown in Fig. 2.9) possess fewer grain boundaries that are aligned with the direction of the current flow. The absence of continuous paths along grain boundaries for diffusion aids in reducing the transport of atoms along these boundaries [41], [42]. In these structures, EM damage tends to occur at the points where grain boundaries branch off or join. Such points are called “triple points” [28], [41].

By selecting a suitable barrier material for the metal, the activation energy for surface diffusion can be increased discouraging such diffusion. A barrier layer is a thin layer on metal interconnect and helps preventing metal from diffusing into the dielectric layer at high temperature. Therefore, a barrier layer must have a high stability and good adhesion to both metal and the dielectric layer. The widely used barrier layer for Cu is tantalum/tantalum nitride (Ta/TaN) [43].

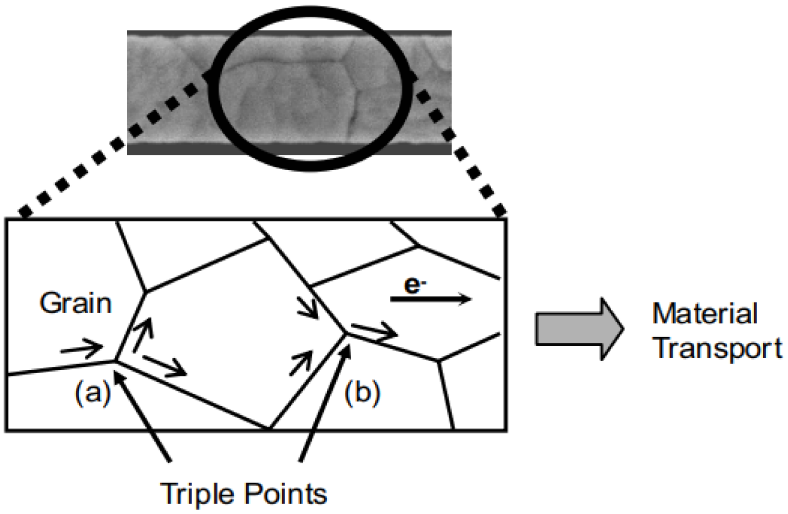


Figure 2.9. Paths of diffusion at triple junctions result in the formation of (a) voids (b) hillocks [40].

Inhibiting one diffusion mechanism, shifts the burden to other diffusion mechanisms creating alternative damage scenarios [44]. As an example, using copper as metal interconnect instead of aluminum, reduces grain-boundary diffusion, but it increases surface diffusion. By using suitable barrier layers, if surface diffusion is reduced, the grain-boundary diffusion takes over. Thus, the material layers used inside any ICs have a complex impact on EM failures [45], [46].

2.3.3. EM Flux Divergence Effects

When there is a disparity in diffusion rates between two materials, it leads to a divergence in atomic flux at their interface. When current flows from a material with higher diffusivity to one

with lower diffusivity, atom accumulation occurs at the interface between the two materials. Conversely, when the current flows from a material with lower diffusivity to one with higher diffusivity, voids tend to form at the interface [49]. EM induced degradation not only depends on grain structure's composition and size affecting diffusivity, but also by the direction in which the current flows. [28], [4], [41]. When electrons move from a via to a metal line, line depletion can occur due to the restricted flow of material caused by the cap and liner layers (Fig. 2.10 (a)). In contrast, when electron flows from a metal line to a via, a void develops resulting in via depletion. Since the metal line width is higher with respect to via width, the current density inside a via is higher, causing a higher EM damage inside a via (Fig. 2.10 (b)).

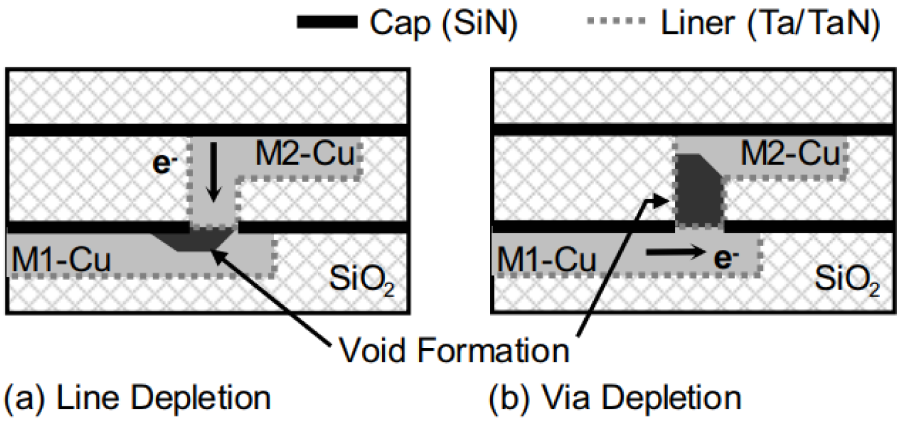


Figure 2.10. Depletion of lines and vias in metal line [41].

2.3.4. Current Distribution Effects

An uneven distribution of current exacerbates the effects of electromigration and the creation of empty spaces (similar as Kirkendall effect). The development of voids results in localized irregularities in current density, and the heightened resistance around the voids triggers additional localized temperature increases, further expediting void formation. Conversely, localized reductions in current density can result in the deposition of migrated atoms, leading to a

further decrease in current density, additional material deposition, and the formation of hillocks, which can potentially lead to short circuits [48].

A non-uniform distribution of current density is sometimes called current crowding. It typically happens in regions with reduced resistance, particularly in localized areas, or in regions where the electric field strength is concentrated, such as at the boundaries of layers [43]. For example, when a current passes through a contact barrier, such as the metal/TiN interface near both the cathode and anode ends, the current crowding occurs, and this is influenced not just by the resistances of the metal and TiN materials but also by the contact resistance at their interface. A higher contact resistance results in reduced current crowding [49].

2.4 Electromigration Quantifications

Diffusion models are used to characterize the divergence in the material flow, which enables to understand the expected locations of material accumulation and depletion and the expected location of initial damage.

2.4.1. Black's Model

Based on empirical studies, in 1960, J.R. Black [50]-[53] was first to predict the lifespan of a metal line when exposed to electromigration. It was considered that the mean time to failure, MTTF, is inversely proportional to the rate of the mass transport, R_m

$$MTTF \quad \propto \frac{1}{R_m} \tag{2.3}$$

and the rate of the mass transport is proportional to the momentum transfer between thermally activated ions and conducting electrons:

$$R_m \propto n_e \Delta p \, N_a \tag{2.4}$$

where n_e is the density of conducting electrons, Δp is the momentum transfer from the electrons to the metal atoms, and N_a is the density of thermally activated ions. Furthermore, assuming that

both the electron density as well as the momentum transfer are proportional to the current density, j,

$$n_e \propto j \ , \ \Delta p \propto j \tag{2.5}$$

and as activated ions follow an Arrhenius equation,

$$N_a \propto \exp\left(\frac{-E_a}{k_B T}\right) \tag{2.6}$$

the mean time to failure is modeled as:

$$\text{MTTF} = \frac{A}{j^2} e^{\frac{E_a}{k_B T}} \tag{2.7}$$

where A is a constant which comprises the material properties and the geometry of the interconnect, E_a is the activation energy, T is the absolute temperature, and k_B is Boltzmann's constant. It was found that not every experimental outcome followed (2.8); however, a fit could be achieved by introducing a variable exponent for the current density. Therefore, Black's equation was modified to [54]: and as activated ions follow an Arrhenius equation,

$$\text{MTTF} = \frac{A}{j^n} e^{\frac{E_a}{k_B T}} \tag{2.8}$$

where n is current density exponent, which can be experimentally determined. When $n = 1$, it represents a void growth phase where a pre-existing void is present, and for a void nucleation phase, n=2 where a void is created due to a critical stress [53]. To evaluate the time to failure of any metal interconnect, empirically validated Black's equation has been predominately used within the EM community.

Black's equation measures MTTF of any metal interconnect under pure DC stress, however this equation has limitation when the EM stress is either unidirectional pulse DC or bidirectional AC. Moreover, it does not take into consideration the transitions between various materials and the conditions at the boundary layers [55]. Furthermore, parameters A, n and E_a are technology

specific. A major limitation is that it is mainly intended for linear interconnects and might not be effectively applicable to complex network paths that include changes in direction. As a result, a few physics-based electromigration (EM) compact models have been recently introduced. These models explicitly describe void nucleation and evolution [56]-[58], which account for the time-dependent degradation of resistance in interconnect wires.

Physics-based electromigration modeling entails the use of a one-dimensional diffusion-drift equation. To solve this equation, it is necessary to have knowledge of the initial conditions, boundary conditions, transport parameters for the atomic species involved, the geometry of the structure, and the conditions under which the testing is conducted.

2.4.2. EM Induced Material Transport Equations

Electromigration is a kinetic process involving the net transport of metal atoms over macroscopic distances, driven by the interplay between two competing mechanisms: diffusion and migration. Since atomic migration occurs through a vacancy exchange mechanism, it is appropriate to describe material transport in terms of vacancy flux. The vacancy flux is in the opposite direction to the atomic transport [59], [60].

Diffusion is a non-equilibrium process that stops once the system achieves full thermodynamic equilibrium. The laws of diffusion are mathematical equations that describe how the rate of diffusion is related to the concentration gradient causing the mass transfer [60], [66].

Vacancies flow from high concentration regions to low concentration regions. According to Fick's first law, the flux of vacancies resulting from diffusion in any region of the metal line, $J_{v(D)}$ is directly proportional to the gradient of the vacancy concentration C_v, [60] as expressed by:

$$J_{v(D)} = -D_v \frac{\partial C_v}{\partial x} \tag{2.9}$$

where D_v is the vacancy diffusion coefficient or vacancy diffusivity. Diffusion coefficients are related to temperature by the Arrhenius law [63], [64],

$$D_v = D_0 exp\left(-\frac{E_a}{k_B T}\right) \tag{2.10}$$

where D_0 is the diffusion coefficient, and E_a represents the activation energy for electromigration.

The electromigration driving force F_{res}, as discussed in section 2.3.1, acts on vacancies and induces an additional velocity component, v_d for the diffusing species, aligned with the direction of the force. Utilizing the Nernst-Einstein relationship, the drift velocity is expressed as [63], [64]:

$$v_d = m \times E \equiv \left(D_v \frac{eZ^*}{k_B T}\right) \times (\rho j), \tag{2.11}$$

where m denotes the mobility and E the electric field, and the vacancy flux due to electromigration, $J_{v(EM)}$ is derived as follows [60]:

$$J_{v(EM)} = C_v v_d = C_v D_v \frac{eZ^* \rho j}{k_B T} \tag{2.12}$$

Under stress-assisted diffusion conditions, the migration process combines with diffusion. Vacancies tend to diffuse in one direction, while their migration under the influence of the electromigration force occurs in the opposite direction. Therefore, the net vacancy flux J_v in any part of the metal line due to the competition of Fickian diffusion and electromigration is given by [60],

$$J_v = J_{v(D)} + J_{v(EM)} = -D_v \frac{\partial C_v}{\partial x} + C_v D_v \frac{eZ^* \rho j}{k_B T} \tag{2.13}$$

Diffusion and electromigration fluxes lead to a redistribution of the vacancies in the metal line, causing divergence in vacancy flux, denoted as $\nabla . J_v$. Since vacancy concentration is not a

conserved quantity, the continuity equation for vacancy conservation is described by Fick's second law, which is given by [53], [64]:

$$\frac{\partial C_v}{\partial t} = -\nabla . J_v + G \tag{2.14}$$

where G is the source/sink term that represents the creation and annihilation of vacancies at specific sites within the metal line. These sites include grain boundaries, extended defects, and interfaces. Vacancies will accumulate if the divergence operator has a positive sign, and they will deplete if it has a negative sign.

Equations (2.13) and (2.14) are the fundamental continuum model equations that describe the behavior of vacancy concentration, accounting for the accumulation or depletion of vacancies due to diffusion and electromigration, as well as the effects of vacancy generation and annihilation, along an interconnect line.

Electromigration causes vacancies to drift toward the cathode end of an interconnect line, leading to a buildup of vacancies in that area. At the same time, this process results in a depletion of vacancies at the anode end. The lattice around a vacancy is slightly relaxed, so when vacancies accumulate, it results in a contraction of volume at the cathode. On the other hand, the depletion of vacancies causes the volume to expand at the anode end [28], [33], [64]. Due to the constraints imposed by the surrounding layers, such as the capping layer, barrier layer, and passivation in copper dual-damascene interconnects, the volumetric changes caused by vacancy accumulation and depletion cannot be fully accommodated. This leads to the development of a hydrostatic stress gradient within the metal line. At the cathode end, tensile stress is generated, while at the anode end, compressive stress develops, as shown in Fig. 2.11. This stress gradient acts as a back stress force that counteracts the forward atom migration driven by electromigration, ultimately reducing the overall diffusion flow [28], [33], [64].

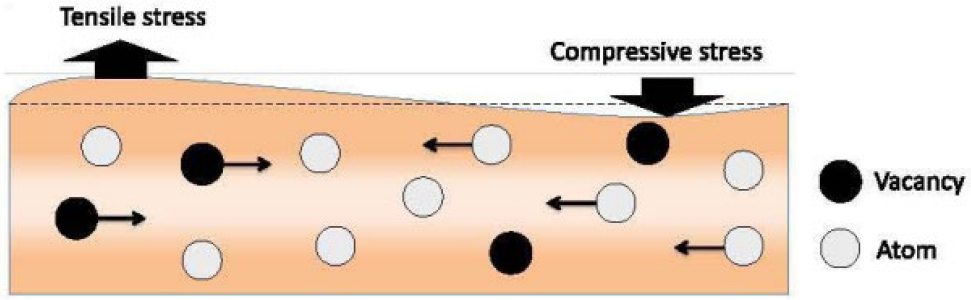


Figure 2.11. Stress migration is a byproduct of EM and involves the migration of vacancies. It occurs in response to a hydrostatic stress gradient and acts as a back stress opposing the effect of forward migration caused by EM [33].

2.4.3. Blech's Model

Blech [59]-[60] conducted an experiment involving the deposition of conductor islands onto a titanium nitride (TiN) film. These islands were subjected to high current density. Given that the conductor resistivity was significantly lower than that of the TiN layer, the high flow of current through the conductor stripe resulted in the movement of the stripe's ends.

Blech noted that, only the upstream end (relative to the electron flow) of the line exhibited movement with drift velocity mentioned in (2.11). Additionally, he observed that the movement of the upstream end ceased when the stripe reached a specific reduced length. Furthermore, he found that no drift was detectable below a certain threshold current density. These observations were formalized by taking into account the vacancy flux resulting from electromigration and the gradient of hydrostatic stress [34], [63] as captured by,

$$J_v = \frac{C_v D_v}{k_B T}\left(eZ^* j\rho - \Omega_a \frac{\partial \sigma}{\partial x}\right) \tag{2.15}$$

where J_v is the resulting vacancy flux, result of the applied electric field and gradient of hydrostatic stress, Ω_a is atomic volume, σ is hydrostatic stress, $\partial\sigma/\partial x$ is the gradient of the hydrostatic stress,

x is the distance along the metal line in the direction of the electron flow, with $x = 0$ at the cathode as shown in Fig. 2.12.

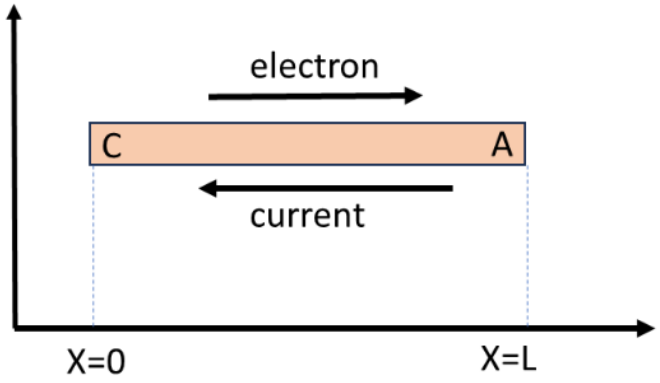


Figure 2.12. A two-terminal metal line with electron flow and current flow indicated by the arrow.

The equation suggests that a gradient in hydrostatic stress acts as a counterforce to electromigration. Therefore, electromigration comes to a halt when the opposing stress gradient, commonly referred to as "back stress," balances the electromigration driving force, resulting in a zero net flow, or $J_v = 0$. This equilibrium state is known as the "Blech Condition", defined by [61]:

$$\frac{\partial \sigma}{\partial x} = \frac{eZ^* j\rho}{\Omega_a} \tag{2.16}$$

Integrating (2.16) over the length of the interconnect, the stress expression becomes [65]:

$$\sigma(x) = \sigma_0 + \frac{eZ^* j\rho}{\Omega_a} x \tag{2.17}$$

where σ_0 is the stress at $x = 0$. The equation demonstrates that when the backflow flux, caused by stress gradients, is equal to the electromigration flux, the stress exhibits a linear variation along the length of the line. Considering that the conductor line can withstand a maximum stress of σ_{max}, a critical product of current density and interconnect length can be expressed as follows [59], [65]:

$$(jL)_{Blech} = \frac{\Omega_a(\sigma_{max} - \sigma_0)}{eZ^* \rho j} \tag{2.18}$$

This critical jL product is called “Blech product”. The electromigration halts when the product of j and L falls below the critical value shown by the right-hand side of (2.16). If EM stops before the critical compressive stress, σ_{crit} required for failure at the anode, the segment becomes immune to failure and hence ‘immortal’. The Blech effect [60] or the Blech immortality condition are common names for this phenomenon. The critical "Blech product" for contemporary copper interconnects falls within the range of 2000 to 10000 amperes per centimeter (A/cm) [66]-[68]. Based on (2.16), a critical line length can be determined for a given current density j, ensuring that shorter lines are not susceptible to electromigration-induced failure. This is commonly referred to as the "Blech Length", represented by:

$$L_{Blech} = \frac{\Omega_a(\sigma_{crit} - \sigma_0)}{eZ^*\rho j} \tag{2.19}$$

Likewise, with a specified line length L, the maximum allowable current density, below which electromigration failure does not occur, is given by:

$$j_{Blech} = \frac{\Omega_a(\sigma_{crit} - \sigma_0)}{eZ^*\rho L} \tag{2.20}$$

One significant implication of the Blech effect is that during electromigration assessments, the jL product must be substantially higher than the critical product $(jL)_{Blech}$ for the particular test structure. Failure to meet this criterion can lead to delayed failures in the test structure, thus providing a misleading sense of safety [60], [65]. Furthermore, it is important to recognize that residual stresses arising from the fabrication process reduce the amount of stress needed for electromigration to reach the maximum threshold that the line can withstand. As a result, this leads to reduced values for the Blech length and the maximum permissible current density outlined in (2.19) and (2.20), respectively [60], [65].

2.4.4. Kirchheim's Model

In the study by Blech, discussed in Section 2.4.3, it was discovered that electromigration induces back stresses, which can potentially delay device failure. The nature and origin of the back stress, however, were not clearly understood.

Kirchheim [53] was the first to incorporate the effect of transient back stress buildup in grain boundaries during electromigration which is caused by the transport and annihilation and production of vacancies. Self- consistent equations were derived describing vacancy electromigration through a grain boundary and the associated stress evolution.

Kirchheim proposed that when a vacancy, induced by electromigration, moves to the grain boundary, the neighboring atoms in the grain adjust or relax in response to the presence of the vacancy, which can result in a change in the volume of the grain by a fraction f, where f is the ratio of the volumes occupied by vacancies, Ω_v and lattice atoms, Ω_a ($f = \Omega_v/\Omega_a$); f is called as relaxation factor, $(0 < f < 1)$ [56]. This change in the grain volume causes hydrostatic stress gradient, to change by a factor of f. The gradient of the mechanical stress serves as an additional driving force in the total vacancy flux equation mentioned before in (2.13), modified vacancy flux equation is expressed as:

$$J_v = J_{v(D)} + J_{v(EM)} + J_{v(\sigma)} = -D_v \frac{\partial C_v}{\partial x} + C_v D_v \frac{eZ^* \rho j}{k_B T} - \frac{C_v D_v}{k_B T} f \Omega_a \frac{\partial \sigma}{\partial x} \qquad (2.21)$$

Where σ is the spherical part of the mechanical stress tensor. The first term on the right-hand side of (2.21) is due to the driving force of vacancy concentration gradient, the second term is due to the electric field, and the third term is due to the vacancy-induced stress gradient. Considering a vacancy sink/source as described in (2.14), the continuity equation can be rewritten as:

$$\frac{\partial C_v}{\partial t} = -\nabla . J_v + G = -\frac{\partial}{\partial x}\left[-D_v\left(\frac{\partial C_v}{\partial x} - \frac{eZ^* j\rho}{k_B T} C_v + \frac{f\Omega_a}{k_B T} C_v \frac{\partial \sigma}{\partial x}\right)\right] - \frac{C_v - C_{veq}}{\tau_s} \qquad (2.22)$$

The last term $(C_v - C_{veq})/\tau_s$ describes the annihilation or production of vacancies, in which τ_s is the relaxation time. The equilibrium vacancy concentration, C_{veq} in a grain boundary is defined as [53],

$$C_{veq} = C_{v0} exp\left[\frac{(1-f)\Omega_a \sigma}{k_B T}\right] \tag{2.23}$$

where C_{v0} is the equilibrium vacancy concentration, in the absence of stresses. A change in vacancy generation produces the volumetric strain in a grain which is expressed as [56]:

$$\frac{\Delta V}{V} = (1-f)\Omega_a \frac{\delta}{d} \Delta C_v \tag{2.24}$$

where $(1-f)\Omega_a$ is the volume change due to lattice relaxation, when a vacancy is considered as a substitutional atom, δ is the grain boundary thickness, d is the grain diameter, and ΔC_v is the generated vacancy concentration. The strain rate is given by [50]:

$$\frac{1}{V}\frac{\partial V}{\partial t} = (1-f)\Omega_a \frac{\delta}{d}\left(\frac{C_v - C_{veq}}{\tau_s}\right) \tag{2.25}$$

Applying Hooke's law $(\partial\sigma = B\, \partial V/V)$, where B is the effective elastic bulk modulus for the material that surrounds the interconnect, the stress rate evolution is given by [56]:

$$\frac{\partial \sigma}{\partial t} = B(1-f)\Omega_a \frac{\delta}{d}\left(\frac{C_v - C_{veq}}{\tau_s}\right) \tag{2.26}$$

By coupling the stress development equation (2.26) with the vacancy concentration dynamics equation (2.22) along the metal line, analytical solutions can be derived that relate the mechanical stress to the production/annihilation of vacancies at the grain boundary for several limiting cases. Additionally, Kirchheim identified three phases in the evolution of vacancy concentration and stress, which play a crucial role in understanding the electromigration phenomenon in 3D interconnects [60].

In summary, in Kirchheim's Model, $\sigma(x,t), J_v(x,t), C_v(x,t)$ are computed by solving trinity of (2.21), (2.22), (2.26), and from which the nucleation and failure times can be computed.

Void nucleation time and location: $(x_{nuc}, t_{nuc}) \coloneqq \arg\min_t \max_x \sigma(x,t) > \sigma_{critical}$, i.e., it finds earliest time for which exists a location where stress exceeds a critical value.

Void growth time and location (which can also be viewed as failure time and location): $(x_g, t_g) \coloneqq \arg\min_t \max_x V(x,t) > V_{critical}$, where $V(x,t)$ is the void volume at t and x. Ie, it finds the earliest time for which exists a location where void volume exceeds a critical value. (Need a relation to map σ, J_v, C_v to V to then compute t_g and x_g.)

Keeping in mind that B is determined by the elastic moduli and the dimensions of the refractory metal liner, the dielectric diffusion barrier, and the dielectric material, its magnitude may vary along the length of the interconnect, especially in the vicinity of the anode and cathode. It's crucial to recall that the elastic bulk moduli of low-κ dielectrics are considerably lower than that of SiO_2 (by roughly a factor of 10). Equation (2.26) demonstrates the relationship between stress buildup and the deviation of vacancy concentration from its equilibrium state, highlighting the significant impact of τ_s on stress development. It is essential to understand that this model accounts for different mechanisms of vacancy generation or annihilation, encompassing processes that take place within the grain boundary, at adjacent grain boundaries, or at dislocations located within the bulk of the grain. These mechanisms result in vacancy relaxation times, τ_s to be of smaller, median, or larger values. Equations (2.22) and (2.26) form a nonlinear system of differential equations which require numerical solutions. Nevertheless, Kirchheim derived analytical solutions for certain limiting cases, identifying three main stages in the evolution of vacancies and stress [53], [56].

The initial phase denotes a short duration with very low initial stress. As a result, the equilibrium vacancy concentration remains unchanged, and the vacancy concentration continues to evolve until it reaches a condition of quasi-steady state. This quasi-steady-state phase is prolonged, characterized by only slight variations in vacancy concentration, while stress levels

increase linearly with time. This phase persists until stress reaches a level that influences the equilibrium vacancy concentration. Subsequently, a nonlinear stress increase occurs over time, following approximately the equilibrium vacancy concentration's development. Kirchheim model [53], [56] describes the rate at which vacancies are transported within the material due to the passage of an electric current. This equation (2.26) provides a more comprehensive understanding of how hydrostatic stress impacts the diffusion of metal atoms in terms of vacancy production and relaxation. Furthermore, Kirchheim [53], [58] demonstrated that if the electromigration lifetime is governed by reaching a certain critical stress, the exponent of current density in Black's equation shifts from n = 1 at low stress levels (where the failure time is dictated by the quasi-steady-state period) to n = 2 at higher critical stress levels (where the time required to reach true steady-state conditions governs the lifetime).

2.4.5. Korhonen's Model

The equations in Kirchheim's work were limited to describing 1D finite lines that were blocked at both ends. In Kirchheim's model, the values of vacancy concentration and stress buildup due to electromigration were found to be identical across all sections of the line, due to the assumption of spherical stress. Furthermore, while the stress evolution equation effectively accounted for the impact of sink/source reactions, the main disadvantage of this approach consists in neglecting the direct contribution of the vacancy flux in the stress evolution.

Korhonen [57] proposed a slightly different model from Kirchheim's. He investigated the effect of the stress gradient caused by electromigration in a narrow interconnect line deposited on an oxidized silicon substrate and covered by a rigid passivation layer. The formulation of the electromigration driving forces in his model is based on atomic flux rather than vacancy flux. The key difference from Kirchheim's work is the consideration of changes in lattice sites per unit volume as the source of deformation, rather than changes in vacancy concentration. In Korhonen's

model, the material transport due to the passage of electric current along the line is assumed to be influenced solely by grain boundary diffusion [57],

$$D_a = \frac{\delta D_{gb}}{d} \tag{2.27}$$

where D_a and D_{gb} are the atomic bulk diffusivity and the atomic grain boundary diffusivity, respectively. In this manner, atoms are primarily deposited at the grain boundaries.

The flux of atoms increases due to the differences in both the chemical and electrical potentials between different regions of the interconnect line. For atomic diffusion the chemical potential function, μ is defined as $\mu = \mu_a - \mu_v$, where μ_a is the atomic chemical potential, μ_v is the vacancy chemical potential [57]. At thermal equilibrium of the vacancies ($\mu_v = 0$), the chemical potential function μ is given by [57], [60]:

$$\mu = \mu_0 - \Omega_a \sigma \tag{2.28}$$

μ_0 is the chemical potential in the stress-free state, and σ is the tensile stress acting across the grain boundary. Considering the impact of chemical potential gradient ($\nabla \mu$), electric potential due to electromigration, the atomic flux J_a is given by [57], [60]:

$$J_a = -\frac{C_a D_a}{k_B T}(\nabla \mu + eZ^* j\rho) = \frac{C_a D_a}{k_B T}\left(\Omega_a \frac{\partial \sigma}{\partial x} - eZ^* j\rho\right) \tag{2.29}$$

where C_a is the atomic concentration and D_a is the atomic diffusion coefficient, and the 2nd half of the equation follows from using (2.28).

In thermal equilibrium, the chemical potential remains constant throughout all grain boundaries, which implies that the deposition of atoms at the grain boundary is independent of its orientation. Additionally, by considering the impact of the rigid dielectric layer on the metallization line, the generation and annihilation of atoms at the grain boundaries lead to changes in the lattice

site concentration C_L per unit volume. These changes result in the development of a uniform mechanical stress, which can be described by Hooke's law as follows [57]:

$$\frac{\partial C_L}{C_L} = -\frac{\partial \sigma}{B} \Rightarrow G \equiv \frac{\partial C_L}{\partial t} = -\frac{C_L}{B}\frac{\partial \sigma}{\partial t} \tag{2.30}$$

Since the lattice site occupied by an atom or a vacancy is assumed to have the same volume [57], [60], the constitutive equation relating stress and lattice site concentration leads to the reformulation of the vacancy continuity equation (equation (2.14)) as follows:

$$\frac{\partial C_v}{\partial t} = -\nabla . J_v + G = -\frac{\partial}{\partial x}\left(\frac{C_v D_v}{k_B T}(\nabla \mu + eZ^* j\rho)\right) - \frac{C_L}{B}\frac{\partial \sigma}{\partial t}, \tag{2.31}$$

where it is assumed that $J_a = J_v$. Assuming that vacancy concentration is in thermal equilibrium with the stress inside the grain, then

$$C_v = C_{veq} = C_{v0} exp\left(\frac{\Omega_a \sigma}{k_B T}\right) \Rightarrow \ln C_v = \ln C_{v_0} + \frac{\Omega_a \sigma}{k_B T} \Rightarrow \frac{1}{C_v}\frac{\partial C_v}{\partial t} = \frac{\Omega_a}{k_B T}\frac{\partial \sigma}{\partial t} \Rightarrow \frac{\partial C_v}{\partial t} = \frac{C_v \Omega_a}{k_B T}\frac{\partial \sigma}{\partial t} \tag{2.32}$$

Substituting $\frac{\partial C_v}{\partial t}$ from (2.32) and μ from (2.28), (2.31) becomes

$$\frac{\partial \sigma}{\partial t}\left(\frac{C_L}{B} + \frac{C_v \Omega_a}{k_B T}\right) = \frac{\partial}{\partial x}\left[\frac{C_v D_v}{k_B T}\left(\Omega_a \frac{\partial \sigma}{\partial x} - eZ^* \rho j\right)\right] \tag{2.33}$$

Dividing both sides by $\frac{C_L}{B}$ we get:

$$\frac{\partial \sigma}{\partial t}\left(1 + \frac{C_v \Omega_a B}{C_L k_B T}\right) = \frac{\partial}{\partial x}\left[\frac{C_v D_v B}{k_B T C_L}\left(\Omega_a \frac{\partial \sigma}{\partial x} - eZ^* \rho j\right)\right].$$

Including the assumption that only a very small number of vacancies is required to restore vacancy equilibrium and to generate stress, such that $\frac{C_v \Omega_a B}{C_L k_B T} \ll 1$, the first term in the brackets on the left-hand side of equation (2.33) becomes negligible. Furthermore, recognizing that $C_L = C_v = 1/\Omega$ and $D_a = C_v D_v / C_L$, the expression for the stress evolution along a metal line induced by electromigration is given by [57], [60]:

$$\frac{\partial \sigma}{\partial t} = \frac{\partial}{\partial x}\left[\frac{D_a B}{k_B T}\left(\Omega_a \frac{\partial \sigma}{\partial x} - eZ^* \rho j\right)\right] \tag{2.34}$$

Korhonen's equation provides a comprehensive description of how hydrostatic stress evolves in confined metal wires when material flux is obstructed at the barrier terminals, such as vias. This equation is applicable to both a single wire in a one-dimensional scenario and multi-segment wires in two-dimensional cases. The advantage of this model is that a closed equation was obtained for the stress evolution due to electromigration. However, important disadvantages are that vacancy induced relaxation effects were not taken into account and vacancy equilibrium was assumed.

In summary, in Korhonen's Model, $\sigma(x,t), J_a(x,t) = J_v(x,t), C_v(x,t)$ are computed by solving trinity of (2.29), (2.32), (2.34), and from which the nucleation and failure times can be computed.

Void nucleation time and location: $(x_{nuc}, t_{nuc}) \coloneqq \arg\min_t \max_x \sigma(x,t) > \sigma_{critical}$, i.e., it finds earliest time for which exists a location where stress exceeds a critical value.

Void growth time and location (which can also be viewed as failure time and location): $(x_g, t_g) \coloneqq \arg\min_t \max_x V(x,t) > V_{critical}$, where $V(x,t)$ is the void volume at t and x. I.e., it finds the earliest time for which exists a location where void volume exceeds a critical value. (Need a relation to map σ, J_v, C_v to V to then compute t_g and x_g.)

Figure 2.13 depicts the progression of stress over time for a single wire as described by Korhonen's equation [57], [64], [70]. The system achieves a steady state when the backward flux of vacancies balances the flux induced by the current, resulting in a uniform linear distribution of stress throughout the wire. In Fig. 2.13(a), the development of stress along the wire is shown, with the left end symbolizing the cathode node and the right end the anode node.

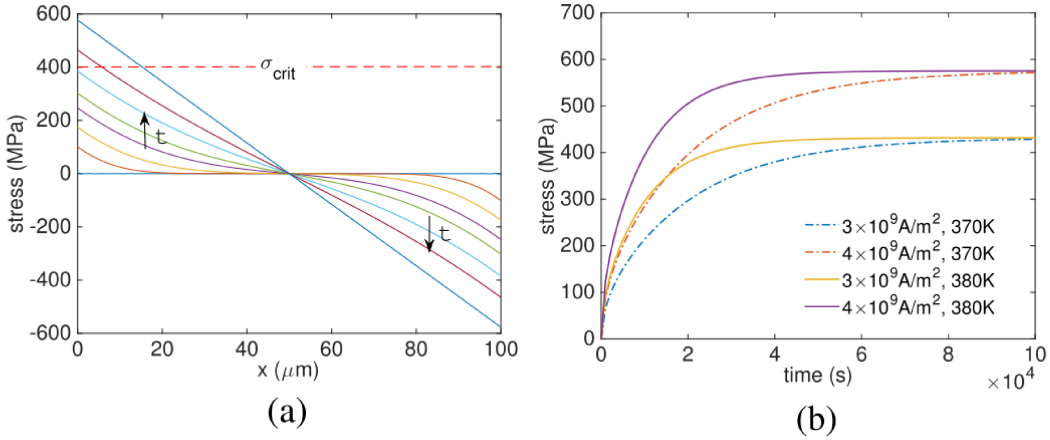


Figure 2.13. Development of hydrostatic stress within the wire, (a) at cathode, (b) over time when subjected to varying current densities and temperatures, assuming no initial stress [70].

This characteristic pattern of hydrostatic stress development is what one would expect under the influence of direct current (DC). Fig. 2.13(b) presents the development of hydrostatic stress at the cathode end of a metal wire, where tensile stress is at its highest, under varying DC current densities and temperatures, demonstrating that both current density and temperature influence the rate at which stress develops.

For Korhonen's equation, [57], [64], [70] if we consider a simple line wire of length L as shown in Fig. 2.12 at the two blocked ends located at $x = 0$; $x = L$, with initial condition:

$$J_v(0,t) = J_v(L,t) = 0$$

$$\sigma(x,0) = \sigma_T \tag{2.35}$$

where σ_T is the thermal stress developed in the metal line while cooling from the zero-stress temperature to the operating temperature. Then the hydrostatic stress value can be analytically solved as follows [64]:

$$\sigma = \sigma_T + \frac{eZ^* j\rho L}{\Omega} \times \left[\frac{1}{2} - \frac{x}{L} - 4\sum_{n=0}^{\infty} \frac{cos\left(\frac{(2n+1)\pi x}{L}\right)}{(2n+1)^2\pi^2} e^{-k\frac{(2n+1)^2\pi^2}{L^2}t}\right] \tag{2.36}$$

Korhonen-defined EM failure process consists of two important phases: the void nucleation phase and void growth phase.

2.4.5.1. Void Nucleation Phase

In this phase, there is an absence of initial voids. At the cathode end of the line, where x =0, the tensile stress begins to rise as time progresses When the tensile stress reaches the critical stress σ_{crit} the void nucleates. To determine the nucleation time t_{nuc}, the last term of (2.36) which is assumed to be dominant term needs to be solved [58], [64], [71]:

$$t_{nuc} = \frac{L^2 k_B T}{2D_a B\Omega} \ln\left[\frac{\frac{eZ^*\rho jL}{2\Omega}}{\sigma_T + \frac{eZ^*\rho jL}{2\Omega} - \sigma_{crit}}\right] \tag{2.37}$$

During this phase, the resistance of the metal line remains unchanged.

2.4.5.2. Void Growth Phase

The resistance of the line stays relatively stable even after the void has nucleated until the void undergoes growth and attains a critical size sufficient to obstruct the wire's cross-sectional area [72]. The phase of void growth can also be analyzed using Korhonen's equation, with a different set of boundary conditions. Since the drift velocity of the void edge relates to atomic flux as in (2.9), the void growth time, t_g required for the void to grow to a critical size, ΔL_{crit} can be derived as [64], [73],

$$t_g = \frac{\Delta L_{crit} k_B T}{D_a eZ^* \rho j} \tag{2.38}$$

It is seen that in void growth phase, the exponent of j is 1. When the void expands to a critical size, there is a sudden increase in resistance. After reaching this point, the resistance

continues to rise gradually due to the current being shunted by the liner barriers [74], [75]. During this phase, the change in metal resistance (ΔR) can be roughly estimated as follows [63], [73]:

$$\Delta R = \frac{D_a}{k_B T}\, eZ^* \rho_{Cu} j \left[\frac{\rho_{Ta}}{h_{Ta}(2h + w)} - \frac{\rho_{Cu}}{hw}\right] \tag{2.39}$$

Here, ρ_{Ta} and ρ_{Cu} are the resistivities of the barrier material (Ta/TaN) and Cu respectively, w is the metal line width, h is the metal line thickness, and h_{Ta} is the barrier layer thickness.

2.4.6. EM Void Induced Effects

2.4.6.1. Void Growth Saturation in Long Line

The process of void growth and its effect on wire resistance is a multifaceted phenomenon that encompasses several failure mechanisms. While void nucleation is a prerequisite for alterations in wire resistance, it is not solely sufficient, as void growth can cease or saturate before the void volume reaches a critical size, V_{max} where it significantly alters wire resistance. Throughout the void growth process, the stress gradient induces a backflow atomic drift velocity, v_b, so the total drift velocity, v_t is given by [64], [76]:

$$v_t = v_d - v_b = \left(eZ^* \rho j - \frac{\Delta\sigma\Omega}{L}\right)\frac{D_a}{k_B T} \tag{2.40}$$

where $\Delta\sigma$ is the back-flow stress and L is the wire length. When the stress gradient generated across metal line balances the EM driving force (i.e. $v_t = 0$), metal atom depletion stops. Korhonen et al. derived the maximum void volume in the one-dimensional metal line, V_{max} [63] as:

$$V_{max} = \frac{\sigma_{in} L}{B} + \frac{eZ^* \rho j L^2}{2\Omega B} \tag{2.41}$$

where σ_{in} is the initial thermal stress. It should be noted that V_{max} varies from line to line and relies on the size, and location of the void. Even when surpassing the critical product jL of Blech model, if V_{max} is not reached, the metal line remains immortal.

2.4.6.2. Void Growth Saturation in Short Line

At void growth region, the resistance change is measured as ΔR (2.39). In short lines, a steady state can be achieved before the change in resistance, ΔR_{max}, reaches a level that is considered unacceptable. As a result, at void growth saturation, there is a higher threshold $(\mathrm{jL})_{\mathrm{sat}} \geq (\mathrm{jL})_{\mathrm{Blech}}$ below which immortality can be attained. This observation is captured by the equation below [77]-[79]:

$$(jL)_{sat} \leq \frac{\frac{\rho_{cu}}{A_{cu}}}{\frac{\rho_{Ta}}{A_{Ta}}} \frac{\Delta R_{max}}{R_0} \frac{2\Omega B}{eZ^*\rho} \tag{2.42}$$

where R_0 is the initial resistance and ρ_{cu}/A_{cu}, ρ_{Ta}/A_{Ta} are the resistivity to cross-sectional area ratios of the metal (Cu) and its liner (Ta), respectively, and B is the bulk modulus.

2.4.6.3. Void Induced Damage

Electromigration failure resulting from void-induced damage is statistically correlated with the direction of electron flow. Consequently, two types of EM failure are observed: early failure and late failure of the wire [80]. Early failures typically occur in a via-above structure, as depicted in Fig. 2.10(a), where a void is created in a via-above line (also known as slit-voids) and reaches a critical size [64], [81], equivalent to the via's diameter. At this point, the via becomes obstructed by the void, interrupting electronic connection to the upper layer. Late failure typically manifests in a via-below structure, illustrated in Fig. 2.10(b), where a void forms in a via-below line (also known as trench voids) and reaches a critical size. Despite this, current can still traverse through the barrier layer (typically fabricated with Ta, which has a much higher resistivity than Cu), leading to a gradual increase in resistance over time. However, it is statistically possible for early failure to occur in a via-below structure and late failure in a via-above structure. Although void growth can occur in these positions, the likelihood is minimal.

A noticeable disparity exists in the reliability when comparing configurations with vias positioned above and below [82] (Fig. 2.10). In the configuration where vias are located above, the dielectric diffusion barrier does not offer a route for the shunting of current around a void.

Consequently, even a void with a very small volume can lead to failure. The value of $(jL)_{sat}$ is thereby lower for segments with vias positioned above compared to those with vias situated below [79]. The experimentally determined values of $(jL)_{sat}$, are as follows: 2100 A-cm [83] and 1500 A-cm [84] for Cu/SiO_2 for via-above segments, 3700 A-cm for Cu/SiO_2 via-below segments [85], and 375 A-cm for Cu/low-κ via-above segments [86].

2.5 Other Stress Effects on EM

Thermal migration, stress migration, and chemical diffusion are three other forms of diffusion in metallic interconnect structures that can significantly impact the back-end reliability of interconnects. Both thermal and stress migration have direct interactions with electromigration, making them important considerations for integrated circuit (IC) designers.

2.5.1. Thermal Migration (TM)

Thermal migration, also known as thermomigration, is a phenomenon that occurs due to the presence of temperature gradients within a material. In metal lines, elevated temperatures accelerate the movement of atoms. Because of their temperature-dependent activation, atoms in hotter regions are more likely to displace compared to those in colder regions (Fig. 2.14). As a result, a larger number of atoms move from areas of higher temperature to areas of lower temperature, resulting in a net mass diffusion in the direction of the negative temperature gradient [33].

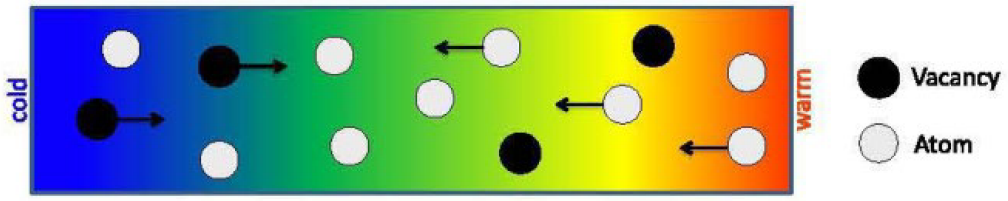


Figure 2.14. Thermal migration (TM) involves the movement of atoms and vacancies, leading to mass transport from one localized region to another, similar to EM, but TM is driven by a thermal gradient, as opposed to an electrical potential gradient in the case of EM [33].

The main reasons for temperature gradients in metal wires are following [28]:

a) High current in the metal line causes Joule heating.

b) Adjacent devices such as high-speed transistors heat up metal lines connected with it.

c) When any metal line is connected with heat sink, the heat gets dissipated at that end and it becomes cooler.

Due to initial current density, atom migration initiates, and voids commence growing, gradually deteriorating the cross-sectional integrity of the electromigration affected area. This, in turn, leads to an escalation in the local current density, resulting in increased local temperatures due to Joule heating. Consequently, this positive feedback loop accelerates atom diffusion, making void growth more pronounced. Therefore, despite being driven by a thermal gradient rather than an electrical potential gradient, thermal migration (TM) directly affects and influences electromigration (EM).

2.5.2. Stress Migration (SM)

Stress migration is the result of mechanical stresses induced in the metal interconnect lines, there are various reasons behind mechanical stress mentioned below [28]:

a) High temperatures (about 500 °C) are used to deposit the metal [87]. Mechanical tension arises when the temperature is lowered to ambient levels due to the different coefficients of thermal expansion between the metal and the insulator.

b) The uneven growth of layers that can occur during the metal deposition process contributes to mechanical stress within the metallization. According to [87], this issue is considered more significant than the effect caused by differing thermal expansion coefficients, and the phenomenon can be evidenced through measurements of wafer curvature [87], [88].

c) Metal lattices typically have vacancies, which means that some of the atomic locations are vacant. Vacancies take up less space than atoms at the same places, despite being aligned with the lattice grid. As a result, a crystal with vacancies has a lower volume than a crystal with the same structure but with atoms. This allows the lattice with vacancies to relax, which in turn causes a local decrease in material volume and a reduction in compressive stress [28]. When EM induces atom depletion at cathode, it develops tensile stress, and accumulation of atoms develops compressive stress at anode. Overall, a stress gradient is generated.

The processes of Electromigration (EM), Thermomigration (TM), and Stress Migration (SM) are intricately interconnected because their influences are interrelated, and they collectively impact the resulting changes in migration.

To illustrate, the increase in current density elevates temperature due to Joule heating, and alterations in temperature subsequently affect mechanical stress due to variations in the expansion coefficient. The high self-heat in FinFET and missing heat dissipation path to the bulk increases the local temperature in the metal lines, which enhances the EM failure.

2.5.3. Frequency Effects on EM

Typically, EM failure is evaluated through DC signal testing. However, in real-world scenarios, ICs are powered by either unidirectional pulsed DC or bidirectional AC signals with various duty cycles, and not just continuous DC signals.

Numerous research groups have conducted investigations into the frequency dependency of electromigration lifetime under pulsed DC stress.

The results, as documented in [89]-[98], have consistently demonstrated that, on average, the lifetime is roughly double than observed under continuous DC stress for a 50% duty cycle.

The Black equation, as presented in (4) is a reliable method for accurately assessing the Mean Time to Failure (MTTF) of any metal interconnect when subjected to pure DC stress.

In the case of pulsed DC-based stress, EM failure is influenced by the frequency at which the interconnect is subjected to stress. Under the presence of Joule heating, in low-frequency conditions, the temperature during the "on" period is higher compared to the temperature during the "off" period. This elevated temperature in “on” period enhances the forward migration, but almost no effective recovery is observed during “off” period due to lower temperature. In high frequency case, “on” and “off” period does not have significant temperature difference, hence recovery during “off” period plays an important role and improves the EM failure time [90], [97].

When the current stress is bidirectional AC, the direction of electromigration (EM) diffusion also reverses during the negative current pulse. Consequently, the EM-induced damage that occurs during the positive current pulse is mitigated or "healed" during the negative current pulse due to the backward migration of atoms. This phenomenon is referred to as "self-healing". The extent of this healing process depends on the duty factor of the positive and negative current pulses [99].

When interconnects are subjected to unidirectional pulsed DC stress, which alternates between "on" and "off" periods, the stress accumulates at the blocking boundary during the "on" phase, while it begins to relax during the "off" phase due to vacancy relaxation. Consequently, the failure of interconnects under electromigration conditions depend on the duty cycle factor of the pulsed DC signal, denoted as r. In such cases, Black's equation is modified as described in [90] to account for these variations and to predict the mean time to failure under pulsed DC stress more accurately:

$$MTTF_{PDC} = \frac{A}{j^n r^m} e^{\frac{E_a}{k_B T}} \tag{2.43}$$

When the current density exponent n is equal to 1, it signifies a failure, limited by void growth. On the other hand, when n is equal to 2, it represents a failure that is limited by void nucleation. If EM failure depends on the frequency of the signal, the constant A will also become frequency-dependent, as this term includes factors related to the void nucleation mechanism [90], [100].

In this context, when m equals to 1, it signifies that material migration exclusively occurs during the "on" period of the current pulse, with no recovery taking place during the "off" period. This model is commonly referred to as the "on-time" model. In cases where m is significantly greater than 1, it indicates that EM recovery occurs during the "off" period of the current pulse due to vacancy relaxation. When m equals to n, it is referred to as the "average current density model". In this scenario, the control over the duty factor response is governed by the time-average of the current [90].

For bidirectional AC signal, $MTTF_{AC}$ (mean time to failure) can be estimated by the following modified Black's equation [99]:

$$MTTF_{AC} = \frac{A}{(rj^{+} - \gamma(1-r)j^{-})^n} e^{\frac{E_a}{k_B T}} \tag{2.45}$$

where r is the duty factor corresponding to the relative duration of positive and negative pulse width of the bidirectional AC current signal, j^+, j^- are current density in positive, negative pulse width of the signal respectively, and γ is called as self-healing coefficient and is calculated as follows [99]:

$$\gamma = \frac{\frac{rj^+}{j_{dc}} - \frac{MTTF_{DC}}{MTTF_{AC}}}{\frac{(1-r)j^-}{j_{dc}}} \tag{2.46}$$

It was reported in [89], when frequency is high enough (f>1 MHz), the EM damage healing factor $\gamma \approx 1$, there is no EM failure is found under pure AC stress. This indicates that at extremely high-frequency AC stress, electromigration caused solely by AC stress is unlikely to pose a significant reliability issue. This phenomenon is significant because it permits the design of metal lines carrying AC signals to be more aggressive, potentially enhancing circuit density and speed by reducing parasitic capacitance.

2.6. EM Reduction Methodology

2.6.1. Reservoir Effects

Numerous studies have indicated that the electromigration-impacted lifespan of multi-level interconnects is increased by the existence of a “reservoir” around the contacts [101]-[103]. Expanded overlaps in metal-via layers augment the volume of interconnect material at critical locations where electromigration failure commonly occurs: beneath, above, and within the via. Reservoirs refer to metallic segments that do not conduct current efficiently or at all, rather serve as a source of atoms to replenish the region near the blocking boundary, where atoms migrate away due to electrical current. The function of a reservoir as a sink or a source is determined by the direction of the electrical current flow as shown in Fig. 2.15.

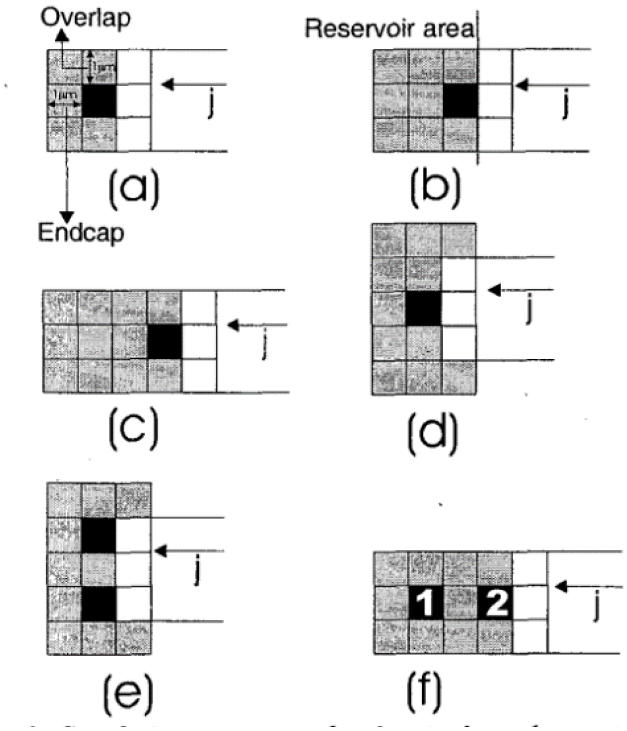


Figure 2.15. Metal-Via structures with single and two via contacts while reservoir area and overlap are varying. The reservoir is placed upstream with respect to the electron flow [103].

Reservoirs functioning as material sources typically extend lifespans, while reservoirs serving as predominant sinks for migrated interconnect material can diminish lifespan. The experimental data from the literature demonstrates that as the reservoir area and the number of contacts increase, the EM lifetime also increases. It is advisable to increase the reservoir in the perpendicular to the current direction rather than parallel to the current direction.

2.6.2. Double/Multiple Vias

Vias require special attention because the current-carrying capacity, or ampacity, of a tungsten via is typically less than that of a metal wire with the same width. Moreover, the migration velocities within the via material, the diffusion barrier, and the metal wire are different. As a result, vias are critical points for the nucleation of voids and are prone to electromigration failure. To

mitigate this increased risk and address common manufacturing and yield issues, the use of double or multiple vias is a standard practice. The arrangement of the via array is crucial: multiple vias need to be positioned in a way that ensures the current flow, and consequently the electromigration degradation, is distributed as uniformly as possible among the parallel vias [28], [4].

2.7. EM Tools For Physical Design Flow

The continuous shrinking of circuit feature sizes has made electromigration in integrated circuits a more severe problem. Manual analysis of current density in complex circuits is tedious and prone to errors, emphasizing the need for automated methods for current-based routing, verification, and post-routing layout adjustments [28], [4], [41], [104]. The most efficient way to limit EM prone failure is to run an EM verification tool which is based on current density check. The objective of current-density verification is to confirm that the maximum current densities within the metallization stay within the permissible limits for the designated operating temperature of the chip, applicable to both analog and digital circuits shown in Fig. 2.16.

Modern layout tools, such as Synopsys IC Compiler and Cadence Encounter, now include typical features like "Sign-off DRC w/ EM rules" and "Sign-off Spice Simulation" with current density verification [28], [4], [41], [104].

Initially, a static verification of the current density at net terminals is performed to ensure that the metallization of these terminals is capable of handling the designated current levels. Nets that are not critical are not subjected to further checks. The criticality of a net is assessed by adding up the worst-case current values for each terminal. If the sum is below the maximum permissible current for the minimum sized and most susceptible to electromigration metallization layer, then the net is not considered for additional analysis [41], [104].

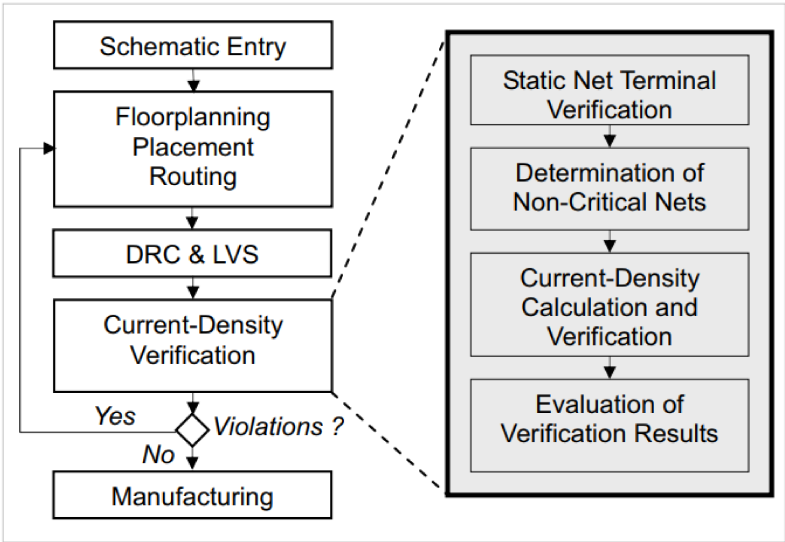


Figure 2.16. EM failure check via Current density verification flow [41].

Digital circuits contain a large number of nets. Typically, power nets have consistent current directions and carry relatively steady currents. In contrast, clock and signal nets carry alternating currents, which tend to have less impact on the lifespan of wires compared to direct currents. This is because alternating currents can induce self-healing, reducing the overall stress and wear on the wires [90], [98]. In digital design, the flow consists of a sequence of synthesis steps that utilize the geometrical information of the circuit. This information aids the current density tool in assessing the risk of electromigration.

A variety of systems for electromigration analysis have been developed to verify digital designs, as documented in [105]-[107]. [105] introduced a computer-aided design (CAD) system for electromigration analysis that examines current density in relatively simple layout patterns of CMOS circuits. This approach breaks down the layout into fundamental shapes, which are then represented as RC networks. This allows for individual simulations of each component. Simplex Solutions [106], released "Thunder & Lightning," a commercial toolkit aimed at analyzing

electromigration in power and ground networks, as well as in digital signal nets. OEA International Inc [107], offers "P-Plan," and Cadence Inc [108], provides "ElectronStorm." Both are commercial-grade verification tools that assess electromigration and Joule heating in power and signal nets of digital circuits.

Until recently, incorporating the impact of current densities into the physical design required significant manual intervention with commercial synthesis tools. The first tool that is aware of current densities, offered by Pulsic Ltd. [109], adjusts wire widths based on the currents at the terminals, though it is only applicable to direct currents (DC). For analog circuits, in particular, there have been verification tools for current densities available for some time, such as Cadence Virtuoso Power Systems [108], Synopsys CustomSim [110], and Apache Totem MMX [111]. These tools work by extracting a netlist from the layout that includes parasitic components, and then they simulate the currents in all wires. Should any of the simulated current densities exceed the thresholds relevant to EM, the tool detects a violation and flags it for attention.

2.8. Conclusion

A primary challenge in contemporary semiconductor technology is the design of reliable integrated circuits (ICs) that maintain high performance without escalating power consumption or chip area. As technology advances, current densities are increasing, and at the same time, the threshold values opposing electromigration are tightening, a trend that is depicted in Fig. 2.17 [112] - [115].

Furthermore, electromigration mechanism is becoming more intricate and is impacting a broader array of nets. As a result, ensuring EM robustness has become a design challenge and is now tackled at different stages of integrated circuit design and manufacturing shown in Fig. 2.17.

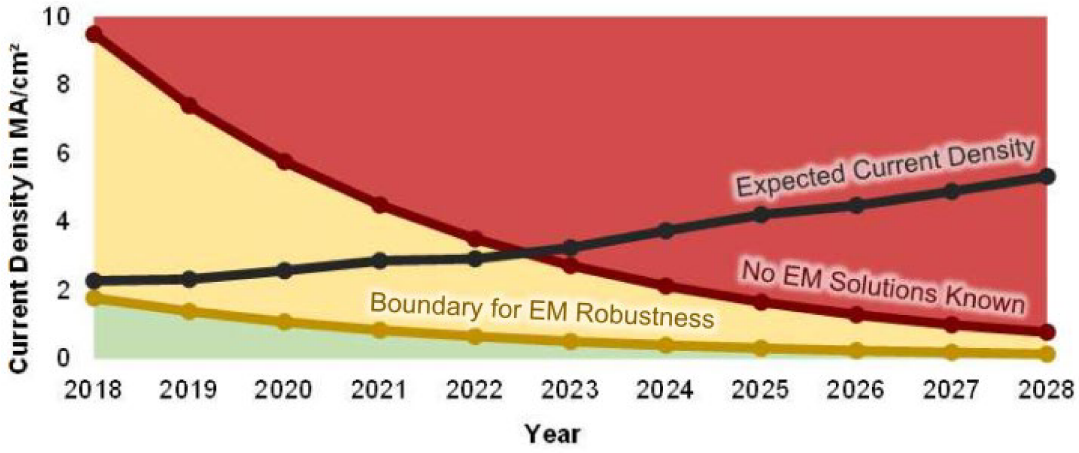


Figure 2.17. Current densities and electromigration (EM) boundary values were forecasted in the 2015 ITRS [108]. The green area represents a zone with no risk of EM degradation, while the yellow area indicates where EM degradation is possible but manageable. In the red area, however, EM degradation occurs, and no known solutions exist for designing EM-robust layouts [112].

The initial constraint related to current density in interconnects gives a choice between limiting the current flow or enlarging the cross-sectional area of the interconnects to mitigate EM. One approach involves curbing the current by reducing the operating frequency, but this would adversely impact the desired performance enhancements in contemporary ICs. Alternatively, opting for the second solution, which entails expanding the cross-sectional area, demands wider interconnects. However, it is not feasible to widen all connections on a chip, and doing so could run counter to the advantages of emerging technologies that rely on smaller structural dimensions [28], [113].

That is why Copper-based interconnect technology encounters significant and formidable challenges as it progresses beyond the 32 nm node [79]. The crucial factor for characterizing the EM risk in these wires is the necessary current density, which implies that the allowable current density should be raised through suitable actions. Since it is not feasible to directly measure current

density at precise points within the conductor, it must be assessed using model-based measurement methods or simulations [116].

Studies are also happening to use short length metal interconnect which gives the benefit of Blech effect. A robust routing using multiple metal lines and multiple vias is becoming necessary. Expanded overlaps of metal-via layers result in an increased quantity of interconnect material at a critical location for EM failure: below, above, and within the via, which is called reservoir effect [117]. In dual-Damascene technology, from EM avoidance standpoint, via-below configurations are preferable to their via-above counterparts as they reduce current crowding [118]. If the metallic crystal lattice has less grain boundaries by introducing small cross sections (which is called bamboo effect), EM diffusion can be reduced as diffusion tends to happen along the grain boundaries. Techniques such as stress liners, dielectric cap or stress memorization are being used to modify the mechanical properties of the materials and reduce the impact of EM [119]. Studying materials with higher melting points or superior resistance to electromigration can be an effective approach [120]. Lowering the operating temperature of the circuit can slow down the diffusion of atoms, reducing the rate of EM. Efficient thermal management solutions are becoming essential to achieve this.

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CHAPTER 3. NOVEL TEST CHIPS FOR ELECTROMIGRATION FAILURE CHARACTERIZARION FROM DC TO GHz FREQUENCIES

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3.1 Abstract

The pursuit of technology scaling has resulted in a substantial rise in Back-End-Of-Line (BEOL) interconnect current density within integrated circuits (ICs). This paper reports the design of novel test chips fabricated using Intel's 22 FFL process technology to assess the electromigration (EM) impact on failure rate of high current densities on Cu-based metallurgies. We have demonstrated the ability for these circuits to characterize direct current (DC), unidirectional pulsed DC as well as bidirectional pulsed AC stress EM effects up to GHz frequencies. Heater structure design enables localized thermal stress up to 300 ^{o}C and is compatible with high-speed CMOS logic infrastructure. Time dependent modulation of the EM effects is studied on 90p Cu alloy metallurgy and results are reported for the first time.

3.2 Introduction

While recent advancements in integrated circuit technology have played a pivotal role in expediting technology scaling, this has been accompanied by a notable increase in Back-End-Of-Line (BEOL) interconnect current density. This, in turn, has increased the risk of BEOL connectivity failures and, as a result, reduced the lifetime due to resulting electromigration (EM) [1]-[3]. The susceptibility of BEOL interconnects can be further exacerbated due to Joule heating,

particularly attributed to an increase in resistivity as the metal interconnect pitch decreases along with scaling [4]. The EM lifetimes of signal interconnects, when subjected to unidirectional pulsed DC (pulsed DC) or bidirectional pulsed AC (pulsed AC) currents, exhibits distinctive features trending with operating frequency [5]. As such the existing DC-based EM risk assessment may not be adequate for enveloping the risk due to the frequency-dependent currents.

For a metal interconnect, current flows from the anode (positively biased) to the cathode (negatively biased). Over time, the atoms within the interconnect begin to migrate from the cathode toward the anode, resulting in void formation on the cathode side and accumulation of material on the anode side. This migration causes volume expansion at the anode and volume contraction at the cathode. However, in copper dual-damascene interconnects, the capping layer, barrier layer, and passivation layer restrict these volumetric changes [6]. As a result, a hydrostatic stress gradient develops along the interconnect line, with tensile stress forming at the cathode end and compressive stress accumulating at the anode end. This stress gradient creates a back-stress force that opposes the atom migration driven by electromigration, ultimately reducing the overall diffusion flow [6].

In the presence of electron wind and hydrostatic stress, the atomic flux J of Cu due to EM can be expressed as [7]:

$$J = D\frac{C}{kT}\left(z^* e\rho j - \Omega\frac{\partial\sigma}{\partial x}\right) \tag{3.1}$$

where E_a is the activation energy of Cu, c is the concentration of Cu atoms, k is Boltzmann's constant, T is the temperature, z^* is the effective charge of Cu ions, e is the elementary charge, ρ is the resistivity in Cu, j is the current density, Ω is the atomic volume, σ is the generated mechanical stress, x is the distance along the metal line in the direction of the electric

current, with $x = 0$ at the cathode, and D is the diffusion coefficient or diffusivity of Cu atoms, which is dependent on temperature and thus governed by the Arrhenius equation as follows [8]:

$$D = D_0 \exp\left(\frac{-E_a}{kT}\right) \tag{3.2}$$

where D_0 is the diffusion constant. The first term in (3.1), which represents the driving force due to the current creating momentum exchange between conducting electrons and metal ion atoms, is absent during the off-period of a pulse stress. The second term of hydrostatic stress allows relaxation of the ion atoms in the reverse direction, thereby facilitating recovery (or healing) effects and reducing the EM damage [9]-[11]. [12] reported a considerable underestimation of the interconnect lifetime, depending on the duty cycle under pulsed DC stressing. The recovery effect is more pronounced under a pulsed AC stressing, as the momentum transfer term turns negative during the off periods, which leads to 'backward migration' of metal atoms and results in a significant enhancement in EM lifetime [13]. For bidirectional pulsed AC EM stress, [11] and [14] reported substantial enhancement in recovery factors close to 1 and corresponding full recovery. [15] observed abrupt and progressive EM failures under 200 MHz pulsed DC stress, while they did not find any failure under bidirectional pulsed AC current. [9] observed a unique frequency dependent MTTF trend shifting from a low- (<100 kHz) to a high-MTTF regime (>10 MHz) when exposed to pulsed DC stressing. The shift was attributed to the thermal effect rather than EM recovery effect.

In the study reported here, the aim was to design and fabricate test chip and investigate frequency dependent EM characteristics under pulsed DC and pulsed AC stress of 100 kHz to 1 GHz. Signals with duty cycle of 50% were used as shown in Fig. 3.1.

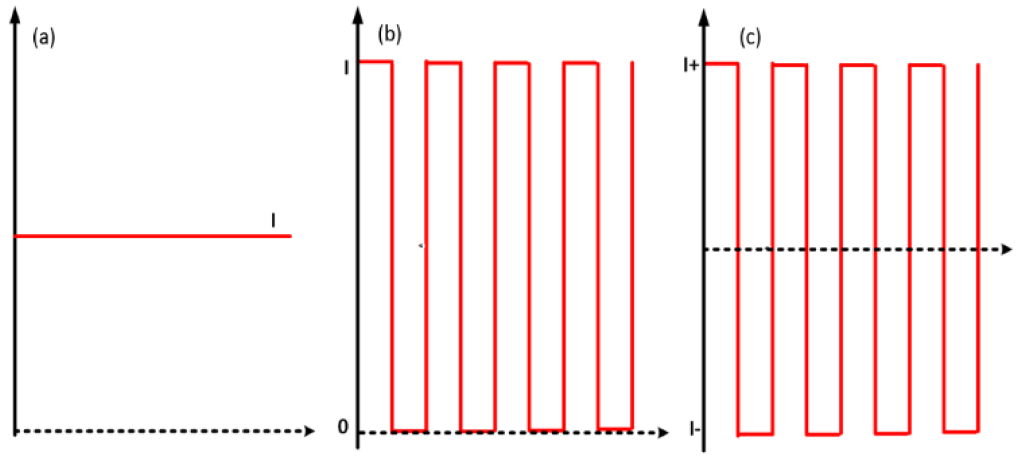

Figure 3.1. EM stress used in our testing (a) DC current (b) unidirectional pulsed DC current (pulsed DC) with 50% duty cycle (c) bidirectional pulsed AC (pulsed AC) current with 50% duty cycle.

We conceptualized and implemented a gigahertz (GHz) range EM testing capability. A circuit-based EM test structure was developed, incorporating both an on-die ring-oscillator (ROSC) and an off-die frequency generator, complemented by a multiplexer (MUX) to offer a broad range of frequencies extending into GHz. An on-die heater utilizing a thin film resistor (TFR) was also implemented as a background heater for thermal conditioning. Previous experiments in pulsed DC and/or pulsed AC EM experiments have predominantly focused on moderate frequencies, typically below 10 MHz, and although [8] achieved testing up to 500 MHz, it is noteworthy that there is a significant gap in the existing literature regarding both the capability and data for GHz-range EM testing. Cu metal line based on Intel's 22 FFL process technology [16]-[17] was employed for the EM testing.

3.3 Circuit Based EM Structures

The standard way to test EM failure is to place the metal interconnect device-under-test (DUT) in an oven at accelerated stress temperature and DC stress current. However, to be able to

measure the effect of pulsed DC and pulsed AC stress current, we designed and fabricated two novel test chips in Intel's 22 FFL process technology [16]-[17] and tested in a dedicated setup. The EM DUT is a Cu metal line, 45 µm long and 44 nm wide. The structure's length is long enough to avoid any Blech effect [18]. The structure is connected with the upper metal by vias. The anode side has 10 vias (three of them are shown in Fig. 3.2), while the cathode side has one. The conventional current generated by the CMOS circuitry comes to the anode and then flows into the cathode side.

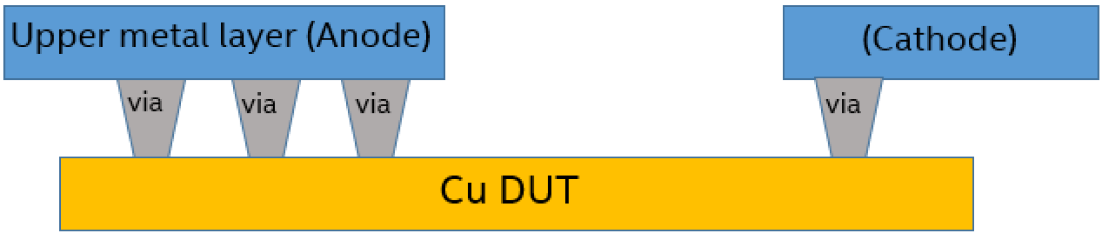

Figure 3.2. EM DUT configuration, current from CMOS circuit arrives at anode and flowing to cathode.

The test chip is essentially split into two parts, shown in Fig. 3.3. These include: 1) CMOS control logic, which consists of a frequency generator, driver, and frequency detector; 2) The on-die heater which envelopes the EM DUT and the temperature sensor.

An on-die ring oscillator (ROSC) and a divider circuit with a multiplexer (MUX) are used as a frequency generator which can provide frequencies ranging from kHz to GHz. Any off-die frequency (kHz to MHz) can also be fed through this same divider circuit with MUX. A large driver is designed to feed the stress current to the EM DUT. A frequency detector is included to validate the stress frequencies downstream from the EM DUT.

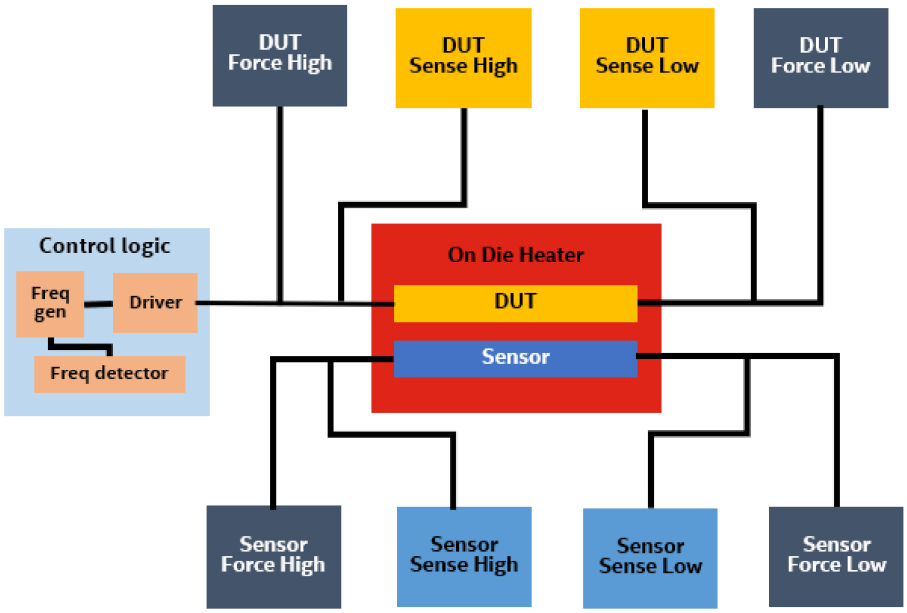

Figure 3.3. EM DUT and metal sensor placed on top of on- die heater, where CMOS logic circuits are kept in safe distance. Four-point Kelvin connections are used for DUT and sensor resistance measurement.

In general, in any CMOS circuit, temperatures far above 120 ºC introduces significant leakage and other reliability problems. To reproduce such effects, a local heater was implemented to provide a ~180 ºC local temperature increase at the EM DUT. The local heater is implemented with a thin film resistor (TFR). The heater contribution, in addition to the die-level test temperature of 120 ºC, yields a local EM DUT temperature of ~300 ºC.

Only the EM DUT and an adjacent metal sensor are placed over the on-die heater. The CMOS circuitry is located at a stand-off distance away from the TFR heater. The proper distance has been determined with post-layout thermal simulations. The metal sensor placed next to the EM DUT measures the actual stress temperature. The metal routings for both EM DUT and the sensor are made as robust as possible using multiple metal lines and multiple vias. For accuracy, and to nullify any effect of metal routing resistances, four-point Kelvin connections have been

provisioned for both EM DUT and sensor. All input and output pads have ESD protection in both the test structures described next.

3.3.1 Unidirectional Pulsed DC Test Structure

This test chip (the CMOS control logic in Fig. 3.3) is shown in detail in Fig. 3.4 that consists of a digital circuit block with a ROSC, a frequency divider, and a frequency selection MUX. This block serves as a signal generator. The EM DUT is driven by a large PMOS transistor, acting as a current driver. There is also a large sized NAND gate to drive the PMOS current driver and a frequency detector with a MUX selection to measure the frequency before and after the EM DUT. The main purpose of this block is to validate the signal propagation. A frequency divider circuit is used to divide high on-die frequencies so they can be measured with ease externally.

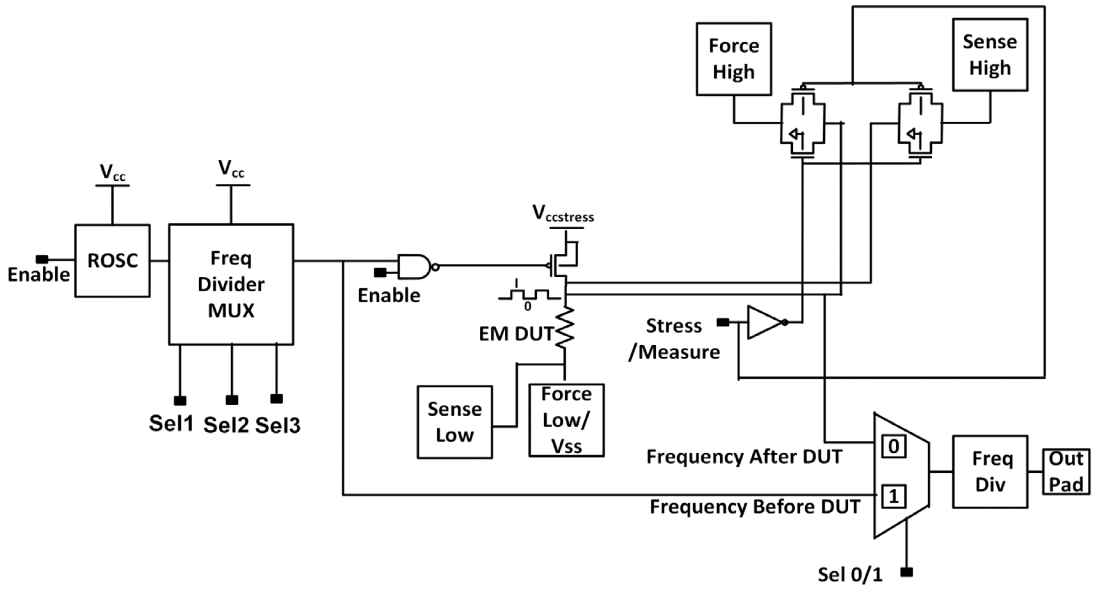

Figure 3.4. EM test structure to work under pulsed DC stress.

For EM effect characterization, optimum-sized transmission gates are used to protect the signal integrity in EM DUT from parasitic capacitance effects generated in the output pads. The transmission gate is an analog switch consisting of both PMOS and NMOS devices.

The power delivery approach includes two rails. The signal generator, NAND gate, frequency detector, and transmission gates are powered up by a nominal power supply (V_{cc}) to avoid any aging effect on the frequency. The PMOS driver is powered up with a dedicated power supply ($V_{ccstress}$) which can take up higher voltages to generate high stress currents,

The EM testing has two modes: stress and measure. An enable signal selects between these two modes. During the stress mode, the signal generator is enabled, the transmission gate is disabled, and the EM DUT is stressed with a pulsed DC stress. In the measure mode, the signal generator and PMOS drivers are off, the transmission gates are enabled, and the Kelvin terminals are available for external characterization.

The same test chip is used to generate EM stress data under DC current. In the DC testing, ROSC is off, the DC stress current is coming from $V_{ccstress}$ and PMOS is constantly on. In this way, the parasitic effect of peripheral circuitry is considered in DC testing and the DC stress results can be compared with pulse-stress-based EM testing.

3.3.2 Bidirectional Pulsed AC Test Structure

The pulsed AC test structure (the CMOS control logic in Fig. 3.3) also has a ROSC block and a frequency selection MUX as shown in Fig. 3.5.

It includes an innovative logic circuit which is controlled by the stress/measure input signal. The EM DUT is connected through large PMOS transistors (A, B) and NMOS transistors (C, D). There are pre-drivers as well, enlarged to properly drive the heavy drivers (A, B, C, D). Like the pulsed DC test structure there is a frequency detector with a MUX selection to measure the frequency before and after the EM DUT so that signal propagation can be verified externally. In this test chip also, optimized transmission gates are used to protect signal integrity during EM characterization at the EM DUT from any parasitic capacitance effects at the output pads. The

power delivery architecture is very similar to the pulsed DC test chip with two rails V_{cc} and $V_{ccstress}$.

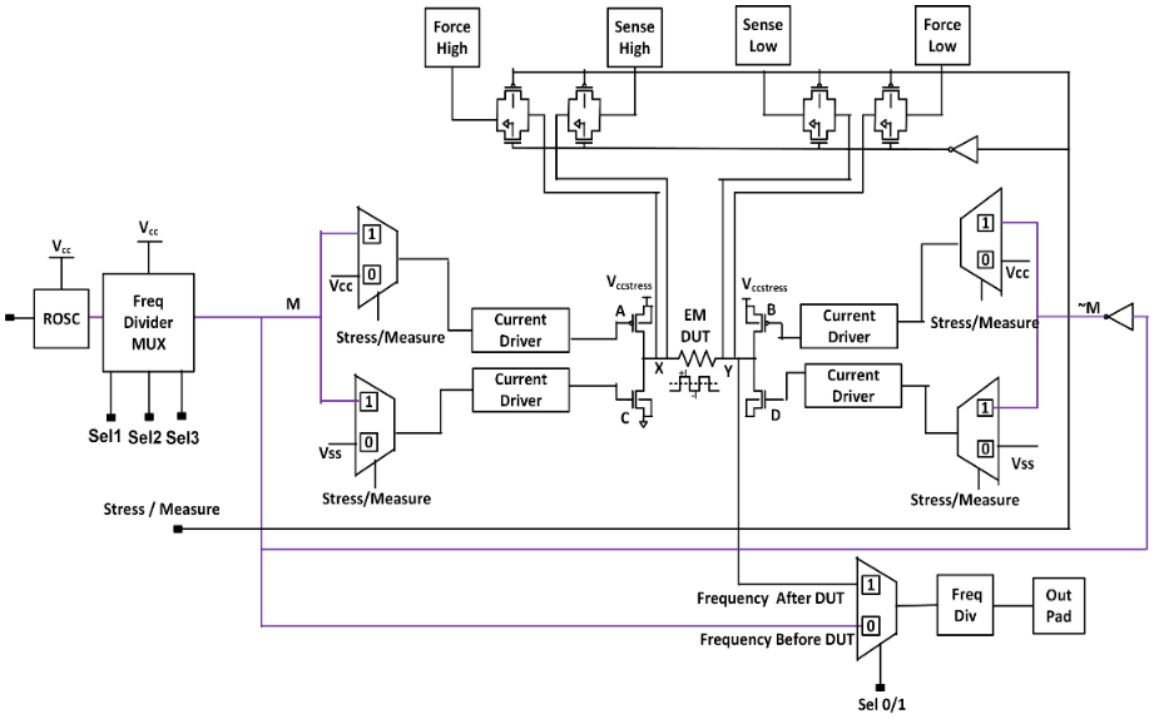

Figure 3.5. EM test structure to work under pulsed AC stress.

Fig. 3.5 shows a simplified schematic of the test chip. The ROSC output M drives devices PMOS (A) and NMOS (C) while the inverted output ~M drives devices PMOS (B) and NMOS (D) (M in purple). While M is zero, A and D are on and current flows from X to Y. While M is asserted, B and C transistors are on and current flows from Y to X. This arrangement creates a bidirectional pulsed AC stress current flow. During the stress mode, all four transmission gates are off When the control signal is in measure mode, the innovative circuit turns all four transistors (A, B, C, D) off. At the same time the transmission gates are enabled to measure the DUT's resistance using Kelvin terminals. The metal sensor resistance is also measured during this time.

3.4 Testing Methodology

The standard methodology of EM testing is to detect EM failures of metal interconnect using wafer level testing under constant DC current and at an elevated temperature (250 ºC -300 ºC) using an oven. The proposed test circuit in this work enables high frequency testing while it provides elevated temperatures. The basic functionality of our EM test structures has been validated on the wafer. For long-term stress, the structures are packaged using wire bonding pin grid array (PGA) packages. A custom board and system have been implemented to test the packaged structures (shown in Fig. 3.6).

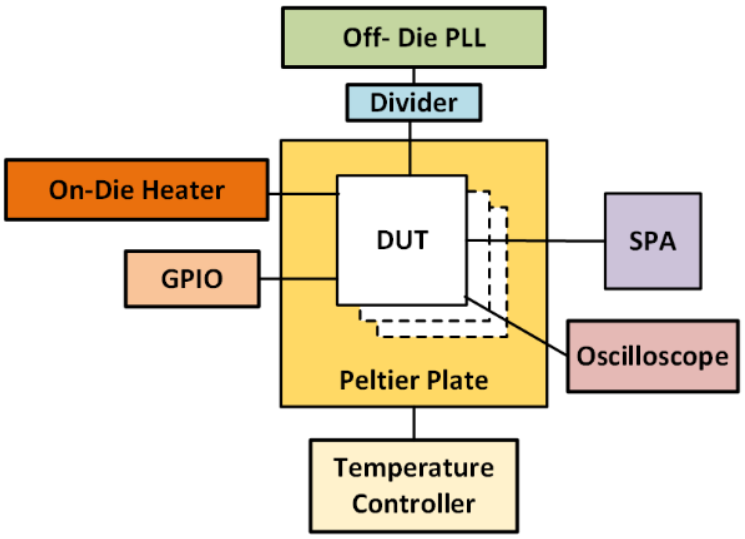

Figure 3.6. Test boards used for packaged test structures.

The system includes general-purpose input output (GPIO) lines to control the DUTs, as well as a low frequency phase locked loop (PLL) and dividers to provide low frequencies (kHz to MHz) to the DUTs. The on-die heater is powered up by a bidirectional current source to avoid any EM effect in the heater itself. The stress current and stress frequency are measured from each DUT individually, using on-board high precision current sensors and frequency counters respectively. During measurement mode, the EM DUT and sensor resistances are characterized with high

precision semiconductor parametric analyzers (SPA). The PGA package temperature is controlled with a Peltier plate.

3.5 Measurement Results and Discussion

3.5.1 On Die Heater Thermal Simulation

Fig. 3.7 shows the thermal profile of the TFR on-die heater alongside the temperature response of both the EM DUT and the metal sensor. TFR on-die heater is comprised of 100 distinct cells and results in 173 ^{o}C of temperature rise over 120 ^{o}C base value in both the metal sensor and the EM DUT as desired.

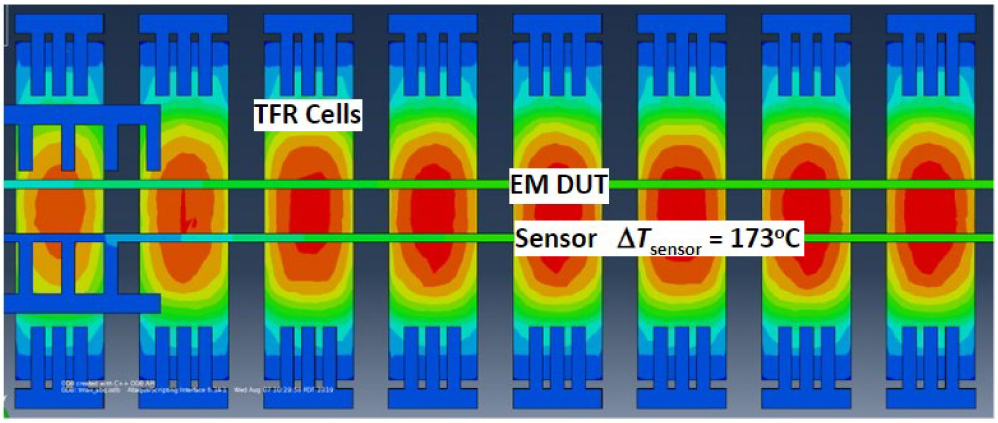

Figure 3.7. Thermal simulation results of the TFR on-die heater and its thermal impact on the EM DUT and the metal sensor.

3.5.2 On Die Heater Measurement

Fig. 3.8 illustrates the temperature measured at the metal sensor with respect to the voltage applied to the TFR on-die heater. The temperature coefficient of resistance (TCR) for the metal sensor was determined by measuring the sensor resistance while varying the Peltier plate temperature. TCR was used to evaluate the temperatures in Fig. 3.8. As depicted in Fig. 3.3, EM DUT and the metal sensor are positioned in close proximity atop the TFR heater, suggesting that the sensor temperature observed in Fig. 3.8 is directly applicable to EM DUT.

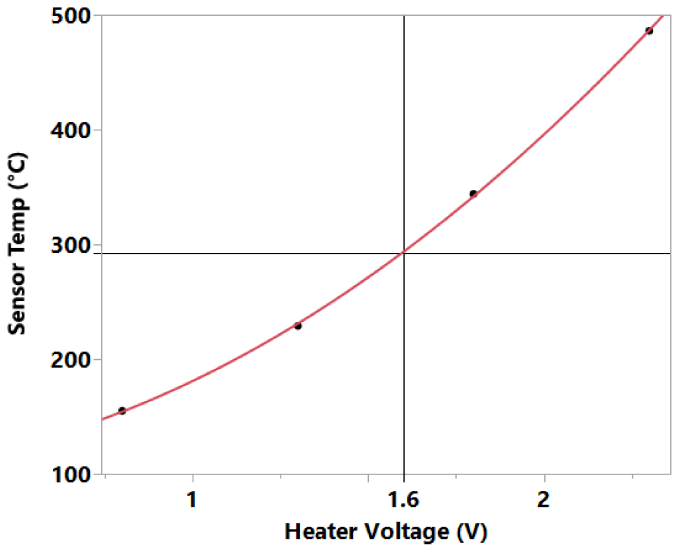

Figure 3.8. Sensor temperature with respect to TFR on-die heater voltage at the Peltier plate temperature of 120 °C.

Notably, the sensor temperature of 293 °C was attainable when the heater voltage was set at 1.6 V and the Peltier plate temperature was maintained at 120 °C. This is consistent with the design that when the Peltier plate supplies an ambient temperature of 120 °C the temperature of the EM DUT can rise to 293 °C. The heater voltage of 1.6 V was consistently used for the thermal conditioning in all EM MTTF measurements.

3.5.3 Stress Temperature Consistency Test

Throughout the EM MTTF measurements, the metal sensor was subjected to an ambient temperature identical to that of the EM DUT. The measured resistance, as depicted in Fig. 3.9, remained remarkably consistent at approximately 600 W during the entire stressing period until the EM DUTs completely failed, indicating that stable and constant thermal conditioning was consistently provided to the EM DUT.

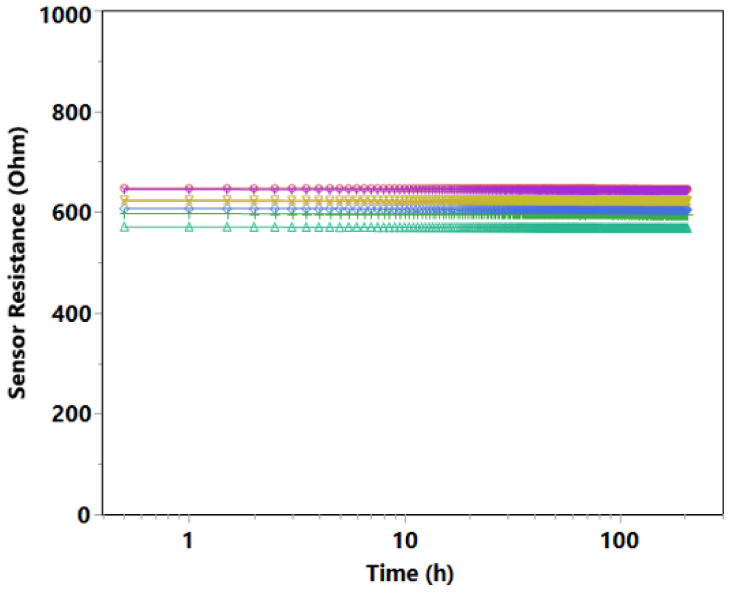

Figure 3.9. Resistance of metal sensor during EM MTTF measurements.

3.5.4 EM DUT Failure Under Pulsed DC Stress

Unidirectional pulsed DC voltage was applied to EM DUT until all EM DUTs completely failed, defined as a 10% increase of resistance. In Fig. 3.10, a pulsed DC voltage of 0.8 V was applied to the EM DUTs at a frequency of 1 GHz with a 50% duty factor. Typical EM failure characteristics (under constant current condition) were observed, (i.e., a sudden resistance jump). Following the resistance jump, however, the EM failure progress seemed to slow down, leading to relatively gradual increase in resistance compared to the initial jump. This was attributed to the reduction in current flow resulting from the EM voiding under constant voltage. The TEM (transmission electron microscopy) image depicting a characteristic EM void beneath a via, which represents the EM failure, is also included in Fig. 3.10 as an inset.

EM MTTF measurements were conducted across a range of frequencies (spanning from 100 kHz to 1 GHz) while including DC stress as well. Pre-stress calibration was carried out to

ensure that the voltages used for pulsed DC stress were set at levels corresponding to an equivalent current for each specific frequency setting.

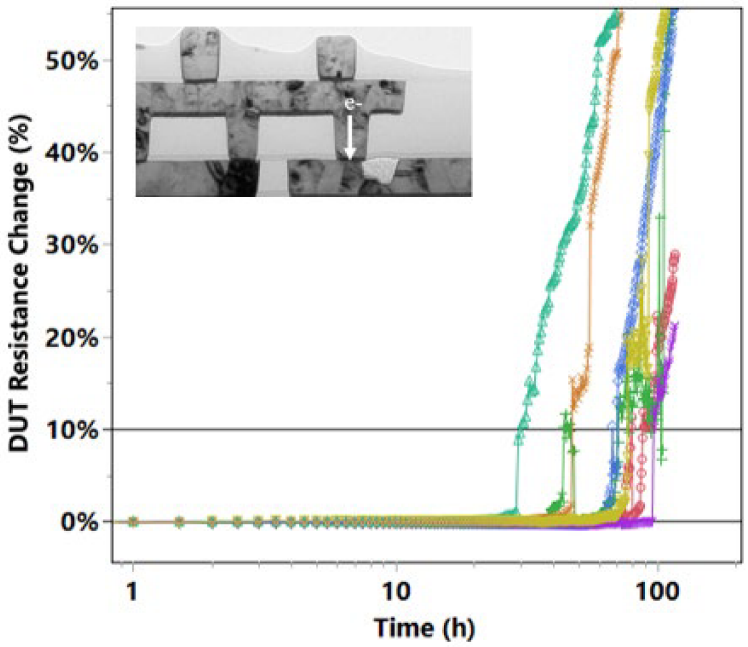

Figure 3.10. A time profile of resistance changes during pulsed DC stressing at a frequency of 1 GHz with a 50% duty factor. TEM image of this EM failure is included as an inset.

Pulsed DC MTTFs are characterized by a modified form of Black's equation [9]:

$$\mathrm{MTTF} = \frac{A}{j^n r^m} \exp\left(\frac{E_a}{kT}\right) \tag{3}$$

where A is a material and geometry-dependent constant, n is the current density exponent, r is the duty factor, and m is the duty factor exponent. When the duty factor exponent m equals 1, it is commonly referred to as the "on-time" model, which directly uses the on-time period of pulsed DC signal for MTTF calculation. The "on-time" model is known to be well-suited for low frequency MTTFs, where the recovery effect during the off-period is minimal [9]. The reported range for duty factor exponent is $1 < m < 2$ [5], [19]-[22]. The modified Black's equation with the duty factor exponent, $m = n$, is recognized as the average current density model. Equation (3) can

be adapted to represent the relationship between pulsed DC and DC MTTFs, as expressed by the following equation [5], [9]:

$$\mathrm{MTTF}_{ratio} = \frac{\mathrm{MTTF}_{pulse}}{\mathrm{MTTF}_{DC}} = \frac{1}{r^m} \underset{@r=0.5}{\equiv} 2^m \tag{4}$$

For our study for the duty factor r = 0.5, the measured MTTF ratios relative to DC MTTF is plotted in Fig. 3.11 across the measured frequency range. This figure shows that the MTTF ratio at 100 kHz is near to 2, which by (4) corresponds to the on -time model with m = 1 implying off period EM recovery is negligible (duty cycle is halved compared to DC, implying the on period is halved to DC, while the MTTF is doubled, implying a DC-like behavior).

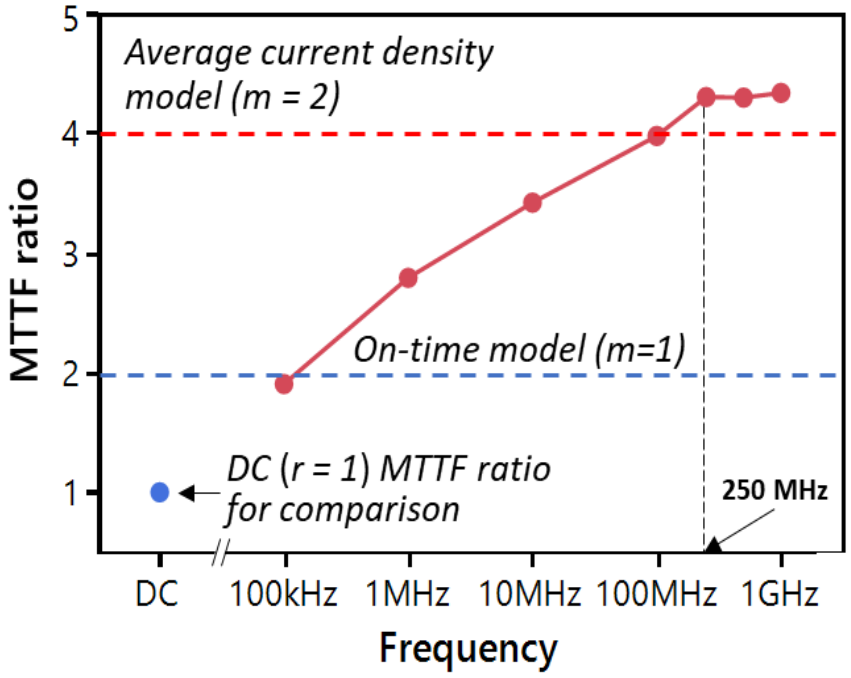

Figure 3.11. MTTF ratios to DC MTTF with respect to frequency. Both on-time model and average current density model (m = 2) lines are also plotted.

However, as the frequency increases above 100 kHz, the MTTF ratio continues to rise, which implies reduced EM degradation, possibly due to less damages in on-periods and/or increased recovery in the off-periods, thereby delaying EM failures and yielding a MTTF ratio

greater than 2. Interestingly, the MTTF ratios in Fig. 3.11 level off at around 4.3 at the frequencies higher than 250 MHz, implying no further significant reduction in the net EM damage rate.

3.5.5 Physics Explanation of EM DUT MTTF Under Pulsed DC Stress

To develop a further understanding of the frequency dependent MTTF, in Fig. 3.12, the temporal thermal behaviors under low- and high-frequency pulsed DC stress are compared, where the solid line depicts the frequency dependent current input, whereas the dashed line represents the frequency dependent temperature profile of the EM DUT. At lower frequencies, the temperature profile (dashed line) can closely follow the square wave pattern of the current input (solid line). This is because the durations of the on- and off-periods are much longer than the thermal time constant of the EM DUT, allowing for nearly full peak-to-peak thermal fluctuations. However, at higher frequencies, the reduced on- and off-times offer reduced duration for temperature rise and fall relative to its time constant, resulting in significantly smaller thermal swings and a temperature profile that substantially deviates from the square wave form.

At the higher frequencies, the lower temperature during the on-periods (relative to that during lower frequencies) results in decreased diffusivity/electromigration, and in contrast, the temperature of the EM DUT during the off-periods is higher relative to that during the lower frequencies, facilitating more effective recovery aided by the increased backward diffusivity caused by higher temperature. These dual effects both favor extended EM lifetime--The frequency dependent thermal behavior depicted in Fig. 3.12 shows both an on-period temperature decrease, and an off-period temperature rise at higher frequencies, that jointly contribute to the MTTF reduction in pulsed DC stress at higher frequencies. Also, there is relatively little room for the temperature swing to decrease beyond the 250 MHz, causing no further net reduction in EM damage rate at further higher frequencies, and hence the observed saturation beyond the 250 MHz.

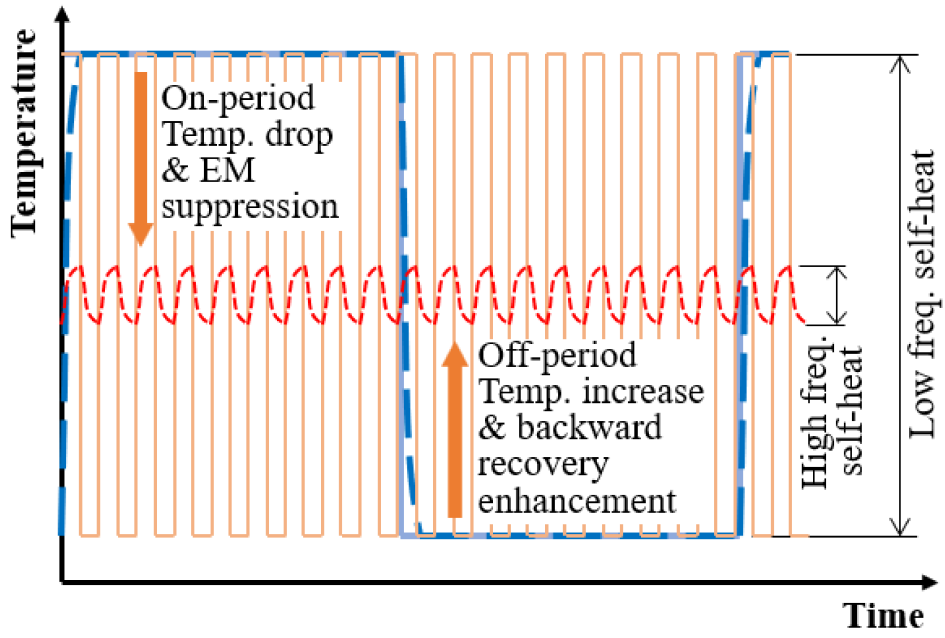

Figure 3.12. Comparison of temperature swings (dashed lines) under unidirectional pulse stress (solid lines) between low- and high-frequency.

3.5.6 EM DUT Failure Under Pulsed AC Stress

We did not find any EM failure from bidirectional pulsed AC stress structures after two months of EM stressing. This finding is indicative of a nearly full EM recovery during negative cycle of the stress current, which also aligns with and corroborates the results reported by [11] and [14].

3.6 Conclusion

In this study, a novel EM test chip was designed, fabricated, and tested, which is uniquely capable of pulsed DC and AC stressing of an interconnect for electromigration effects over a wide range of frequencies spanning from DC to 100 kHz to 1 GHz based on Intel's 22 FFL technology. Additionally, thin film resistor (TFR) on-die heater was incorporated to provide stable and consistent thermal conditioning up to ~300 ^{o}C. Frequency dependent MTTF trend was experimentally demonstrated. At low frequencies up to 100 kHz, the recovery during the off-period

was not effective, leading to the MTTF ratio following the on-time model. At frequencies spanning 100 to 250 MHz, the increasing rise in the MTTF is indicative of net reduction in EM damage rate. At frequencies exceeding 250 MHz, however, the increase in the MTTF ratio surpassed what was originally anticipated based on the average current density model that accounts as reported in [5], [8], meaning that these previous publications failed to adequately account for the thermally induced benefits at higher frequencies due to an on-period EM suppression and an off-period EM recovery. Thermal simulation revealed that the MTTF enhancement at high frequencies was primarily attributed to a reduction in the on-period self-heat and in contrast its off-period increase affording a higher recovery. Additionally, no EM failures were observed in bidirectional stress tests implying close to full EM recovery during the negative stress periods.

Note due to the interplay between the electromigration time constant versus the self-heat (SH) driven temperature time constant, it is not feasible to separate out the contribution of each mechanism towards the observed MTTF dependence on frequency. If indeed in some practical setting a lower stress current results in negligible self-heat, our approach can still be utilized for the MTTF study, and where the effect of thermal time constant would have no role (since negligible self-heat), and only the electromigration time constat will be effective.

In summary, EM lifetime subjected to unidirectional pulsed-DC can be substantially enhanced, especially at high frequencies. Our study shows that when significant self-heating is accompanied during on-period, existing EM model based on modified Black's equation (the average current density model) does not effectively predict the unidirectional pulsed DC MTTF trend. The MTTF saturation beyond 250 MHz is another interesting observation of our study.

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CHAPTER 4. NON-UNIFORM HEATING INDUCED ELECTROMIGRATION FAILURE CHARACTERIZATION USING LASER

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4.1 Abstract

Very-large-scale integration (VLSI) technology scaling has resulted in a substantial rise in power density within a chip. This leads to thermal non uniformity across integrated circuits (ICs) impacting electromigration (EM) which occurs due to dislocation of conducting elements of interconnects caused by electron flow. Detecting EM risk by accelerated stress methods is an active area of research. This paper describes a technique that uses laser to create concentrated area of high temperature, or hot spot. The high temperature is applied to targeted areas of the specific circuit or intellectual property (IP) block of a product while the rest of the chip continues to operate at standard conditions. The notable benefit from this technique is the capability to selectively accelerate the stressing (electromigration) process of an individual IP block, rather than stressing the entire chip uniformly.

4.2 Introduction

As devices are miniaturized through fin field effect transistor (FinFET) technology, the power density of the products increases. This miniaturization trend can lead to notably elevated temperatures in specific regions within an IC (integrated circuit). Consequently, there is a growing attention to thermally generated reliability concerns such as fin induced self-heating (FISH), thermal runaway, thermal migration, negative bias temperature instability, electromigration (EM). These are the main degradation mechanisms sensitive to temperature that present significant risks

to interconnect failures and device reliability. Electromigration occurs due to the movement of atoms caused by the flow of current through the metal interconnect. When the current density is sufficiently high, the heat generated within the interconnect can repeatedly dislodge atoms from their original positions creating voids and hillocks. The conventional approach to ensuring product's thermal reliability involves conducting accelerated aging tests, exposing a product to elevated temperatures and voltages (also known as a stress test or High Temperature Operating Life test) for a duration that estimates the product's entire lifespan under normal usage conditions by the customer [1].

In this scenario, multiple issues arise: First, the product may exhibit various failure modes, each with its own rate of occurrence. It is challenging to identify which mode is the main reliability limiter. Second, the equipment utilized for stressing products, such as tester cards and reference design PCB (printed circuit board), have a finite capacity for power delivery. An increased power demand during stress testing can strain these power delivery systems. This issue restricts the highest possible temperature that can be used for stress conditions. Also, no mechanism exists to perform non-uniform or spot heating that arise in practical setting, although a sensor circuit to detect void formation under uniform heating was reported in [2]. The authors applied standard uniform heating, waited for initial void to expand over metal line, and detected the increased resistance by using the sensor circuit, while collecting intermediate TEM (transmission electron microscopy) images during the process.

Addressing these factors, a novel method has been developed to create high temperature at localized areas (hot spots) on a die that is operating under standard conditions by targeting the area of interest with a continuous wave (CW) laser. This approach facilitates the analysis of thermal effects in two keyways: (1) it confirms the adequacy of the test temperature with high precision,

and (2) it assesses the temperature-related aging and susceptibility of specific IP blocks within the silicon. Our method provides both high spatial precision and rapid testing, as a few days of laser-induced temperature stress reproduces the effects of multiple years of regular usage, while the rest of the chip remains unaffected and continues to operate normally.

As per our knowledge, this is the first time a non-uniform temperature based electromigration effects are made possible and the corresponding results are reported.

4.3 Non- Uniform Heating Based Electromigration

For the past thirty years, electromigration has been the subject of active research [3]-[5]. As device sizes shrink, it becomes possible to increase the number of devices per unit area, enhancing in-device density and causing higher current density within the device, which in turn raises operating temperatures non-uniformly within the ICs. Further, the need for high-speed operation results in a higher frequency switching that has its own ramifications towards heating pattern. These factors collectively contribute to making electromigration a significant challenge for the reliability of contemporary ICs.

In case of a metal interconnect, the current flows from anode to cathode (i.e., the electrons flow from cathode to anode), and a current-induced electromigration accelerates under higher temperature, when the interconnect atoms start migrating from cathode to anode, leading to the formation of voids on the cathode side (and piling on the anode side).

This results in volume expansion at the anode and volume contraction at the cathode. However, the surrounding layers in copper dual-damascene interconnects, specifically the capping layer, barrier layer, and passivation layer prevent these volumetric changes. Consequently, a gradient of hydrostatic stress develops within the interconnect line. Tensile stress arises at the cathode end, while compressive stress builds up at the anode end. This stress gradient acts as a back stress force that counteracts the forward migration of atoms caused by electromigration,

ultimately reducing the overall diffusion flow. This mechanism is called stress migration (SM) [6]-[7].

Thermal migration, also known as the thermomigration (TM), is driven by temperature gradients. It occurs due to mainly two reasons: 1) If there is a temperature difference in a metal interconnect, atoms situated in hotter regions are more likely to become dislodged because they are more energetically activated by the heat. Consequently, there is a higher rate of atomic diffusion from the warmer areas to the cooler ones compared to the movement in the reverse direction. This imbalance results in a net diffusion, towards the areas with lower temperatures, following the path of negative temperature gradients [6]-[7]. 2) The current flow sets off the electromigration of atoms, leading to the formation and expansion of voids, which progressively compromise the structural integrity of the area impacted by EM. As a result, the local current density intensifies, which in turn raises local temperatures due to Joule heating. This creates a positive feedback loop that further speeds up the diffusion of atoms and exacerbates the growth of voids.

Stress migration acts against the flow of electromigration, while thermal migration speeds it up. In general, stress migration (SM), thermal migration (TM), and electromigration (EM) are closely linked, as their effects are intertwined. Together, they play a role in determining the overall pattern of atom migration within the metal interconnects.

In standard electromigration test, high current density and high temperature are used as stress conditions, and where standardly, the applied temperature remains uniform along the metal interconnect. In such a test, thermal gradient generally occurs due to non-uniform resistance induced from electromigration and resulting non-uniform Joule-heating from the flowing current. In other words, the resulting thermal gradient is not controllable in traditional EM test. In our proposed laser based electromigration experiment, the laser induced stress temperature is

generated on a specific spot on the metal line, whereas the rest of the metal line has relatively lower temperature, mimicking real-world spot-heating with a non-uniform temperature distribution across the metal line.

4.4 Traditional EM Test Structure

The standard method for testing EM failure involves placing the metal strip designated as the device under test (DUT) in an oven, subjecting it to an accelerated stress temperature and at a DC stress current. This is shown in Fig. 4.1, where the EM DUT is a Cu metal line designed and fabricated in Intel's 22FFL [8]-[9] process technology. The DUT's length is chosen to be long enough to avoid any Blech effect [10]. The test structure is connected to the upper metal line using via and four-point Kelvin measurements are provisioned in the test structure. During the stress phase, stress current from a source measure unit (SMU) comes to the anode and then flows into the cathode side. During the measurement phase, a small current is flown through the force pads and the voltage difference in the sense pads is measured, to then calculate the DUT resistance which is indicative of a void formation.

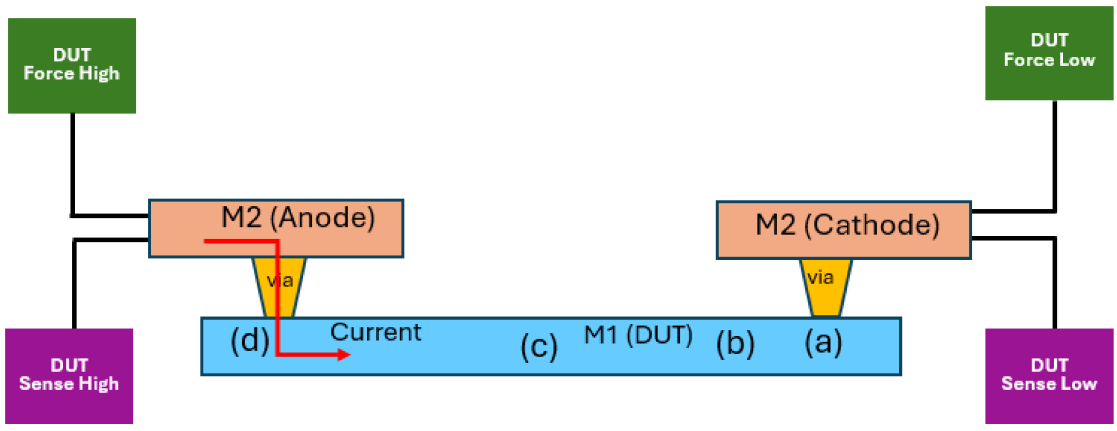

Figure 4.1. EM DUT configuration, current from SMU is coming to anode and flowing to cathode side.

4.5 Laser based Spot- Heating Set Up

In our design, the silicon die with the EM DUT structure is packaged using wire bonding over a test board. The package has a glass opening for exposing to laser. The test board is connected to a source of stress current and the instrument for measuring voltage, current, and resistance.

Laser light in microwave range (1550 nm) is directed into the silicon device from the bulk side. Since the photon energy at 1550 nm (0.8 eV) is less than the bandgap of silicon (~1 eV), it does not cause inter-band transitions to excite electrons from valance band to conduction band. Thereby laser heating does not generate electron-hole pairs or additional free carriers (whose movement could also contribute to EM). The laser can still transfer energy to the free carriers in the conduction band, leading to intra-band absorption and localized heating, shown in Fig. 4.2. This is important because this free carrier absorption (FCA) phenomenon does not interfere with the carrier dynamics (i.e. currents, threshold voltages, voltages at nodes, etc.) of the device under analysis, yet it generates sufficient localized heating.

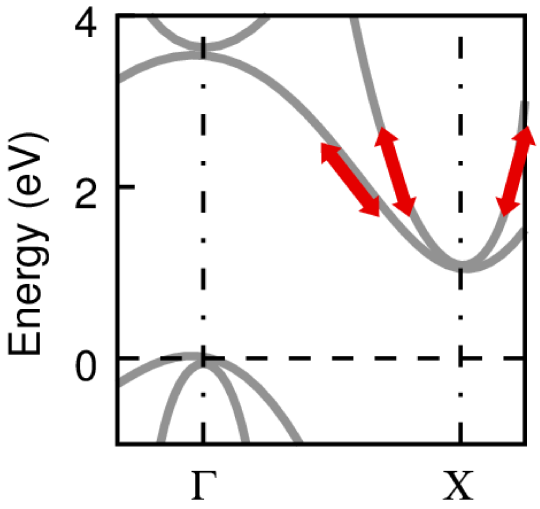

Figure 4.2. Inter-band thermal laser process.

The laser light is precisely focused on the silicon, targeting an area at or below the level of the fins, to a spot of diameter approximately 1-2 micrometers. This concentration of light energy centered into a rather small area results in the generation of temperatures that can't exceed 300 °C.

For testing complex devices with advanced multilayer interconnect technology, the FCA process based localized heating works well as this process generates heat in the semiconductor bulk. However, with backside-injected FCA it is important to use a bulk thickness that balances a good interaction length to generate heat and a limited heat diffusion to target the region of interest. Accordingly, in this work the samples are thinned 50 μm.

In general, to determine the bulk side thickness needed for creating a specific temperature profile, it is essential to consider the wavelength, absorption coefficient, and carrier density. The absorption coefficient is a measure of how much light can be absorbed by a particular material, which has to do with how deeply the light can penetrate into the material. The wavelength of light also determines the penetration depth and the absorption coefficient. Carrier density refers to the concentration of free charge carriers (electrons and holes) in the material, which determines the level of interaction of light with the material. These factors collectively determine how much the substrate needs to be thinned to allow the laser beam to heat the target area within the metal line effectively.

The laser setup along with the test board and the packaged silicon is shown in Fig. 4.3. The laser beam used in this work is a continuous wave laser with a coherent monochromic light of wavelength of 1550 nm. The laser's power depends on the applied current value. A commercial power supply is used to maintain a desired current into the laser diode. In our case, the power output and intensity of the beam is held constant throughout the experiment. The additional power control consists of a polarizer and a wave plate. The polarizer rejects one polarization while

transmits the rest of the light. The polarized light passes through a wave plate with adjustable angle. By varying the angle of the laser light, its delivered power can further be adjusted.

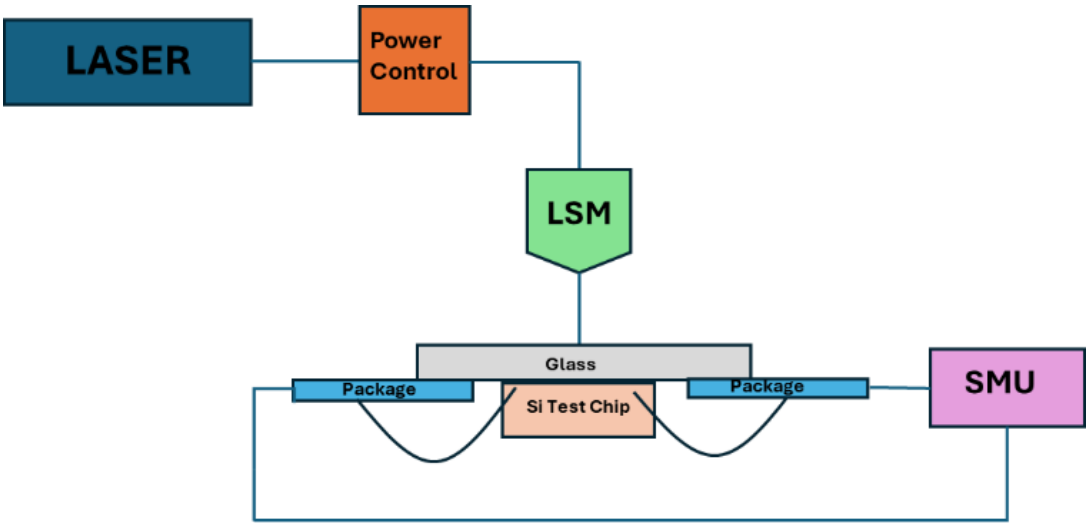

Figure 4.3. Laser with a power control and LSM to locally heat up the packaged silicon through a glass opening. SMU serves as a source of current to the DUT, and it measures the voltage, current, and resistance of the DUT.

The polarized laser light is passed through a laser scanning microscope (LSM) to scan a detailed image pattern on the sample. This setup allows polarized focused light to create localized hot spot on the desired location in the DUT. The objective lens used has a numerical aperture of 0.8 [11].

4.6 Results and Discussions

Before starting the temperature stress testing, the TCR (Temperature Coefficient of the Resistor) was characterized by varying its temperature. Then a laser-based scan was performed throughout the test structure to evaluate the resistance profile across the DUT. Using the TCR value, the resistance profile was converted into temperature profile and the resulting contour plot is shown in Fig. 4.4.

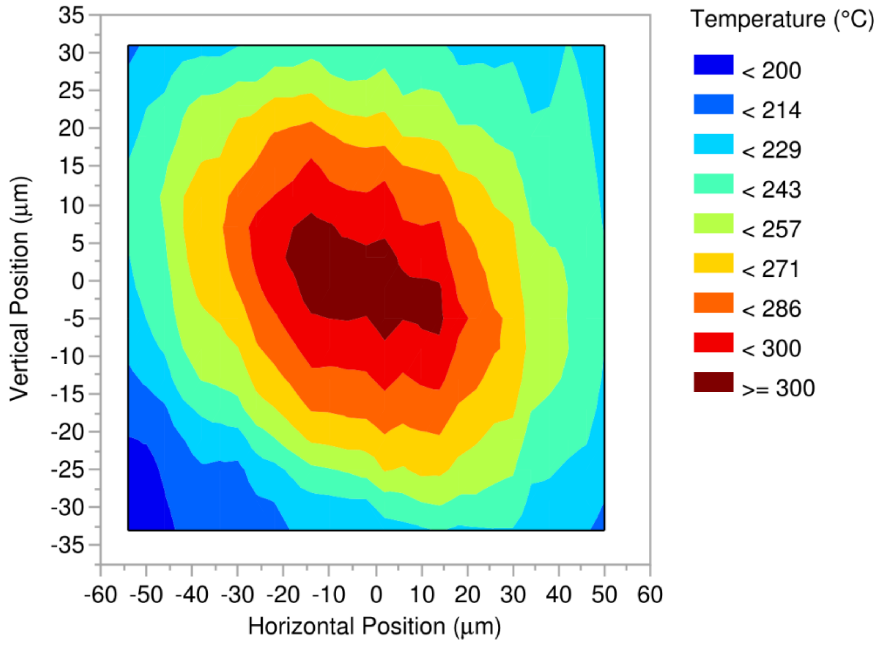

Figure 4.4. Thermal spatial profile of the test structure by laser scanning.

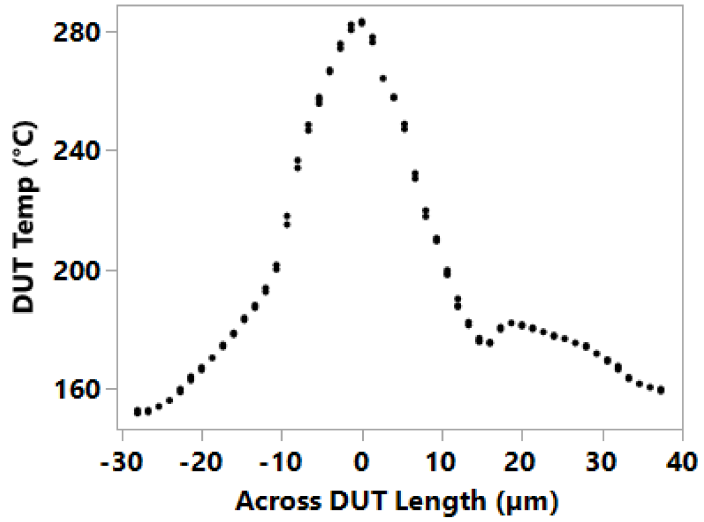

Figure 4.5. Cross section of thermal spatial profile across the DUT.

A cross section was taken from the thermal spatial profile to understand the temperature gradient across the DUT length. It was found (see Fig. 4.5) that a temperature of 280 °C was maintained

over ~ 2 μm. The heat diffused to 120 °C in 40 μm, further dropping down to almost room temperature in 100 μm. This result demonstrated that the laser heating is highly localized.

After obtaining a thermal spatial profile of the DUT, laser was focused on the desired location for thermal stressing. Our primary objective was to study the non-uniform heat effects on two types of locations on the DUT: 1) metal-via junction, i.e., location (a) in Fig. 4.1, and 2) on the meal strip, i.e., location (b) or (c) in Fig. 4.1. The laser location on the metal-via and on the metal strip is shown in Fig. 4.6.

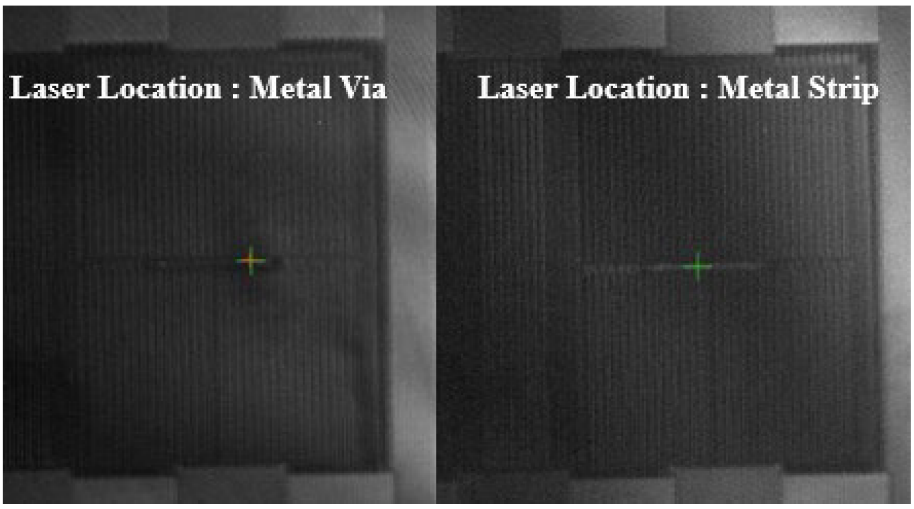

Figure 4.6. Laser location on the metal-via junction (left) and metal strip (right).

Since there is some variability in DUT resistance and in the bulk thickness, each unit was pre-characterized for heat generation by varying the laser power as shown in Fig. 4.7.

The sample was subjected to a stress current density of 0.0015 A/μm^2. To prevent any damage to the glue used to mount the silicon on the glass substrate, the experimental temperature was limited to 280 °C by applying a laser diode current of 30 A and adjusting the power with polarizer system.

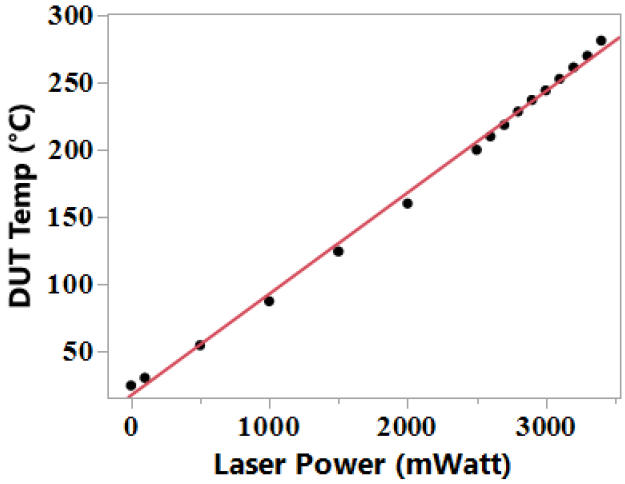

Figure 4.7. DUT temperature vs laser power, calibrated before starting the stress.

This laser based non-uniform thermal stress generation capability is the very first to our knowledge, and we used it to study the impact of the location of localized heating on time to failure of EM DUT. For this, we focused the laser on three primary locations on the DUT: 1) At metal-via junction, i.e., location (a) in Fig. 4.1 (this location is labeled as 0% location), 2) One quarter of the length away from the metal-via junction, i.e., location (b) in Fig. 4.1 (this location is labeled as 25% location), and 3) At the center of the strip, i.e., location (c) in Fig. 4.1 (this location is labeled as 50% location).

The DUT resistance results as a function of stress time are shown in Fig. 4.8. First, we observed that at the 0% location, the time to failure was much less compared to those at 25% and 50% locations. Second, there was an abrupt increase in DUT resistance at the metal-via location (0% location), while on the metal strip (both 25% and 50% locations) the DUT resistance increase was bit gradual initially (for the initial 120 hrs. or so) before attaining an abrupt rise eventually.

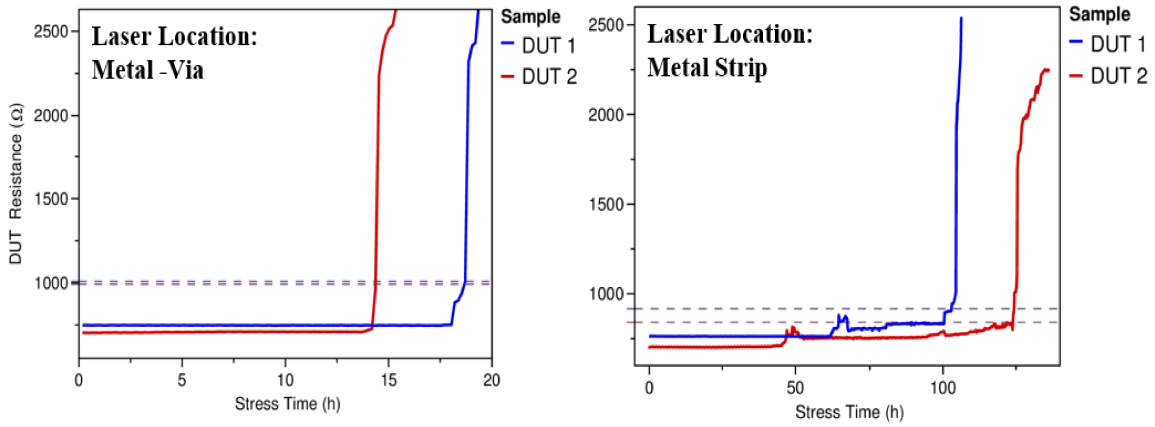

Figure 4.8. DUT Resistance failure over time: metal-via junction (left) and metal strip (right).

To confirm the physical failure mechanism, failure analysis was done on both types of failure locations. The corresponding TEM (Transmission Electron Microscopy) images are shown in Fig. 4.9. From these laser-based thermal stressing experiments, we observed two distinct failure modes based on the location types of the laser injection, metal-via junction versus metal strip.

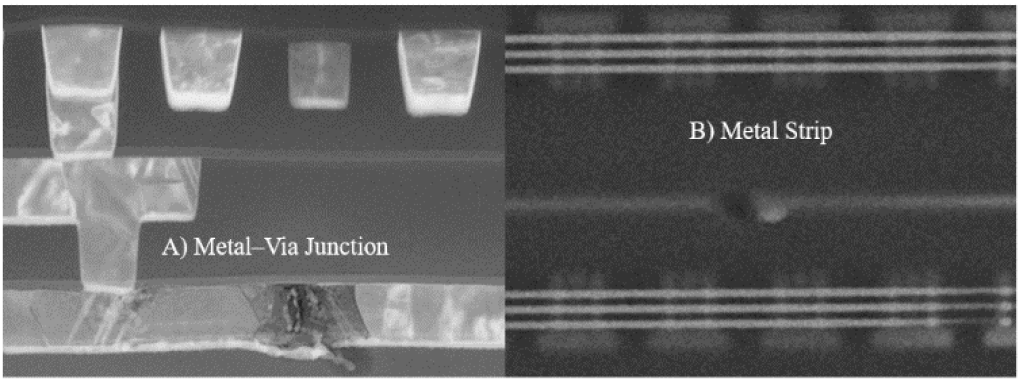

Figure 4.9. TEM images of void formations a) metal-via junction, b) on metal strip.

At metal-via junction, the via width is much smaller than the metal width, increasing the rate of void formation compared to the metal strip, reaching the critical size in about 15 hrs, an order of magnitude smaller compared to the metal strip. Once the void reached a certain critical size, there was a sharp increment of resistance.

The gradual then abrupt resistance change on metal strip suggests the existence of recovery/healing effect during the initial EM before the initial void turned into its critical size. The opposing effects of thermal versus stress gradients played the pivotal roles for delaying the critical size of the void [2]. To gain deeper insight into the contribution of each of these factors, intermediate TEM imaging of the silicon can be conducted, offering additional valuable information.

The electromigration failure criteria is defined in the JDEC standard as a 20% rise in the original resistance [12]. However, the industry-wide EM failure criteria is considered as 10% increment of resistance, as even the 10% increment in resistance causes a significant RC delay in high-speed circuits such as clock generators [13], [14]. For the abrupt failures at the metal-via location (0% location) the 10% failure criteria or 20% criteria are essentially equivalent to indicate a failure time. For failures on the metal strip (both at the 25% and 50% locations), there are initial resistance changes (even reaching 10%) indicating precursor sub-critical voids, but meaningful void occurs much later than the initial 10% resistance increment. Hence, for the metal strip, the industry wide criteria of 10% resistance change does not adequately reflect the occurrence of EM failure. The time to increase 10% DUT resistance and time to attain EM failure at the various laser injected locations are shown in Fig. 4.10.

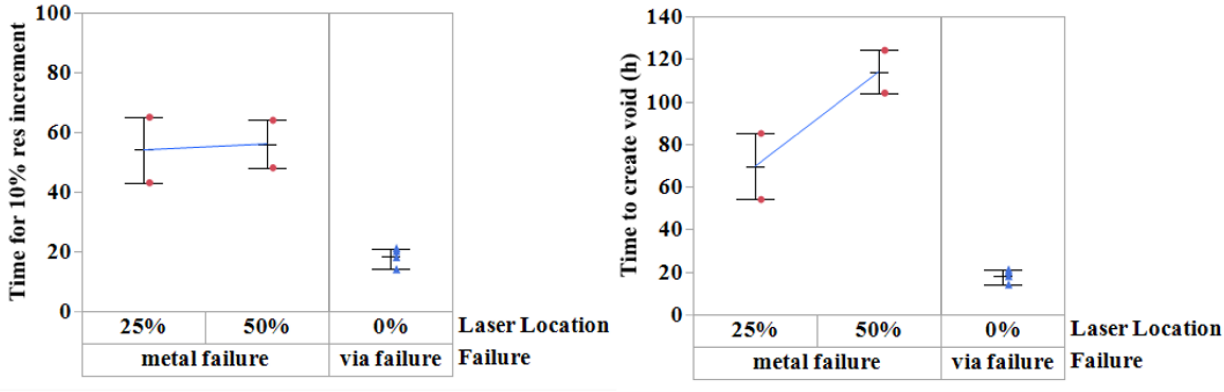

Figure 4.10. Time taken for 10% increment of DUT resistance versus time taken to generate void as a function of the laser injection locations.

4.7 Conclusion

This paper introduced for the first time a laser-based mechanism for localized heating for creating true thermal gradients and corresponding thermal stress. It also presented laser based thermal stress test study, to report a very first non-uniform heat based electromigration data. The failure mode signatures based on the types of heating locations have been presented. In any IC product, if a designer thinks any specific location to be most vulnerable to temperature stress, the proposed laser-based mechanism facilitates the desired localized heat testing that not only does not heat up the rest of the product area, but also does not activate any extra carriers during the heating process. It may be possible to use the proposed laser-based test mechanism to study other reliability mechanisms such as hot carrier injections, bias stability, soft error rate, time-dependent dielectric breakdown, etc.

4.8 References

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CHAPTER 5. GENERAL CONCLUSION

A primary challenge in contemporary semiconductor technology is the design of reliable integrated circuits (ICs) that maintain high performance without escalating power consumption or chip area. As technology advances, current densities are increasing, electromigration is becoming a high risk for ICs. The EM failure in high-speed ICs such as clock generators, SerDes is under more scrutiny as there is limited research on EM failure due to MHz to GHz frequency effect.

This thesis describes the novel EM test chips were designed, fabricated, and tested, which were uniquely capable of pulsed DC and AC stressing of an interconnect for electromigration effects over a wide range of frequencies spanning from DC to 100 kHz to 1 GHz based on Intel's 22FFL technology. The on-die ring oscillator provided the high frequencies, the on-die heater generated the local uniform heat to stress the metal interconnect without creating any functionality issues to the rest of the test chip. At 100 kHz EM MTTF was twice the MTTF at DC. But as the frequency increased, we found out due to thermal swing limitation from 1 MHz to 250MHz, the lower temperature during the on-periods (relative to that during lower frequencies) resulted in decreased diffusivity/electromigration, and in contrast, the temperature of the EM DUT during the off-periods was higher (relative to that during the lower frequencies), facilitating more effective recovery aided by the increased backward diffusivity caused by higher temperature. These dual effects both favored extended EM lifetime. After 250 MHz as thermal swing was almost constant EM MTTF benefit was also constant.

Due to the interplay of Cu atom diffusion time constants and self-heat driven temperature time constants, it was not feasible to de-convolute the contribution of each mechanism towards the observed MTTF dependence on frequency. A lower stress current resulting in negligible self-heat may be an alternative approach to decouple of the effect of thermal time constants. In these tests,

the on-period EM suppression would be minimized, and the off-period EM recovery would be primary mode of enhancement and effective even from low frequencies since the off-period temperature will closely match that of the on-period. As such, the tests will provide a more comprehensive understanding on how pulsed DC EM behavior varies with frequency. However, those approaches may require significantly longer stress durations to achieve meaningful results.

This thesis also introduced for the first time a laser- based mechanism for localized heating for creating true thermal gradients and corresponding thermal stress. It also presented laser based thermal stress test study, to report a very first non-uniform heat based electromigration data. The failure mode signatures based on the types of heating locations were also presented.

At metal-via junction, the via width was much smaller than the metal width, increasing the rate of void formation compared to the metal strip. The void reached the critical size at metal-via junction was an order of magnitude less time compared to the metal strip. Once the void reached a certain critical size, there was a sharp increment of resistance.

The gradual then abrupt resistance changes on metal strip suggested the existence of recovery/healing effect during the initial EM before the initial void turned into its critical size. The opposing effects of thermal versus stress gradients played the pivotal roles for delaying the critical size of the void.

In future to gain deeper insight into the contribution of each of these factors, intermediate TEM imaging of the silicon can be conducted, offering additional valuable information.

In any IC product, if a designer thinks any specific location to be most vulnerable to temperature stress, the proposed laser-based mechanism facilitates the desired localized heat testing that not only does not heat up the rest of the product area, but also does not activate any extra carriers during the heating process.