Ultra-Low Power Logic and Photonics: Challenges and Opportunities

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3/31/2023

Ack: NSF **ECCS-2042079** intel **ECE, ICTAS**

VirginiaTech
Invent the Future

Outline

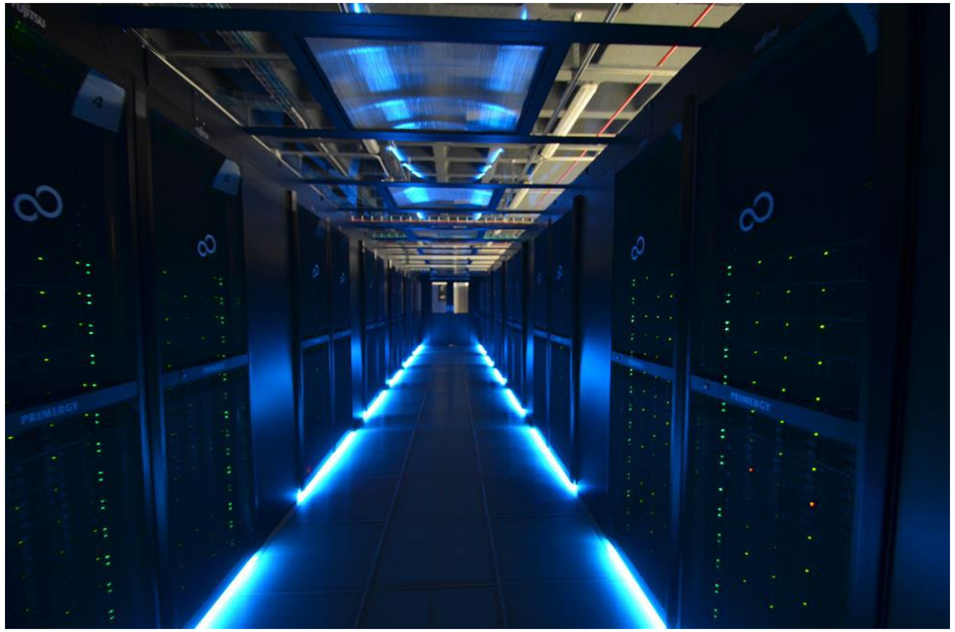
- Introduction
- Our research towards (Materials –to-devices of non-Si materials)
  - Energy-efficient devices for logic and memory at ultra-low voltage (Ge, GeSn on In(GaAl)As)
    - Tunnel FETs and FinFETs
    - High-k dielectrics, MOS-Cs on Ge and strained Ge (ε-Ge)
  - MBE growth → materials analysis → device/modeling feedback
    - Defect control, strain and bandgap engineering group IV & III-V materials
    - Heterointerface control at atomic level
  - Group IV GeSn quantum materials for photonics
    - Magnetotransport on strained Ge
    - Carrier lifetime on group IV (Ge, ε-Ge, GeSn) materials
- Summary & Challenges

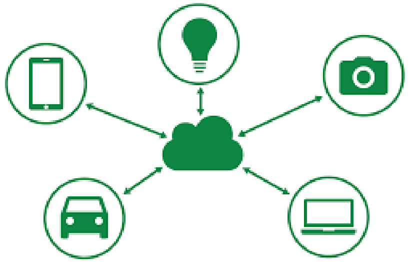
Why Do We Need Now?

Desktop/PC → Mobile Devices

Desktop/PC → HPC

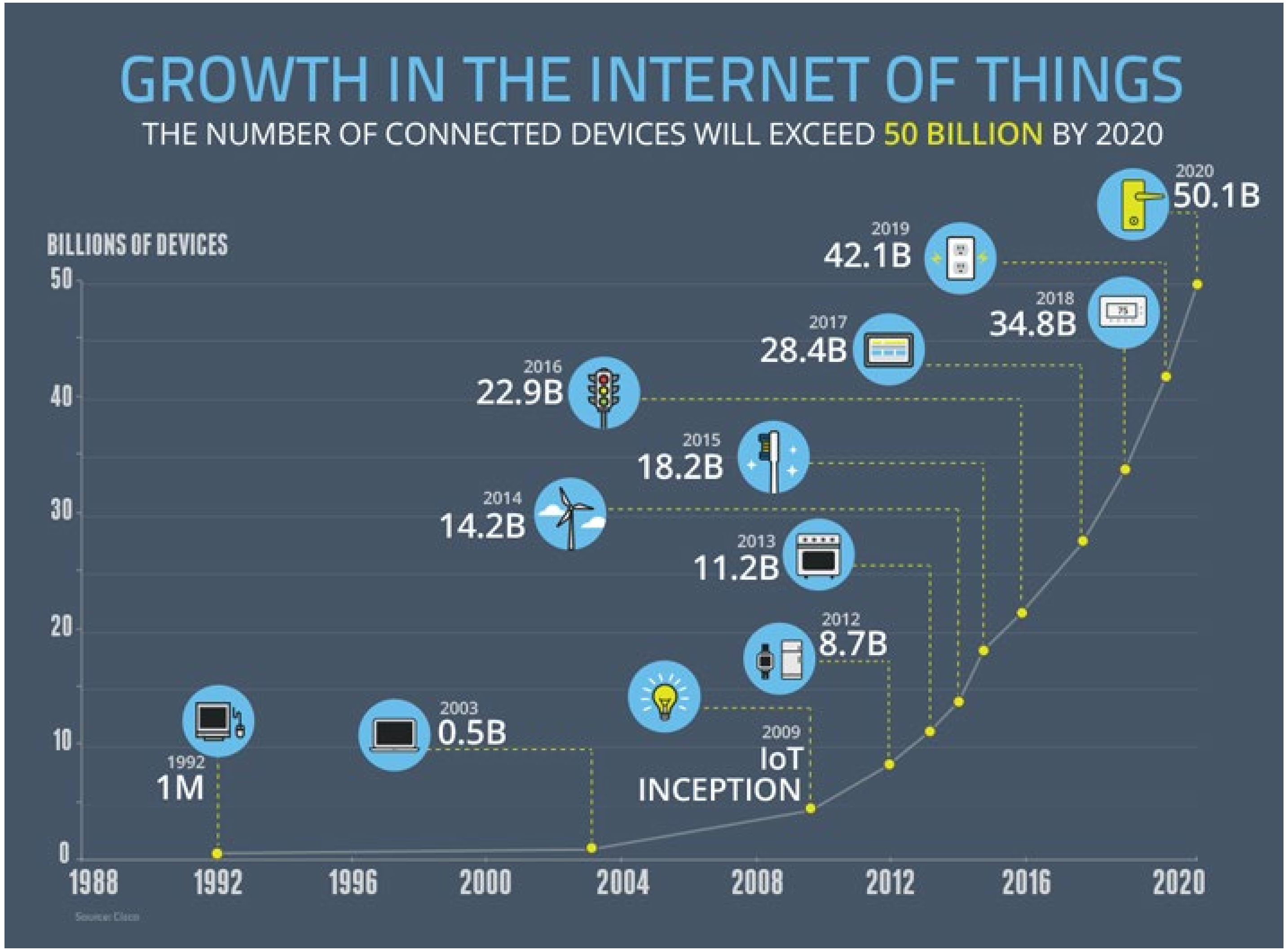
Desktop/PC → IoT





http://www.business2community.com/big-data/internet-things-iot-going-impact-business-01572401

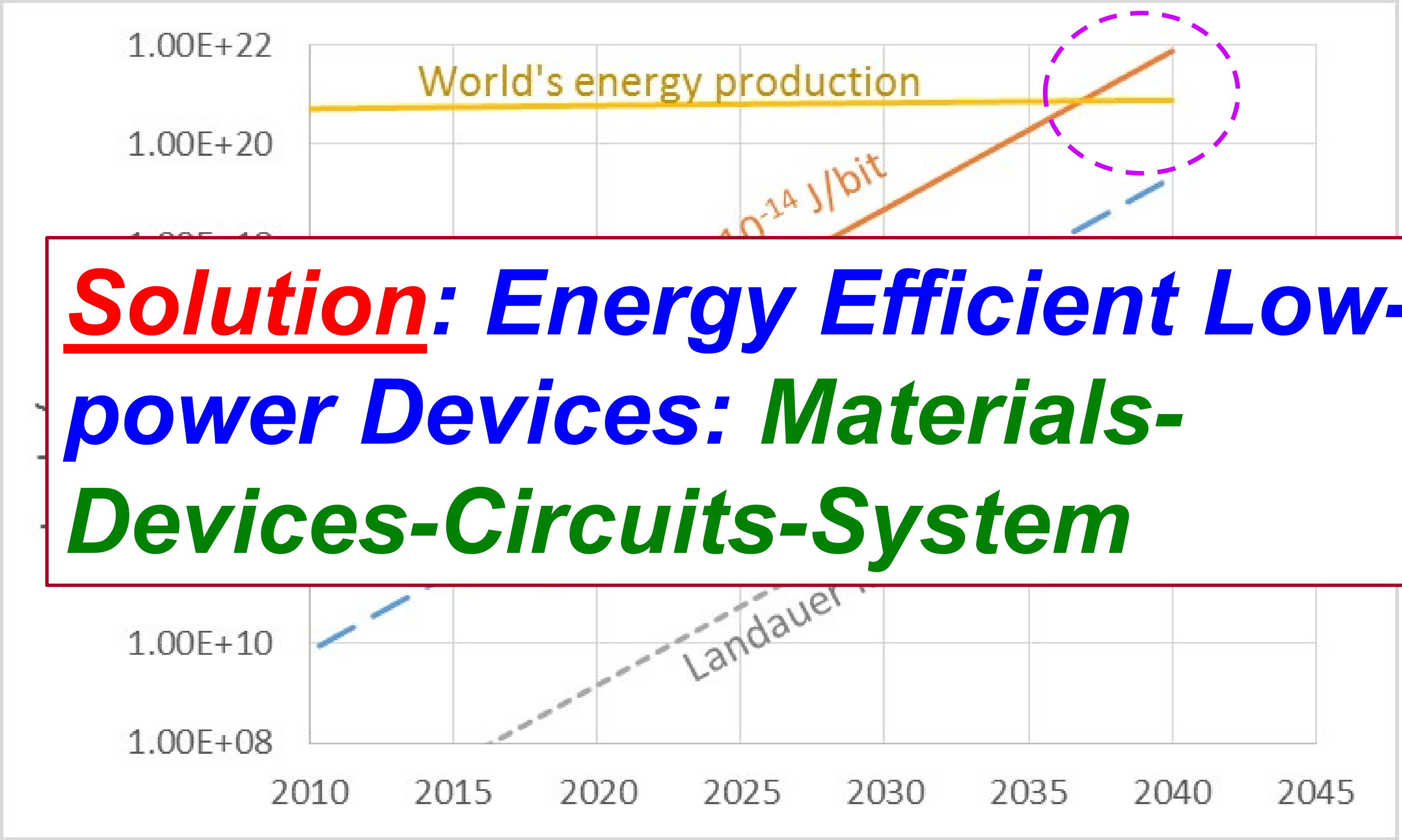
Data Explosion in IoT Era



Source: CISCO

By 2020, 50B connected devices with 2 Zeta Byte annual data traffic

Total Energy for Computing in IoT Era



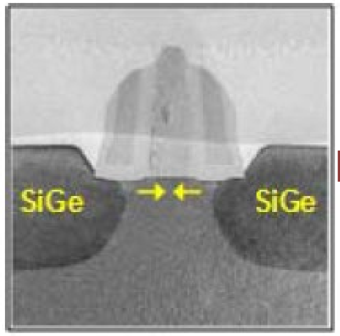
Solution: Energy Efficient Low-power Devices: Materials-Devices-Circuits-System

Source: SIA

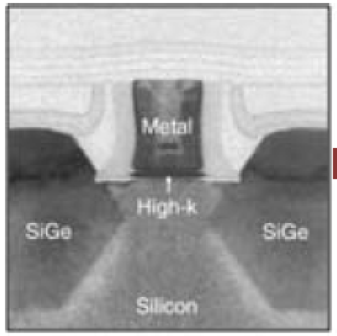
By 2040, World's energy production is less than energy needed for computing !

Conventional CMOS Technology: Scaling & Architecture

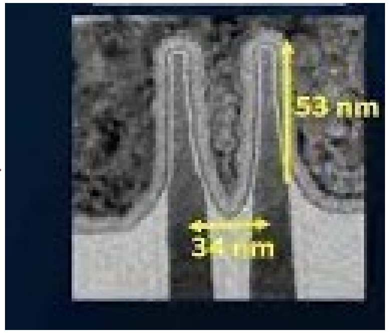
Source: IEEE Spectrum



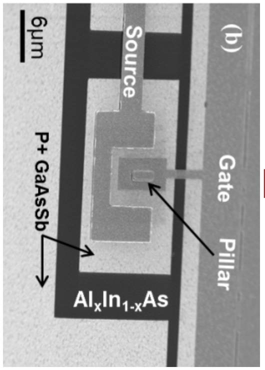
1st Generation Strained Silicon 65nm



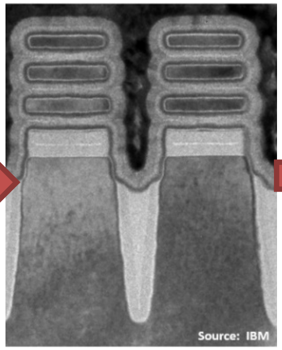
1st Generation High-κ Metal Gate 45 nm node

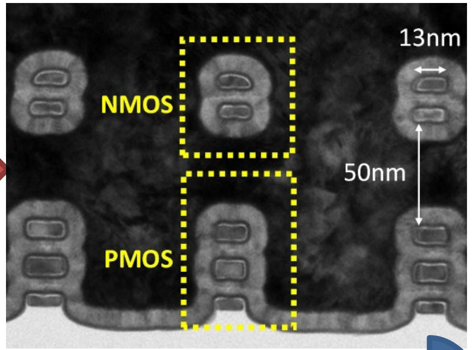


FinFET/ Trigate 22nm and below



TFET





Nanosheet-FET Gate-all-around (GAA)

Source: Intel

Alternate channel CMOS (non-Si)

Alternate channel NSFET (non-Si)

Non-Si based CMOS??

Why look beyond Si CMOS?

1. Scaling Limit : Quantum effects
2. Limited mobility : Supply and power leakage
3. Photonic integration and light source is a challenge
4. Diminishing ROI & yield (?)

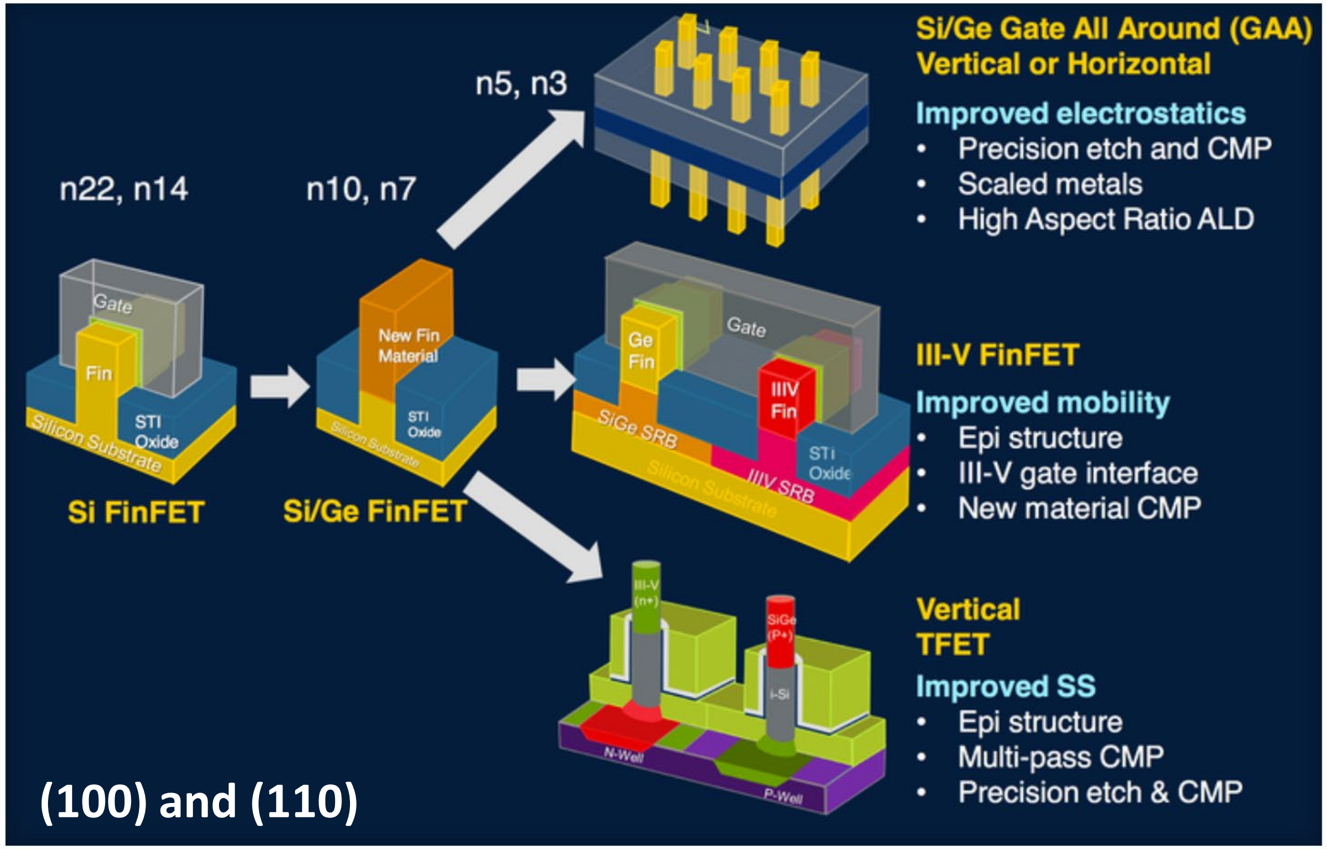
Topic -1 of discussion TODAY

III-V and Ge for High Performance Computing

IBM-spends-3-billion-to-push-the-far-future-of-computer-chips

IBM

July 9, 2014 4:02 PM



Applied Materials, which manufactures chipmaking tools, envisions chips made with a 3nm ("n3") manufacturing process.

http://www.cnet.com/news/ibm-spends-3-billion-to-push-the-far-future-of-computer-chips/

Hudait *et al*: "Extreme high mobility CMOS logic"
Patent # *9548363* (2017); *8802517* (2014); *8518768* (2013); *8183556* (2012)

What Should non-Si CMOS Accomplish to Reach the Market?

Speed
- Operating Frequency > 6GHz
- Computation rate

Density
- Large number of gates per die
- Vertical integration
- Minimize Cost

Power
- Low static current
- Low dynamic current
- Low voltage (V_{DD} and V_{TH})

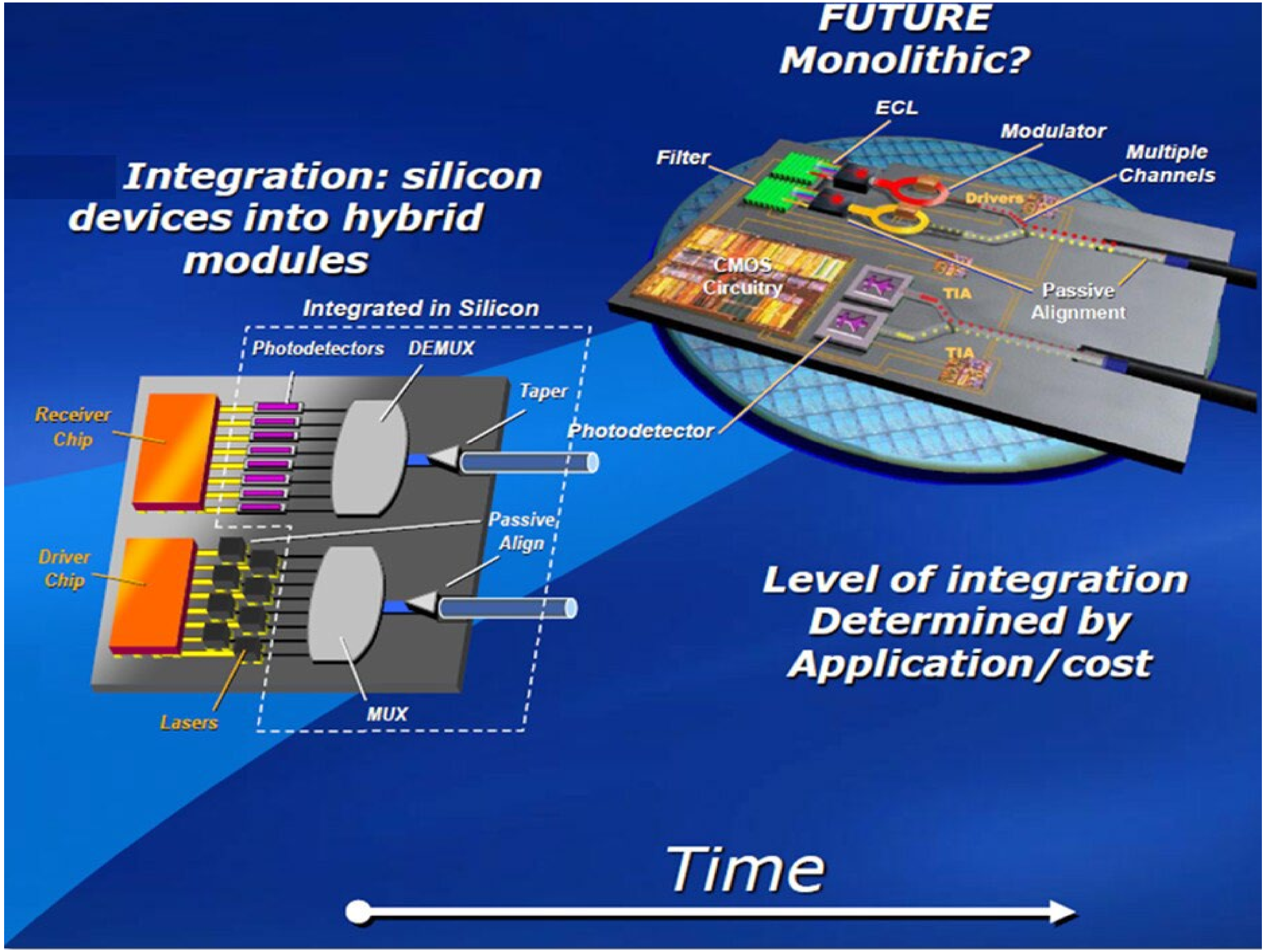
Scalability
- Moore's Law
- Feature size
- ROI on scaling

Compatible with Si
- Leverage existing fab
- Leverage existing tech

Reliability
- Die-to-Die yield
- Gate-to-Gate reliability

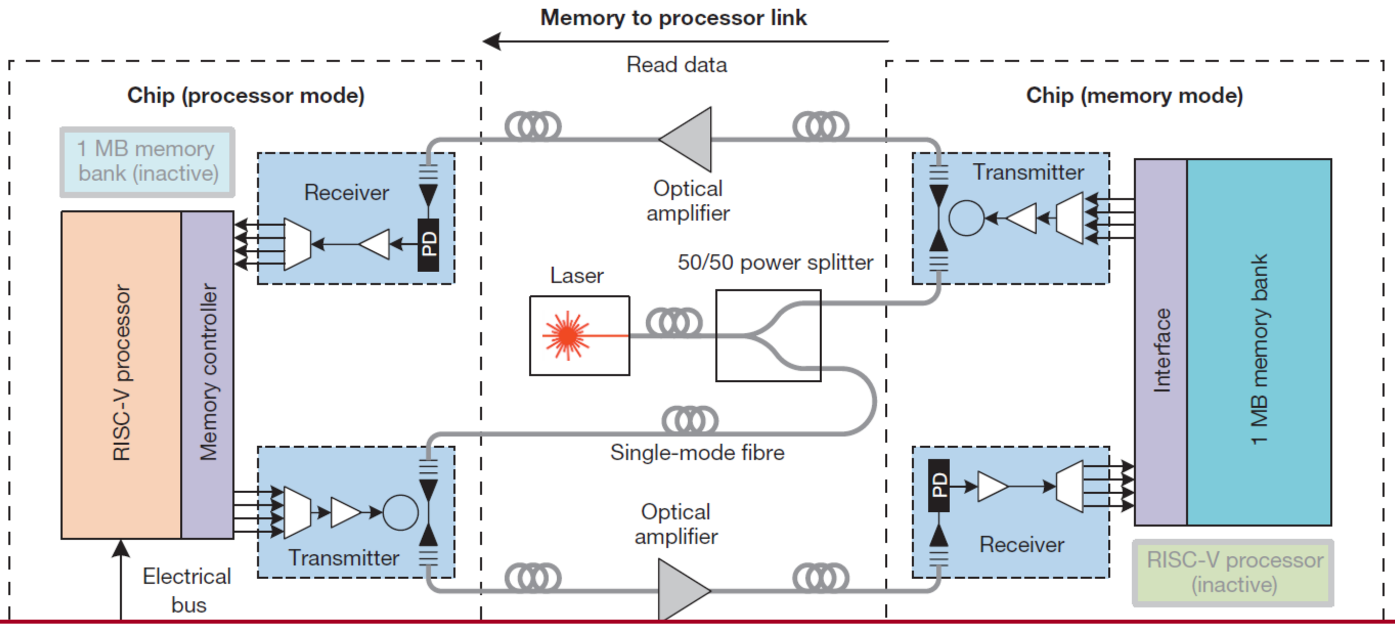
Compatible with Photonics
- Beyond electronics
- Opto
- Quantum Tech.

Artistic view of Monolithic Optical Interconnects



Source: Intel Photonics Group

Chip-scale Electronic-Photonic Systems: Powerful Computer !



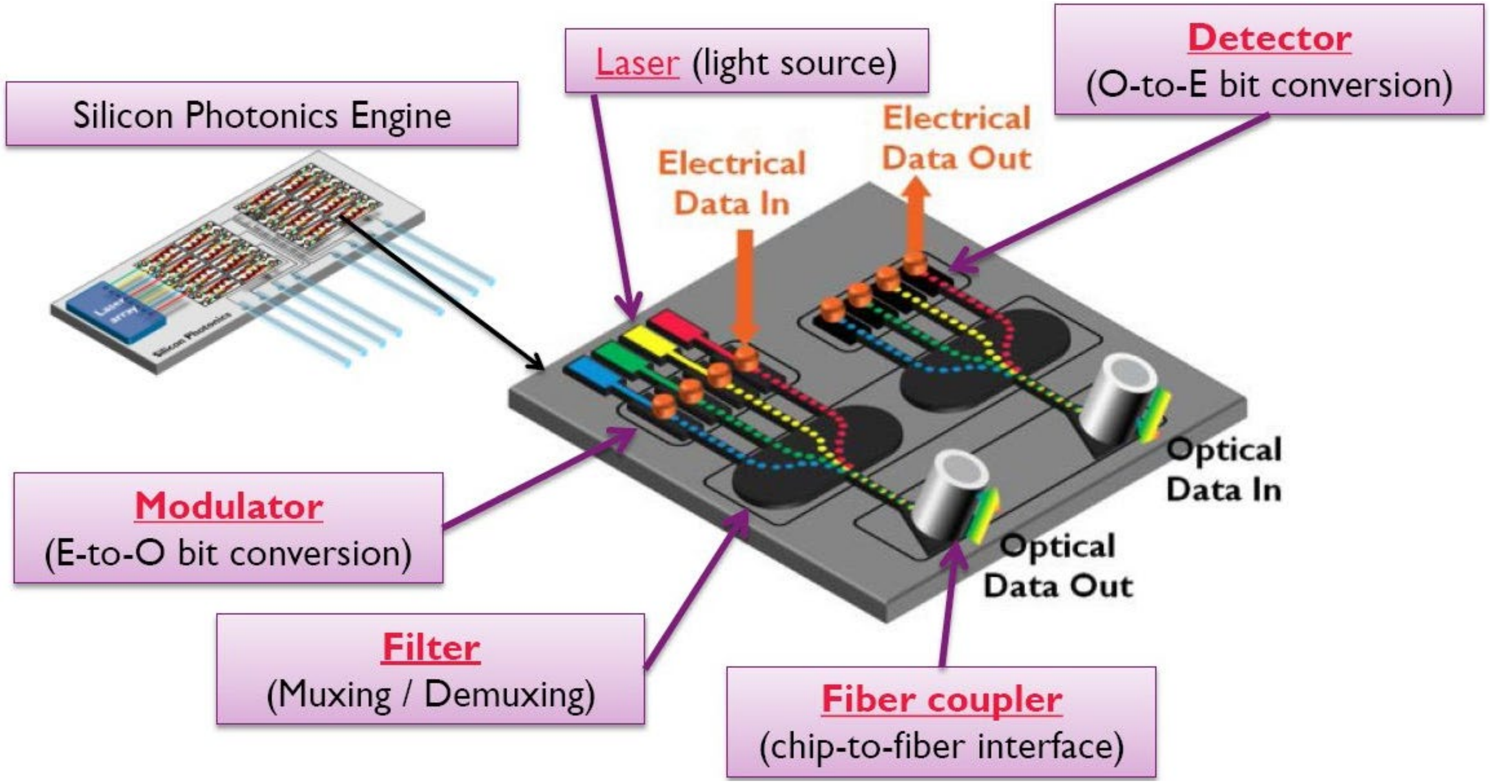
Solution: Monolithically/Heterogeneously Integrated Tunable Laser

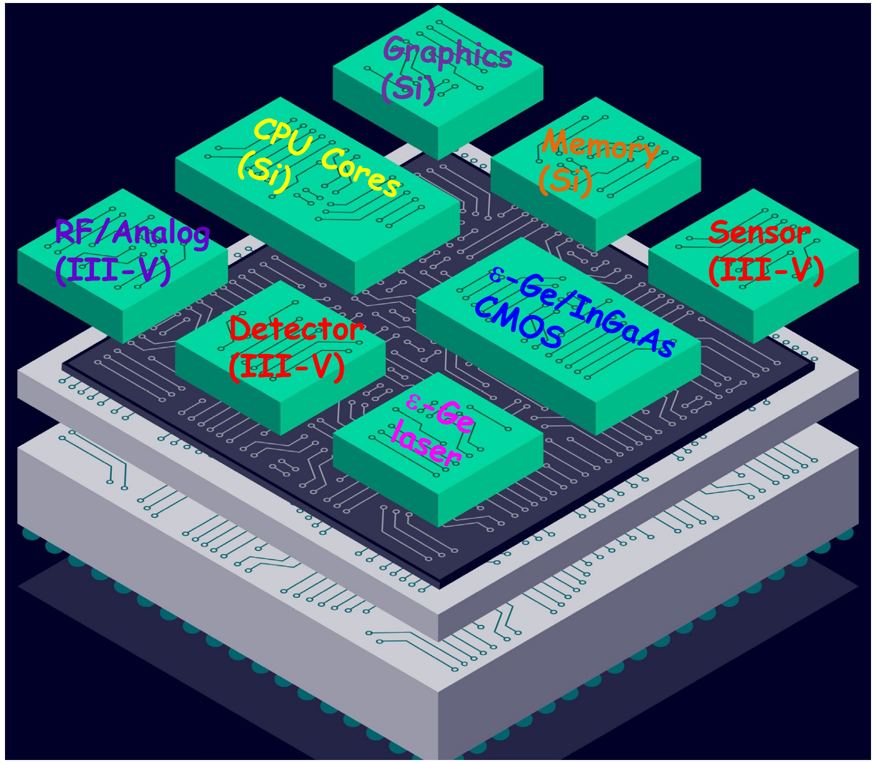
- **Tea-pot was generated using the above fabricated microprocessor, but *the laser was externally coupled to the processor*.**

Topic -2 of discussion TODAY

Chen Sun *et al*, "Single-chip microprocessor that communicates directly using light", *Nature* 528, 534, 24/31 December 2015.

Futuristic CMOS-compatible Intra-chip Photonics





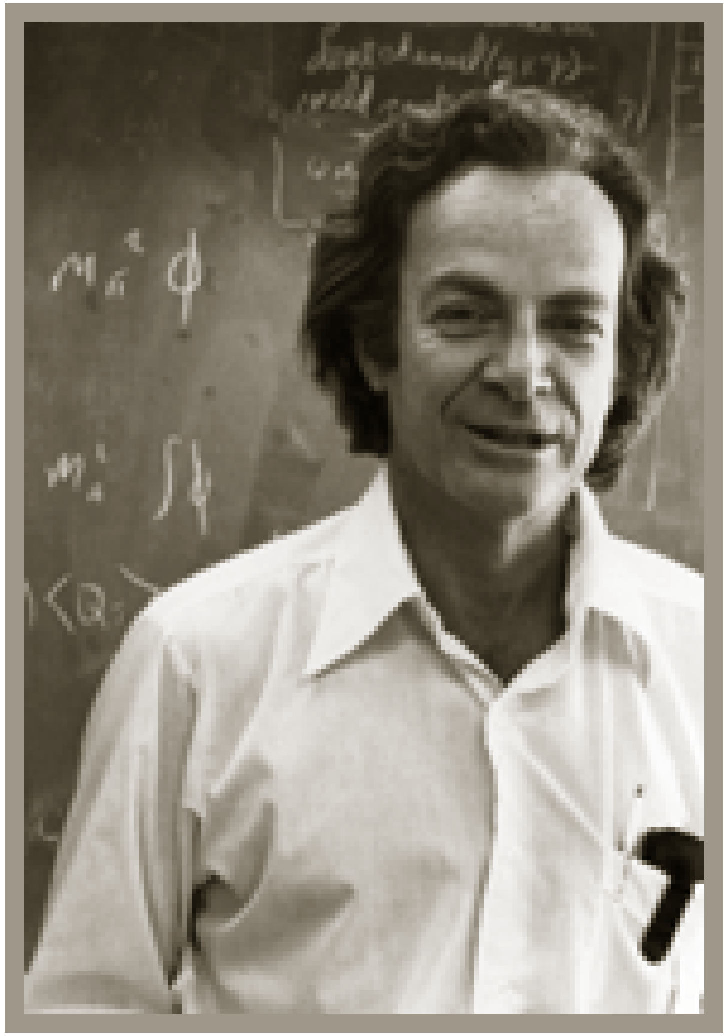
Courtesy CEA-Leti

➤ Aims to achieve Group-IV based devices compatible to Si photonics

Topic -2 of discussion TODAY

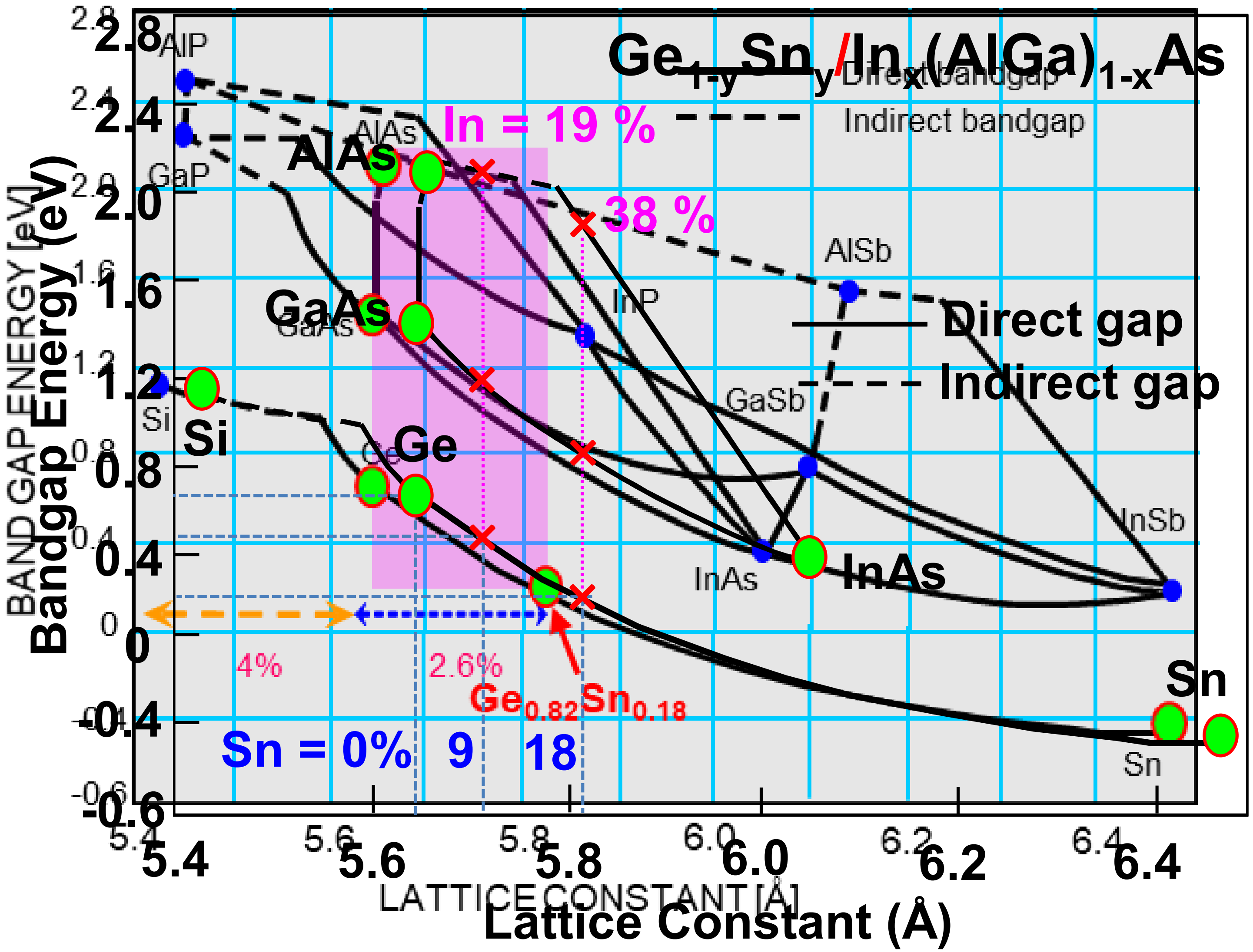
Julien Happich, "CMOS-compatible intra-chip photonics brings new class of sensors", http://www.analog-eetimes.com/news/cmos-compatible-intra-chip-photonicsbrings-new-class-sensors. *EE Times*, October 15, 2013.

Plenty of Room at the Bottom?



- In 1959, Richard Feynman delivered a talk titled "*Plenty of Room at the Bottom*" at the American Physical Society.
- Feynman envisioned the <u>ability to manipulate things at the atomic level</u>, leading to:
  - <u>New Materials</u>
  - Miniaturized Motors
  - Miniaturized Computers

Selection of non-Si Materials for CMOS and Optoelectronics



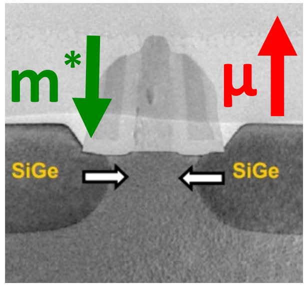
- InSb or InGaAs on Si has large lattice mismatch → needs lattice adapter to mitigate defects and dislocations

Electronics

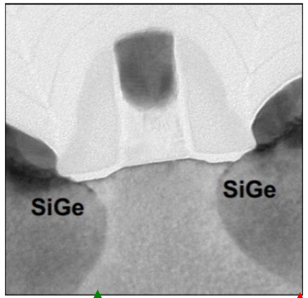
TFET & FinFET (Topic-1a, 1b)

Scaling of Si Transistor: Thermal Challenges

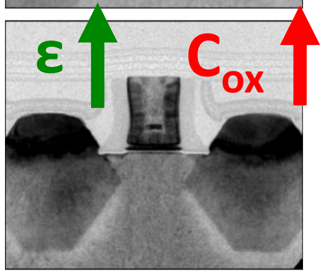
90nm
2003
Ghani, IEDM 03



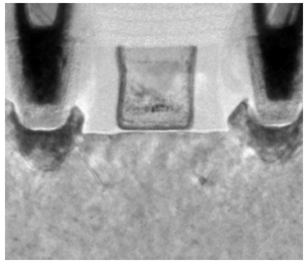
65nm
2005
Tyagi, IEDM 05

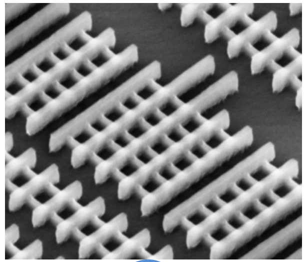


45nm
2007
Mistry, IEDM 07

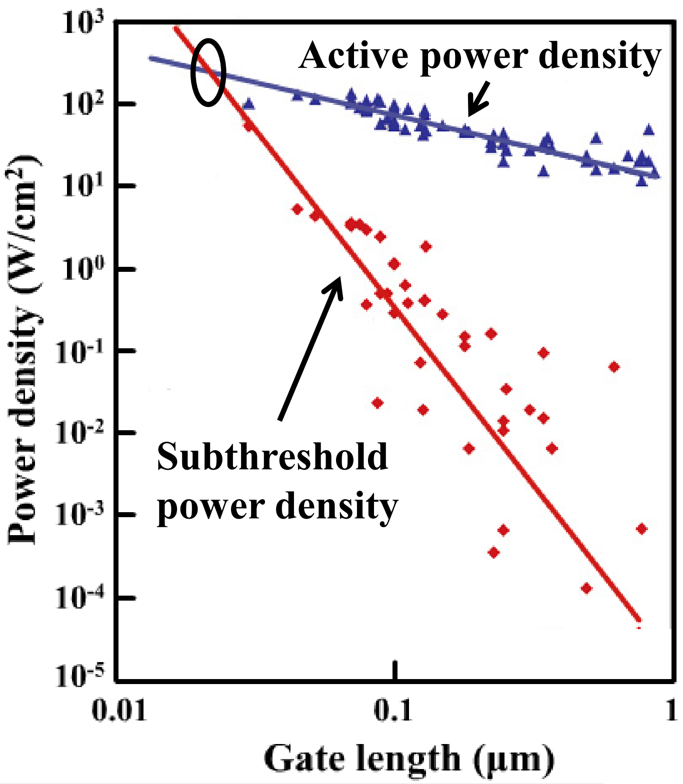


32nm
2009
Packan, IEDM 07

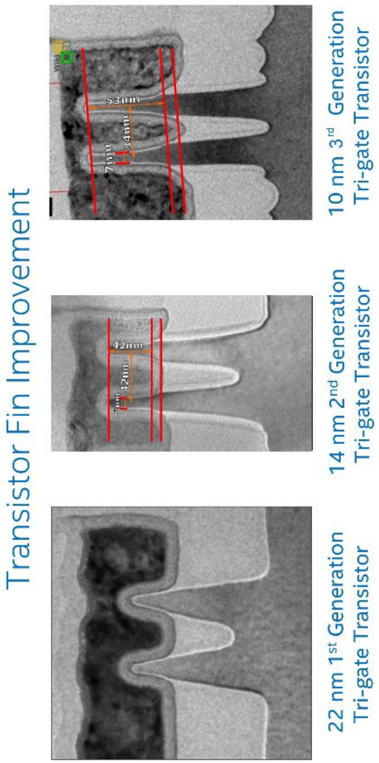




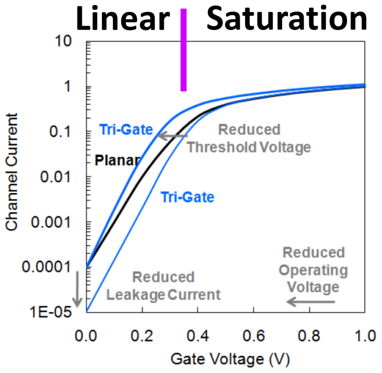
22nm
2011
Intel



E. J. Nowak, IBM *J. Res. & Dev.*, **46**, 169 (2002)



Mobile Devices: Power Consumption

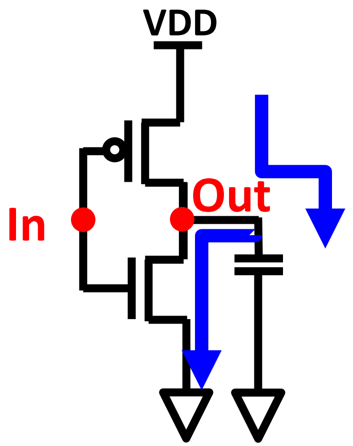


$$P = n(\alpha C V_{DD}^2 f + I_{OFF} V_{DD} + I_{sc} V_{DD})$$

Active Power | Leakage Power | Leakage Power

P: Total Power Consumption
n: Number of Transistors
C: Load Capacitance
V_{DD}: Supply Voltage
f: Operation Frequency
I_{OFF}: OFF-state Leakage Current
α : Activity factor
I_{SC}: OFF-state Current when both P- and N-MOS are ON

Inverter



Low Power Consumption → V_{DD}, I_{off} ⬇

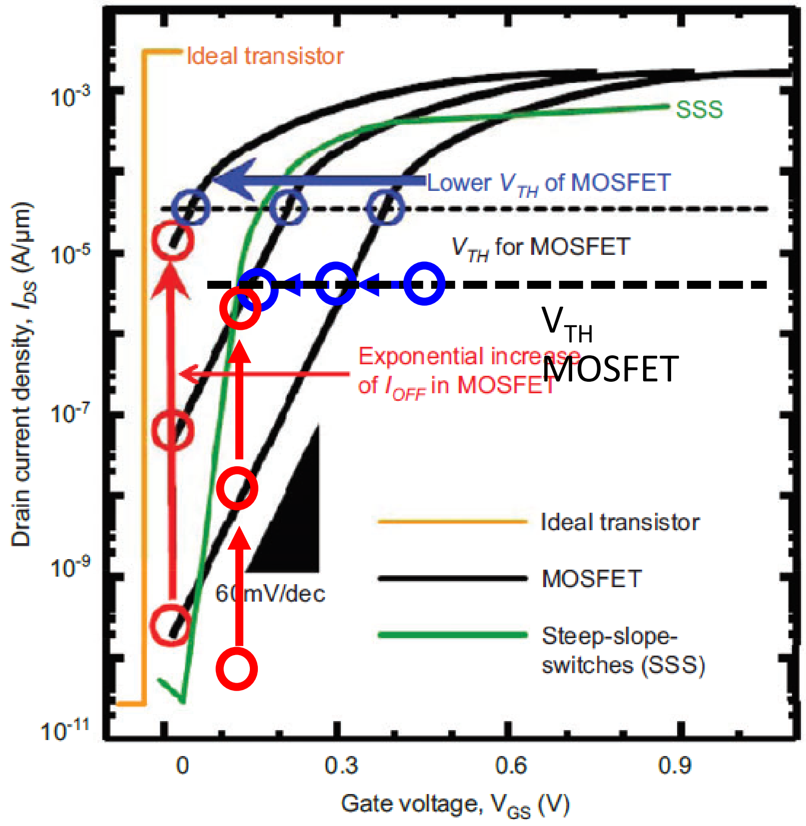
$$I_{ON} = \frac{W \mu C_{OX}}{2L}(V_{DD} - V_{TH})^2$$

Need to be scaled together

I_{ON}: ON-state current
W: Gate Width
C_{OX}: Oxide Capacitance
μ: Carrier Mobility
L: Gate Length
V_{TH}: Threshold Voltage

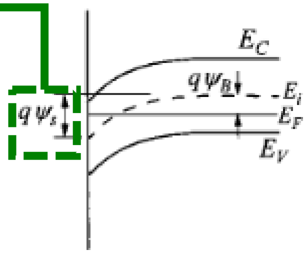
High Performance (High I_{ON}) → V_{TH} ⬇

Lower Limit of MOSFET Subthreshold Slope



Zhu and Hudait, *Nano Technology Rev*. **2**, 637 (2013)

$$SS = ln(10)\frac{dV_G}{d(q\psi_s/KT)}$$



$$\frac{dV_G}{d\psi_s} = \frac{kT}{q}\ln(10)\left(1+\frac{C_D}{C_{OX}}\right)$$

$$SS \rightarrow \frac{kT}{q}\ln(10) \quad [\mathrm{mV/dec}]$$

$$I_{OFF} = I_{DS}\cdot 10^{-V_{TH}/SS}$$

New FET architectures need to satisfy:

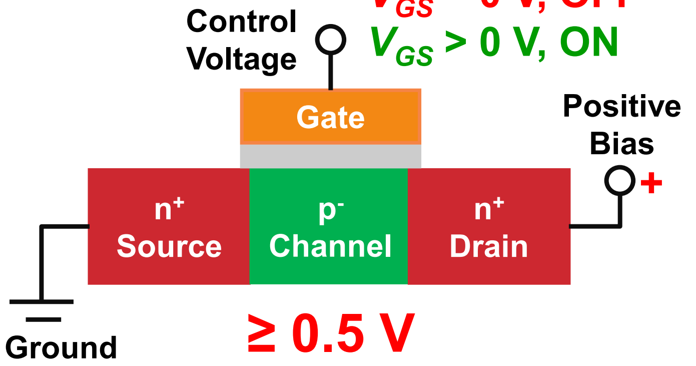
1) Steep *SS* characteristics
2) Low V_{TH}
3) Low OFF-state current

Tunnel FETs can satisfy these requirements!

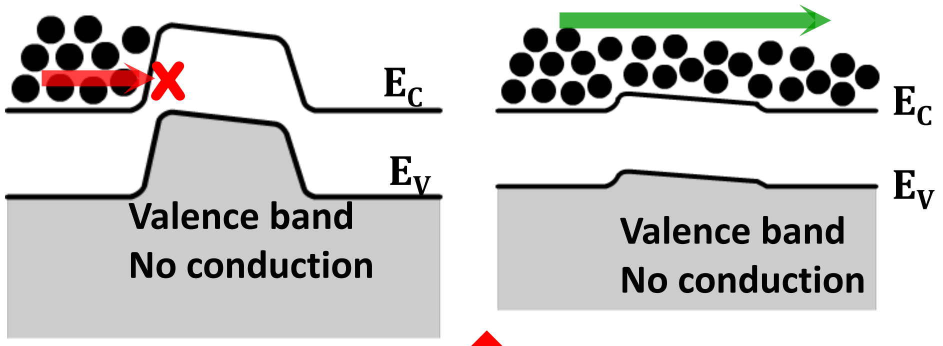
Comparison Between MOSFETs and Tunnel FETs

N-MOSFET

V_{GS} = 0 V, OFF
V_{GS} > 0 V, ON



≥ 0.5 V



OFF

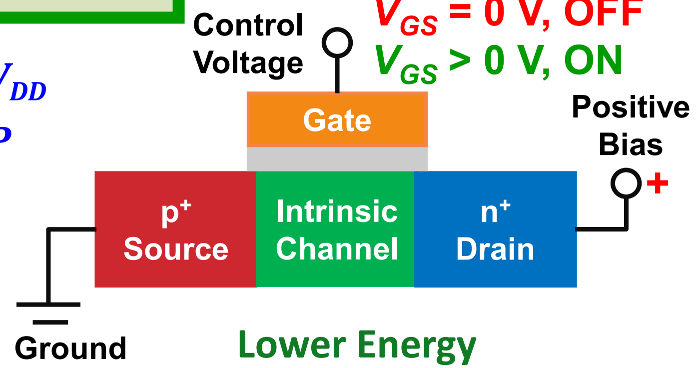
ON

Thermionic Emission

N-TFET

↓ V_{DD}
↓ P

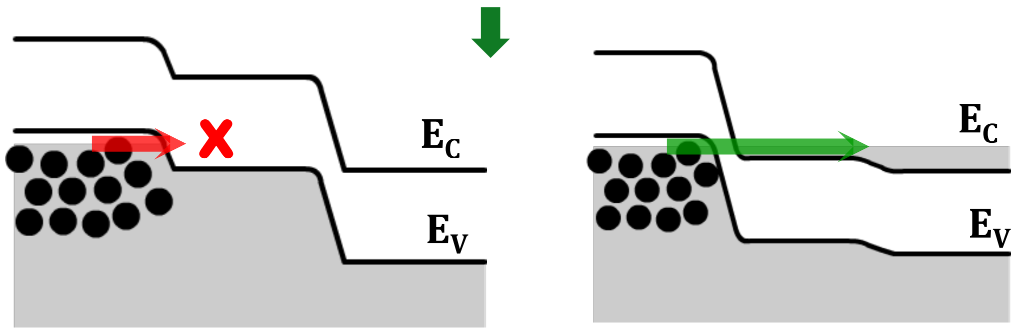
V_{GS} = 0 V, OFF
V_{GS} > 0 V, ON



Lower Energy
Lower Voltage

≤ 0.3 V

Band-to-band Tunneling



OFF

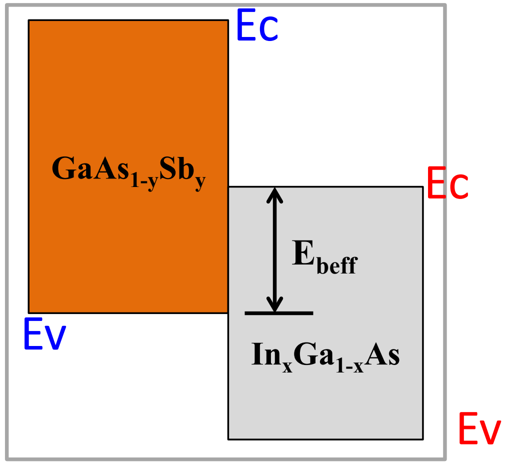
ON

Tunnel Transistor (<0.3V): Band Alignment Engineering

Tunneling distance λ

$$T_{WKB} \approx \exp\left(-\frac{4\lambda\sqrt{2m^{*}}E_G^{3/2}}{3q\hbar(\Delta\Phi + E_G)}\right)$$

Sze SM, Physics of Semiconductor Devices, 3rd. Ed.



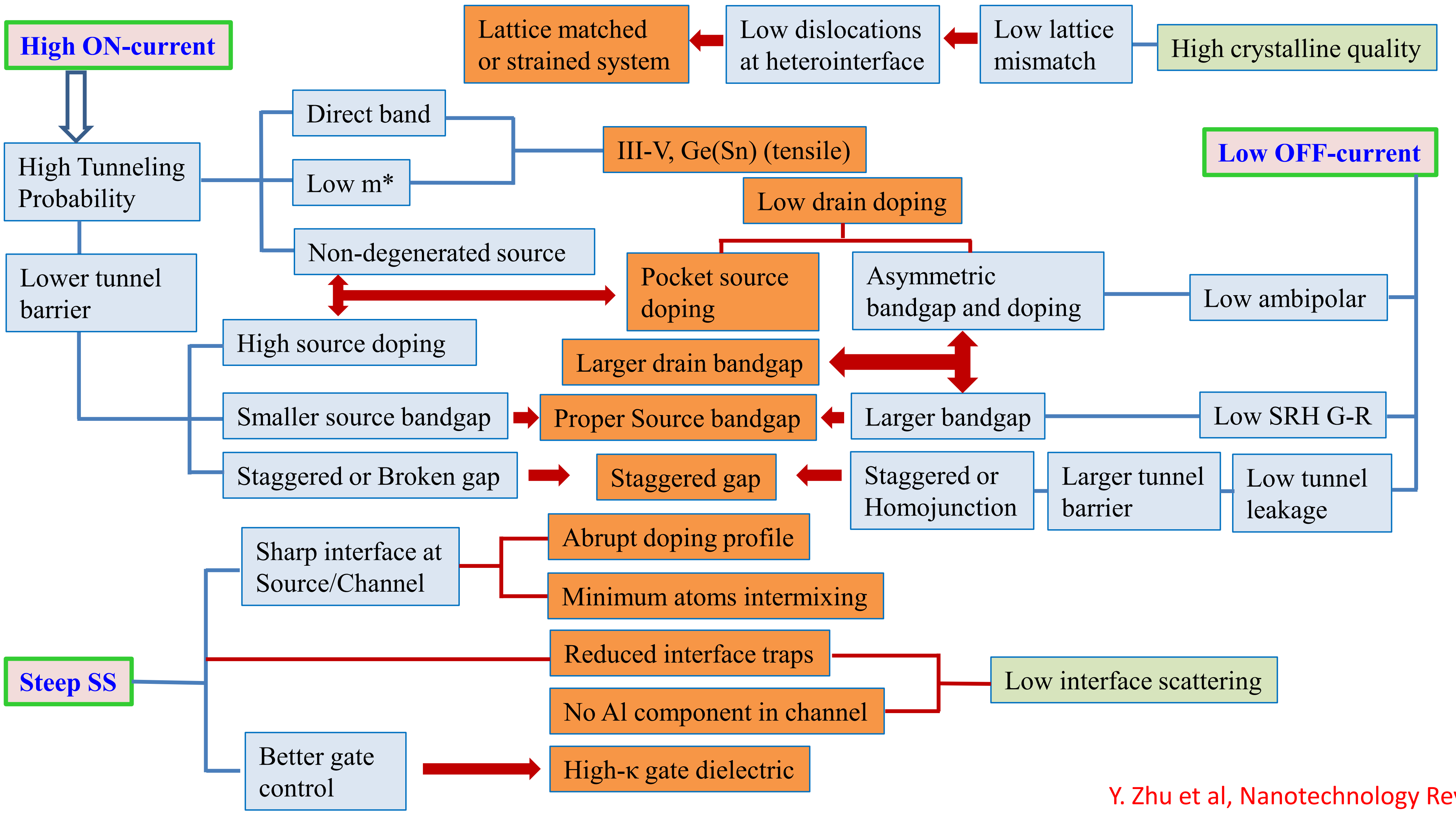
Design Criteria and Materials Selection:

1) **Low λ → Abrupt, defect-free tunneling interface.**
2) **Low m^* → Low E_G or strained materials.**
3) **Low E_{beff} → Heterojunction tunneling interface and strained materials.**

Tensile Strained Ge/InGaAs and GaAsSb/InGaAs have the potential to meet all criteria!

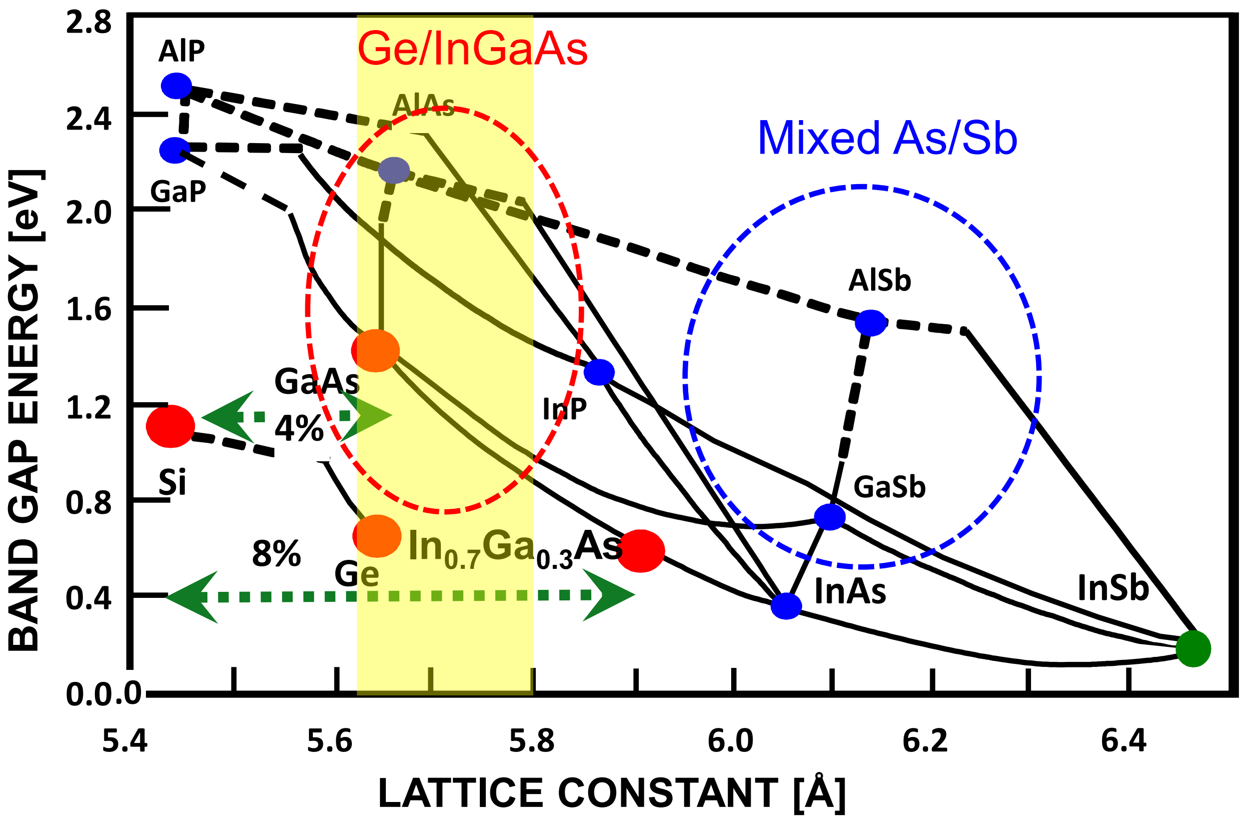
Larger tunneling distance	Reduced tunneling distance	Zero tunneling distance

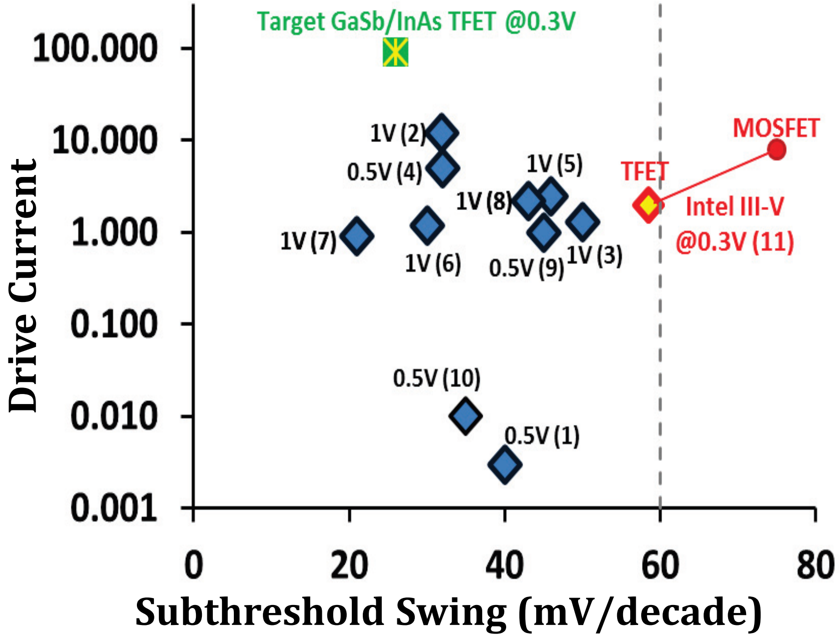
Comprehensive Consideration of a TFET Design



Y. Zhu et al, Nanotechnology Review (2013)

Tunnel Transistor (TFET) Materials Selection



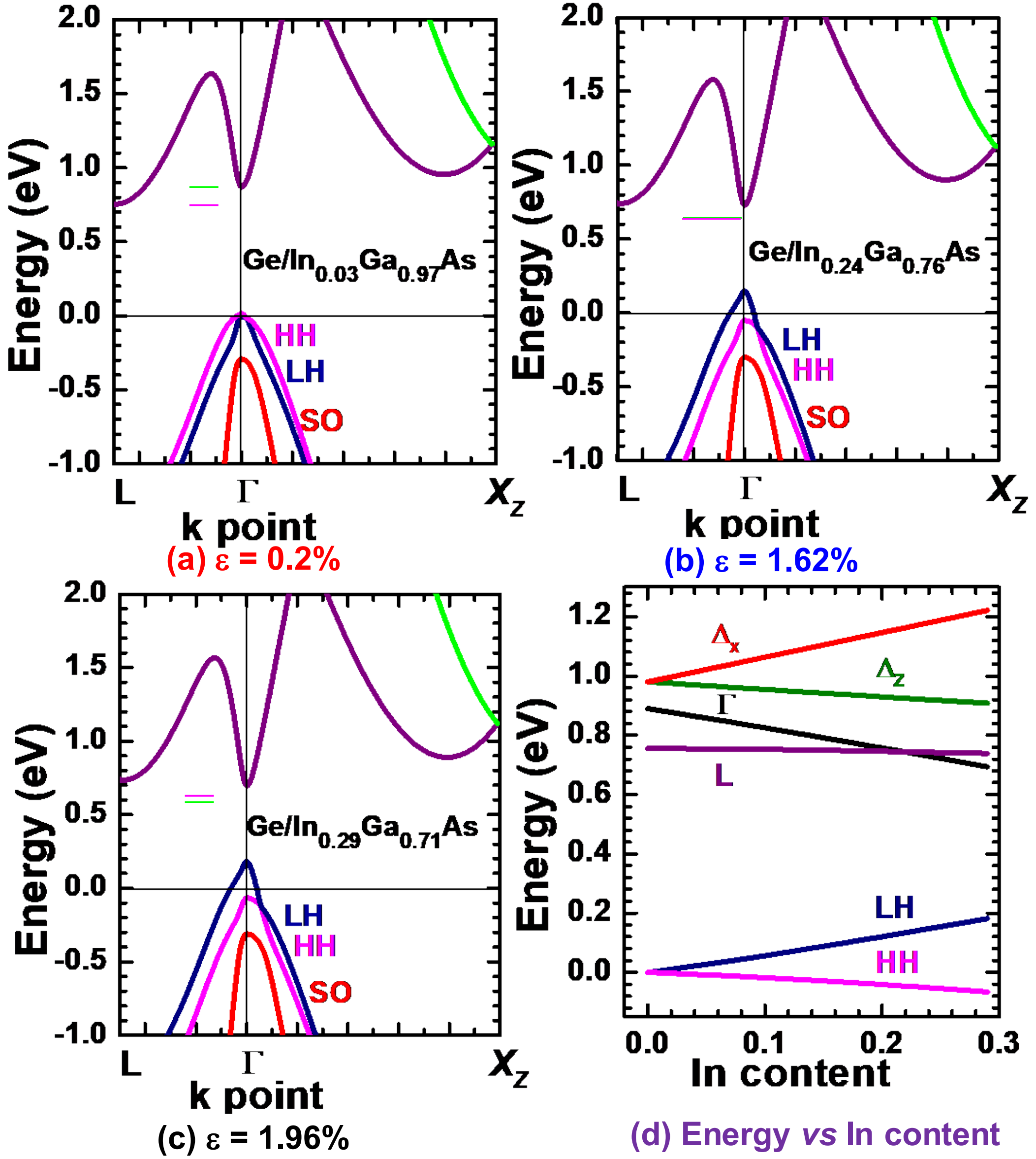


Ian A Yong et al., *IEDM*, 22.1 (2015) (Intel)

Previous: InAs, InGaAs, Si, Ge, GaAs (Homojunction); $GaAs_{1-y}Sb_y/In_xGa_{1-x}As$ (Heterojunction)

New: Tensile Ge/$In_xGa_{1-x}As$ (Heterojunction)

Tensile Strain Engineering of Ge for TEFT and Photonics
(Strain & Bandgap Engineering)



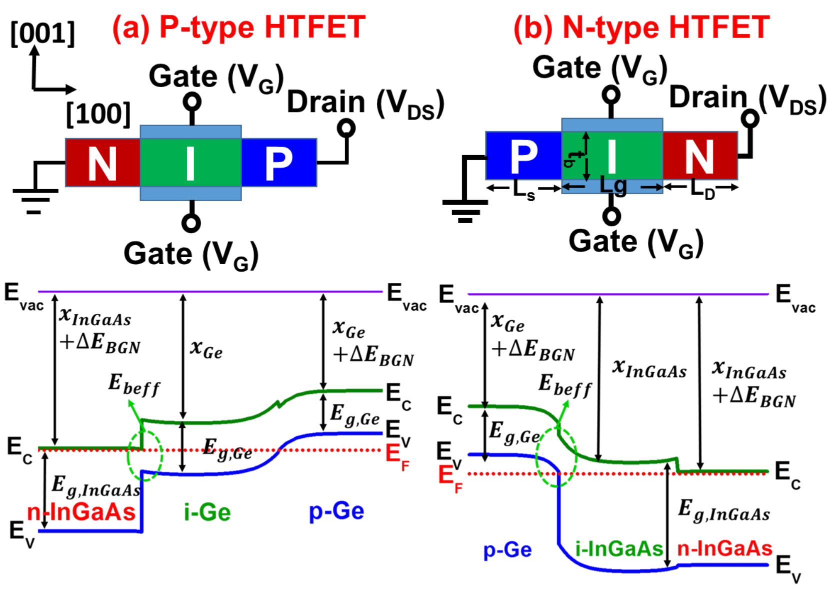
- Aims to achieve direct bandgap Ge by strain or alloying with Sn (i.e,GeSn)

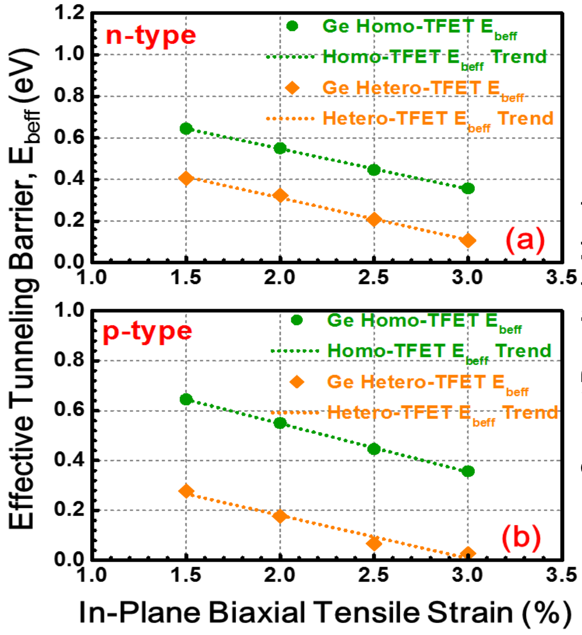
Benefits of tensile Ge for TFETs:

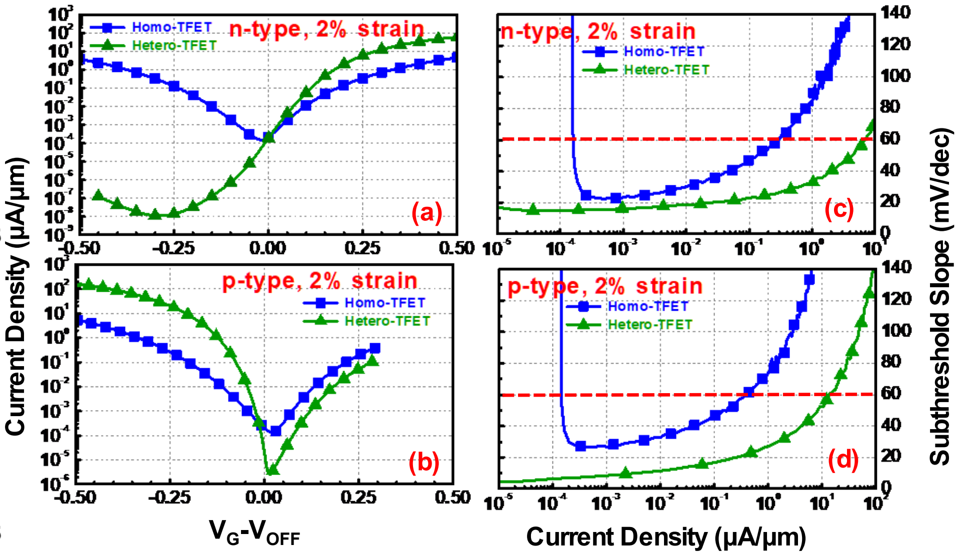
1) ↓E_g^{Ge} → ↑T_{WKB} → ↑I_{ON}
2) Indirect E_g to direct E_g → ↑T_{WKB} → ↑I_{ON}
3) Tunable direct E_g → Ge Laser

Hudait et al, ACS Appl. Electron. Mater. (2021)

Theoretical Understanding of Ge/InGaAs TFET Performance







Structural models and simulated schematic band diagrams

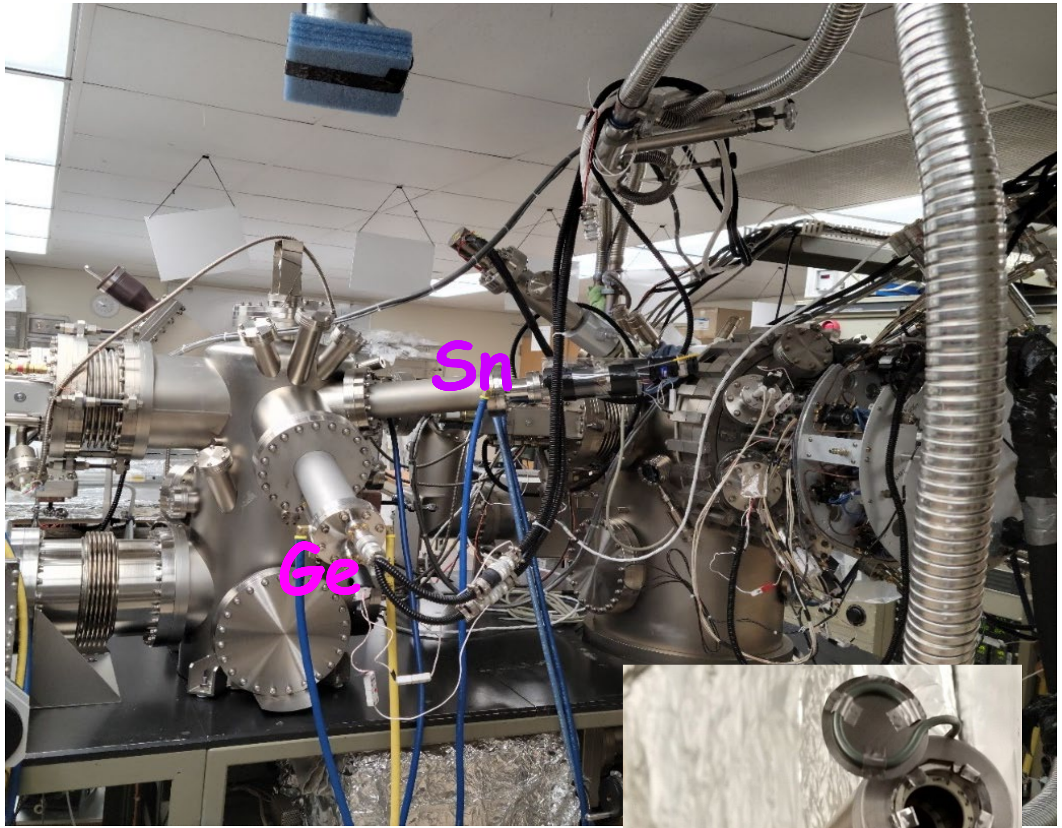
Strain-induced reduction of the E_{beff}: Simulation

Current-voltage and subthreshold swing characteristics

- Modeling work suggests significant advantage of Ge/InGaAs TFETs than GaAsSb/InGaAs system
- Developed a compact model with the experimental results as a function of strain in Ge for both n- and p-channel TFETs

Liu, Clavel, Hudait, *IEEE TED (2015).*

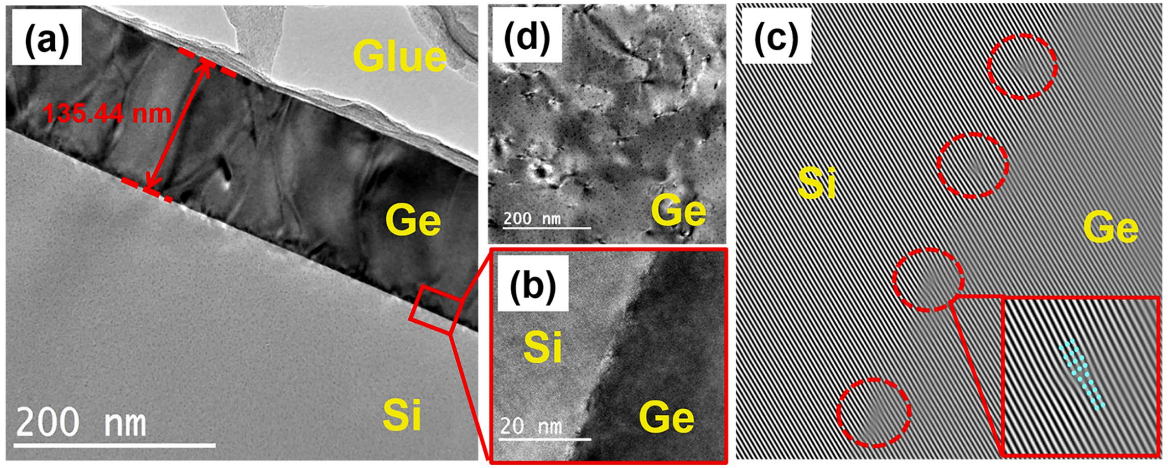
Dual Chamber MBE for III-V and Ge(Sn) @ ADSEL



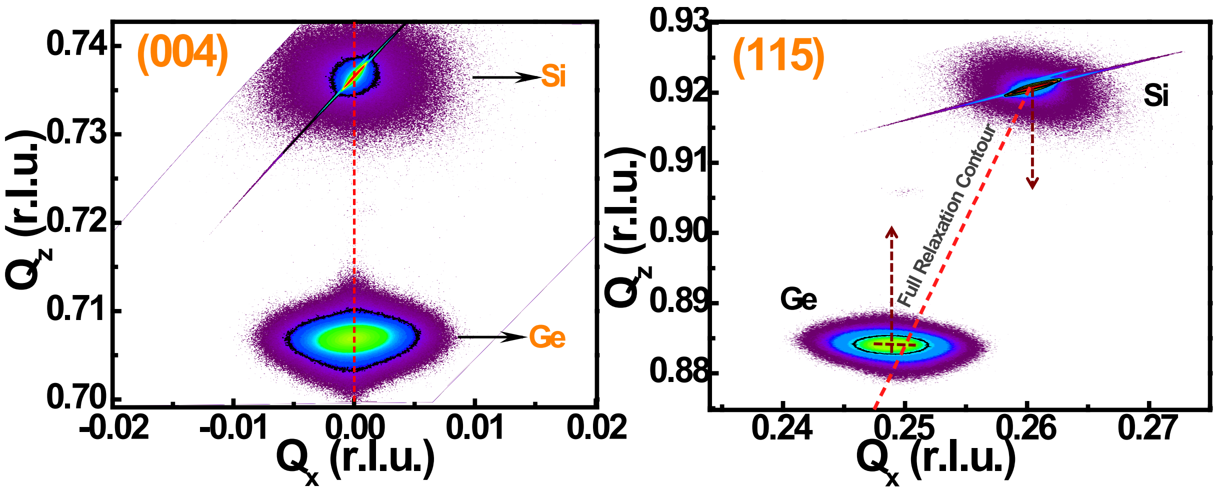
- No restriction for ε-Ge growth on III-V buffers
- Shallow angle Sn source restrict the amount of Sn flux → required to mount with Ge source (upward port)

Sn effusion cell

Epitaxial Ge Directly Grown on Si



(i) XTEM



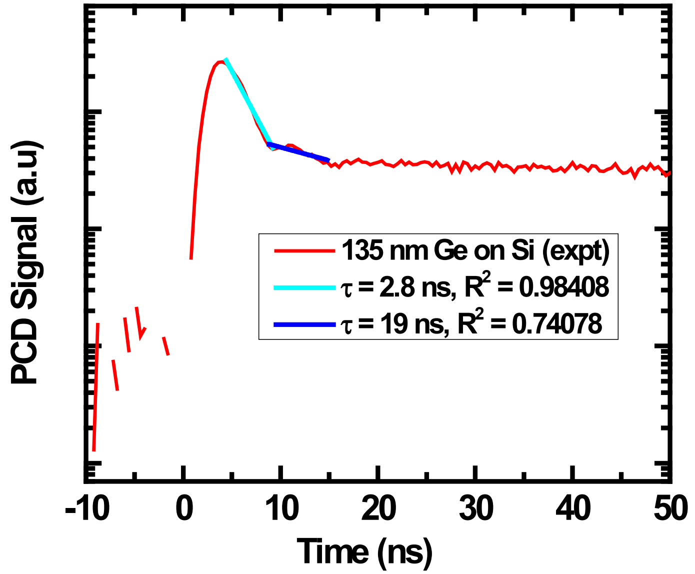
(ii) RSMs

A.Ghosh *et.al*, *AIP Adv.*, 2017, **7**, 095214.

Cross section TEM micrograph of:

i. Ge grown on Si showing interfacial misfit and threading dislocations. ☒

ii. Poor carrier lifetime ☒



(iii) Carrier recombination

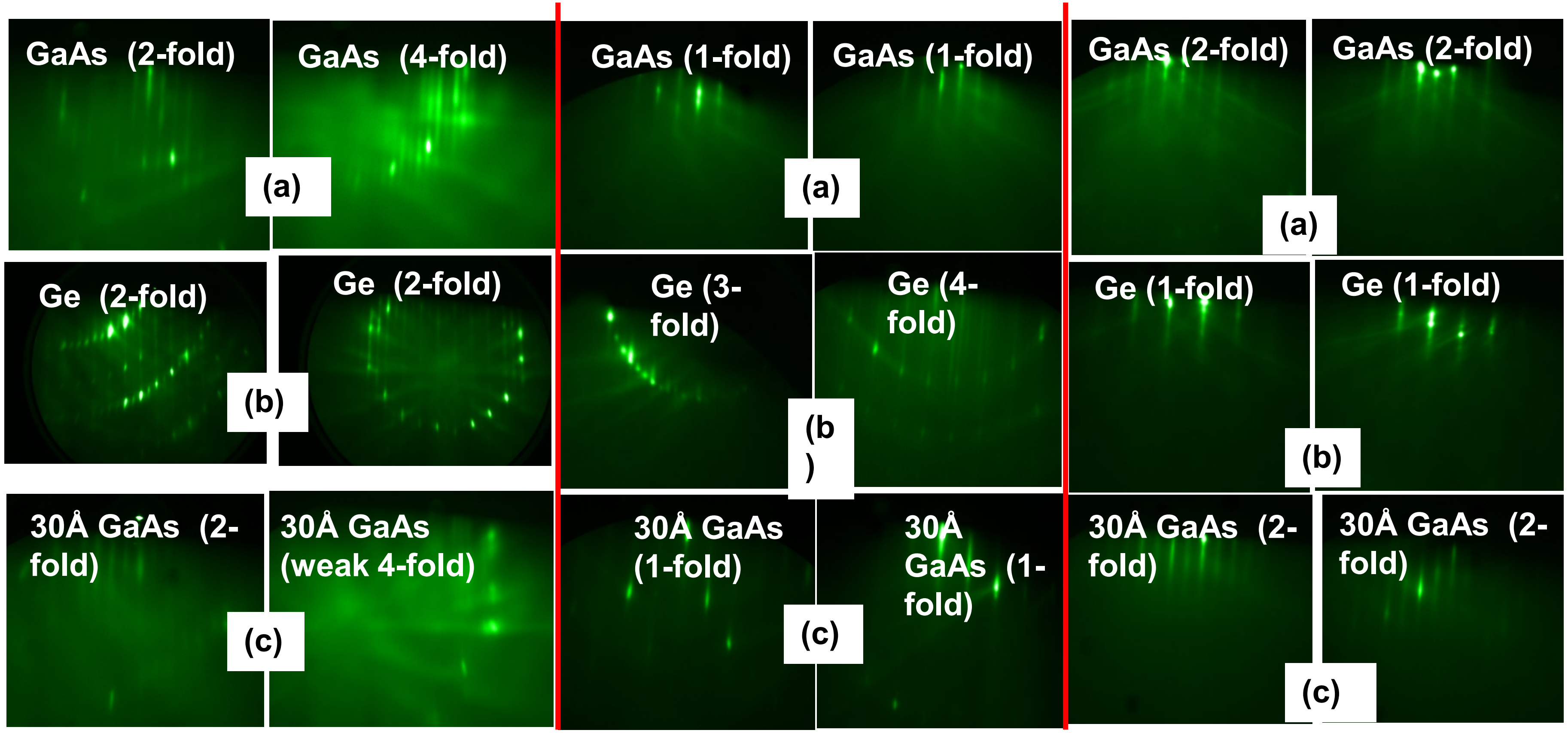
Surface Oriented un-strained Ge Layers: In-situ RHEED

(100)/2-6º GaAs | (110) GaAs | (111)A GaAs

Substrate

Ge

Top GaAs

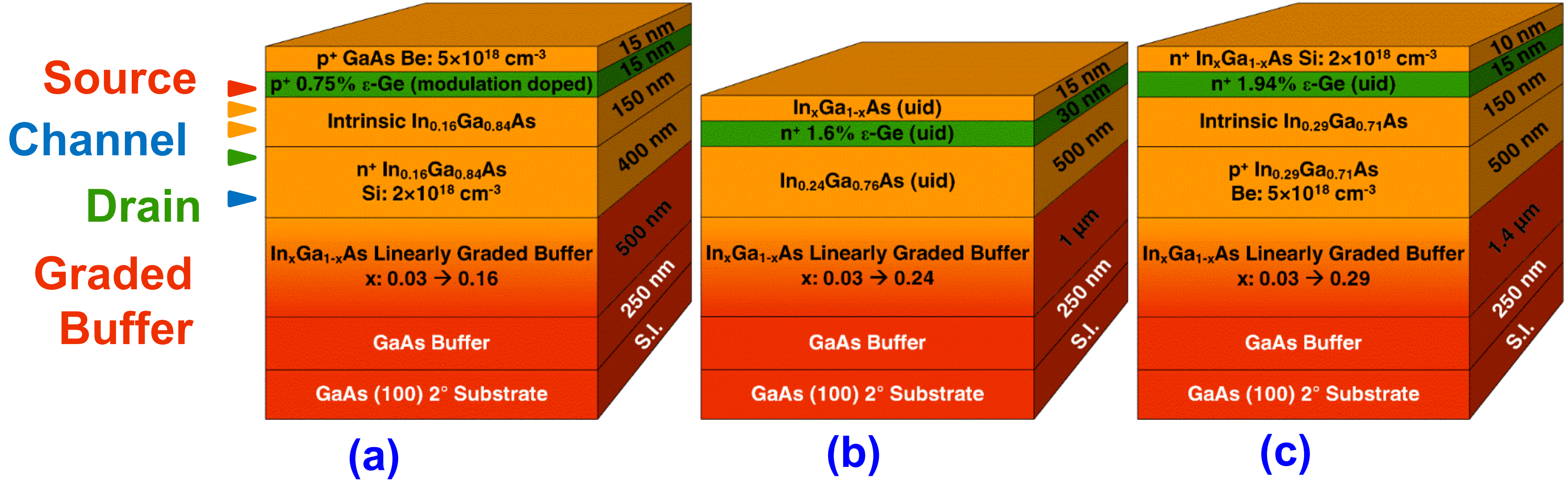


- Ge surface reconstructions were excellent !
- Each orientation exhibited different surface reconstruction

Hudait et al, JVST-B (2013)

VirginiaTech Invent the Future

Ge/InGaAs Tunnel Transistor Structures: Experimental



Separate III-V and Ge Growth Chambers: Minimize atomic interdiffusion

Tunable Strain: Modulate E_{beff}, m^* and T_{WKB} through ε and In alloy composition.

Sharp Heterointerface: Results in lower λ, higher T_{WKB} and increased I_{ON} .

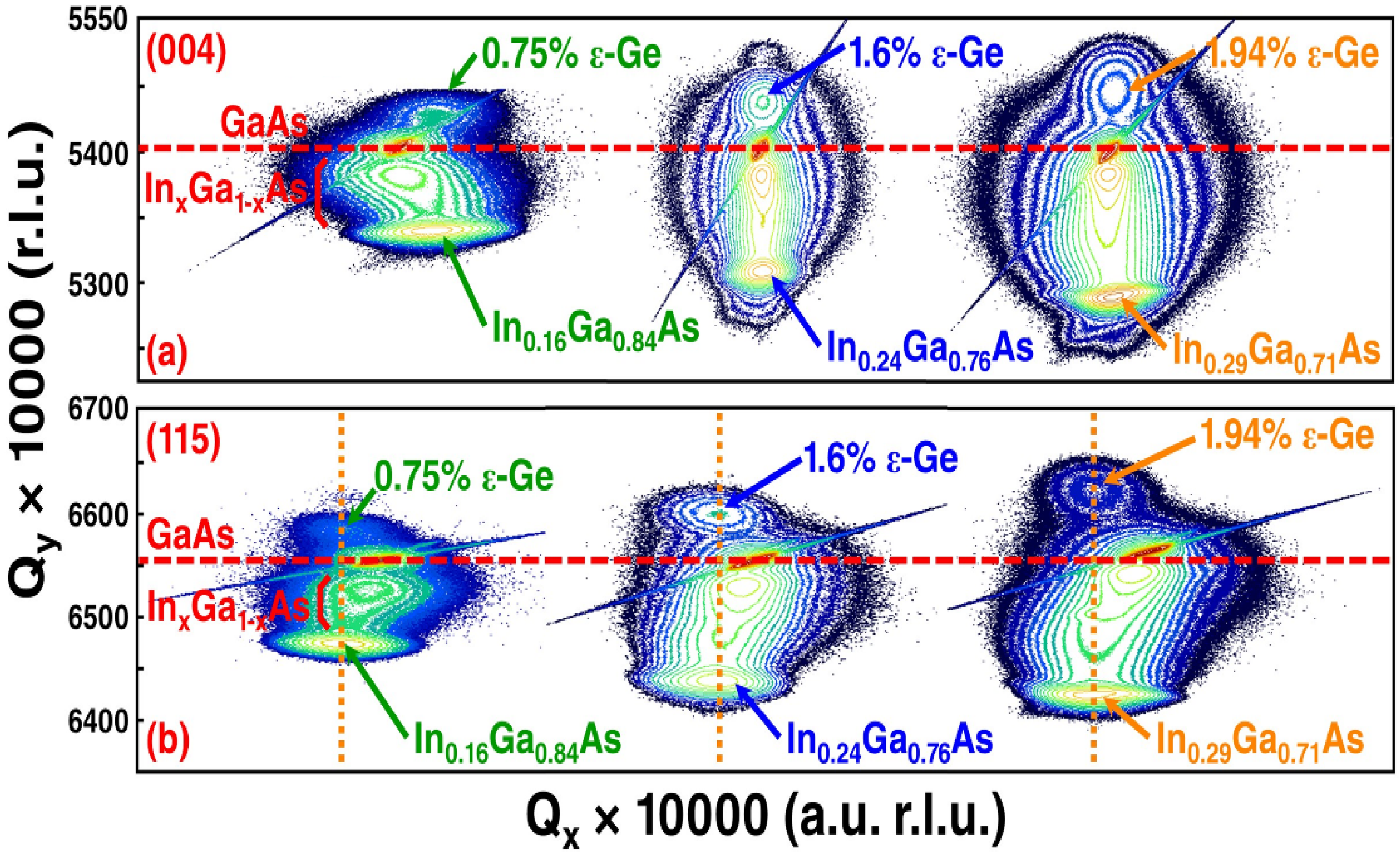
Strain Relaxation of ε-Ge/$In_xGa_{1-x}As$/GaAs: Experimental

Vertical alignment of (115) ε-Ge RLPs with InGaAs virtual substrates confirms pseudomorphic Ge epitaxy.

Minimal tilt observed in high strain samples due to full relaxation of InGaAs buffer.

ε = 0.75%, $In_{0.16}Ga_{0.84}As$
ε = 1.60%, $In_{0.24}Ga_{0.76}As$
ε = 1.94%, $In_{0.29}Ga_{0.71}As$

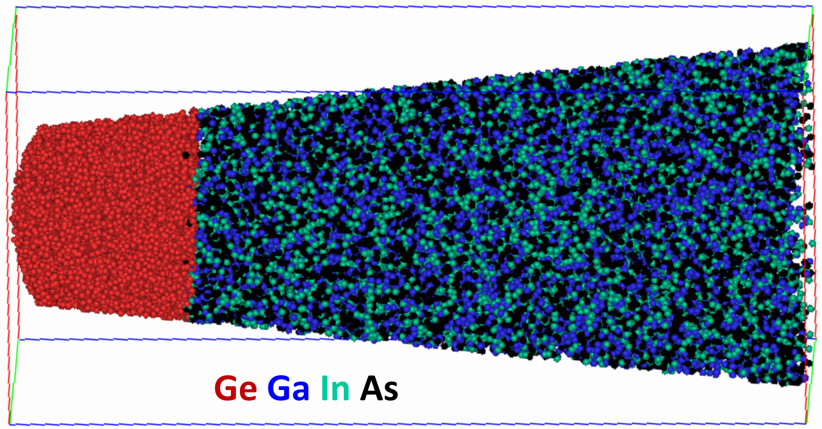
Increased Ge RLP intensity due to waveguide formation.



Material	Lattice Constant (Å)			In Composition (%)	Tensile Strain, Ge (%)	Critical Layer Thickness (nm)
	Out-of-Plane (c)	In-Plane (a)	Relaxed (a_r)			
ε-Ge/$In_{0.16}Ga_{0.84}As$	5.7201	5.7123	5.7164	15.7	0.75	270.8
ε-Ge/$In_{0.24}Ga_{0.76}As$	5.7506	5.7478	5.7492	23.7	1.6	42.6
ε-Ge/$In_{0.29}Ga_{0.71}As$	5.7693	5.7677	5.7685	28.5	1.94	25.9

Atom Probe Tomography (APT) of 1.6% ε-Ge/InGaAs (λ)

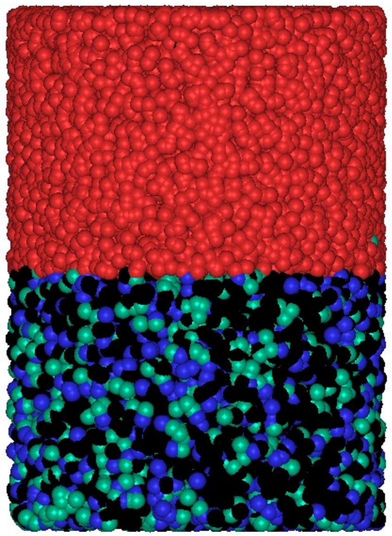
(a)



The reconstructed volume is 75x75x170 nm^3

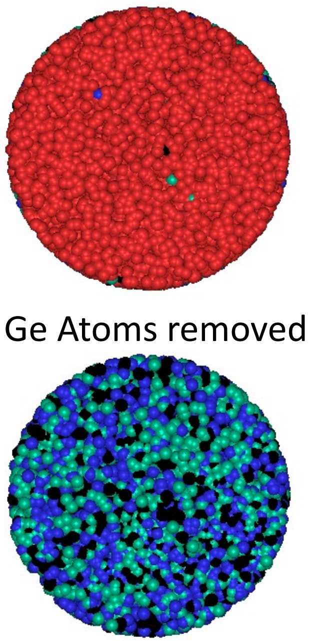
Intel Corporation

(b)



5 nm

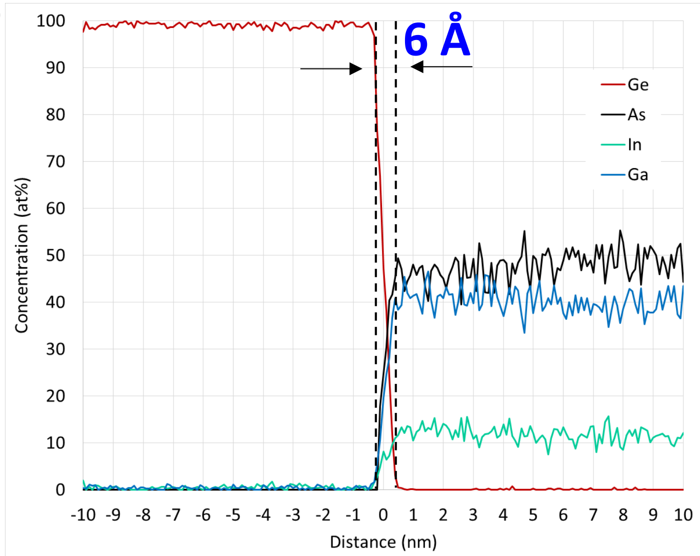
(c)



Ge Atoms removed

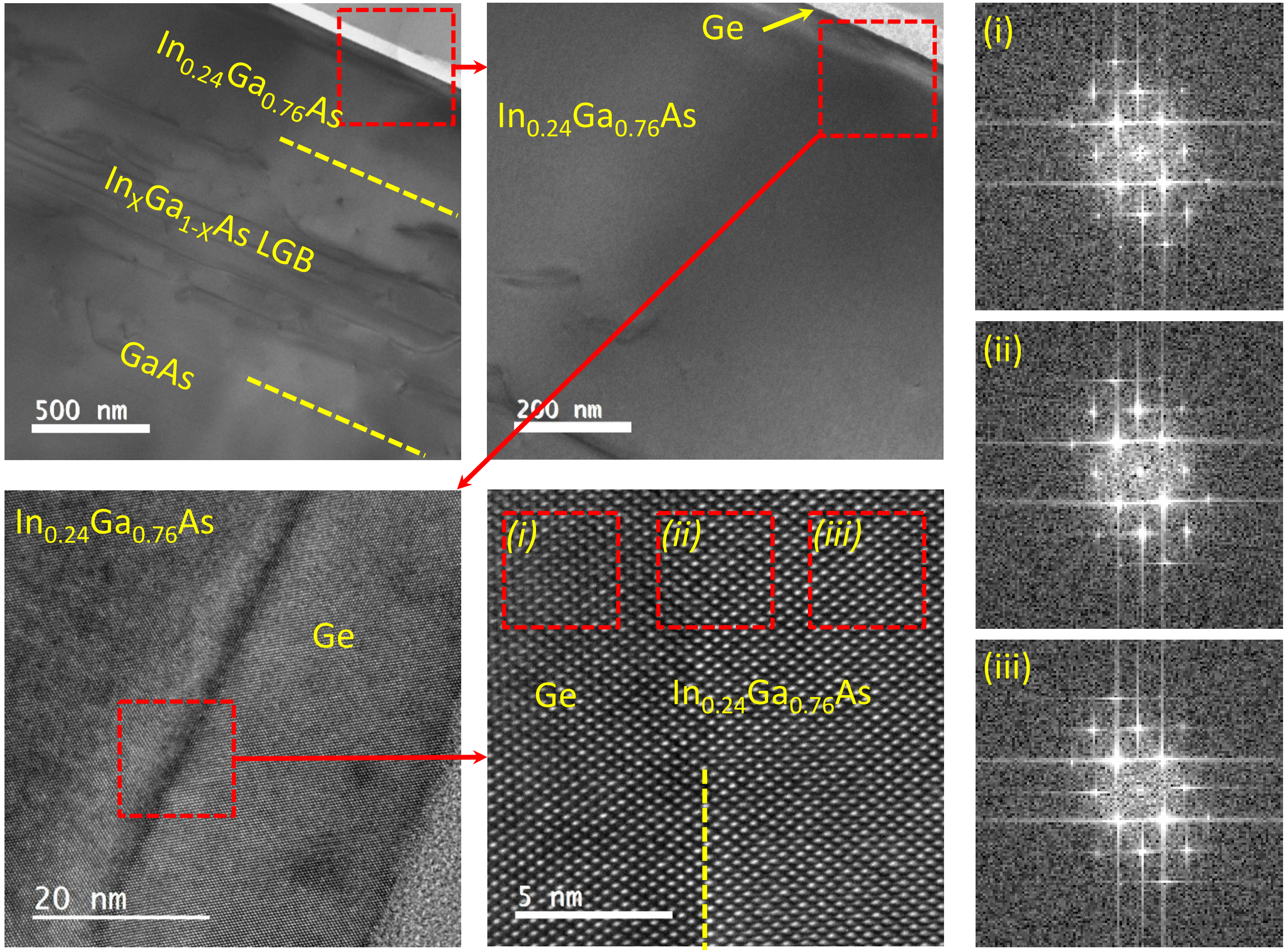
5 nm

(d)



M. B. Clavel *et al*, *Phys. Rev. Appl.* ,2022, **18**, 064083-1-12.

TFET Structural and Heterointerface Quality: Experimental



M. B. Clavel *et al*, *Phys. Rev. Appl.* ,2022, **18**, 064083-1-12.

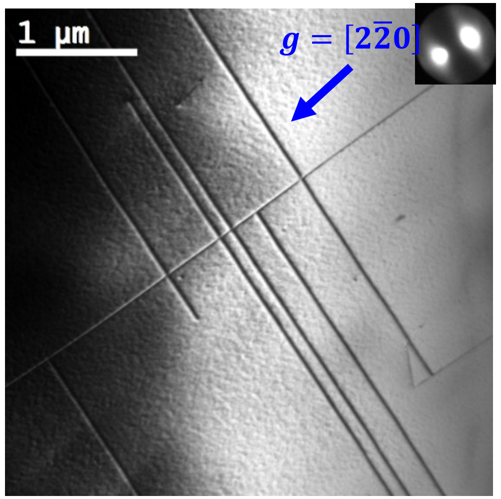
InGaAs/GaAs buffer accommodates lattice mismatch-induced defects.

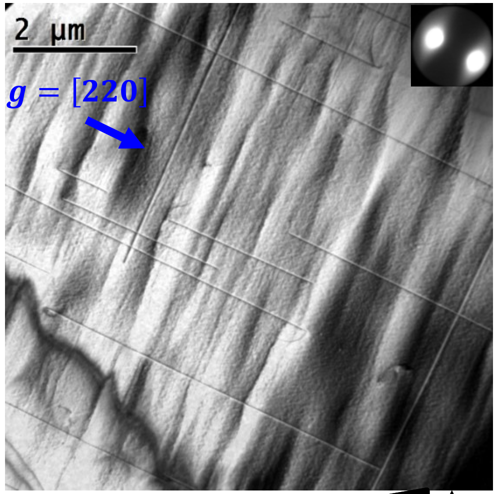
Dislocation- and defect-free active area and Ge/InGaAs tunnel junction.

Strained Ge epitaxy observed in lattice indexing and FFT analysis.

TFET: $\lambda \downarrow \rightarrow T_{WKB} \uparrow \rightarrow I_{ON} \uparrow$

Depth Dependent Defect Analysis of ε-Ge: Experimental

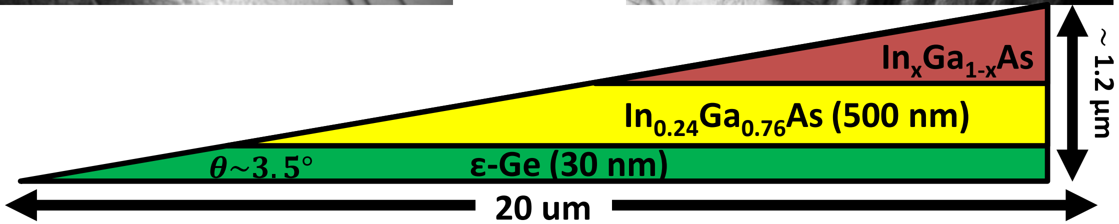


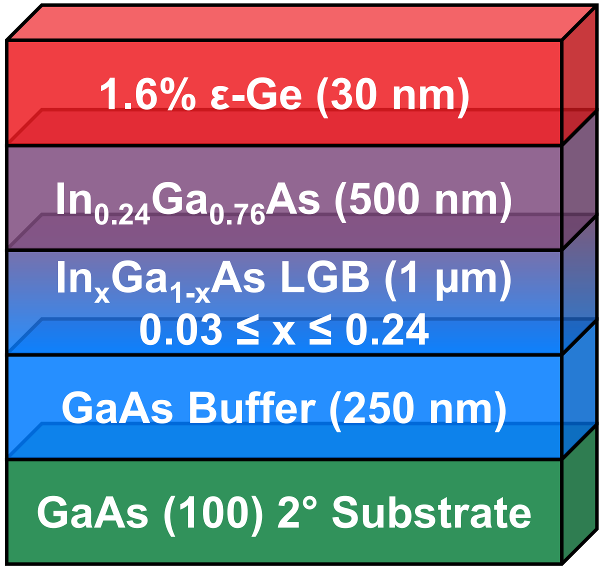


Hudait et al, ACS Appl. Electron. Materials (2021)

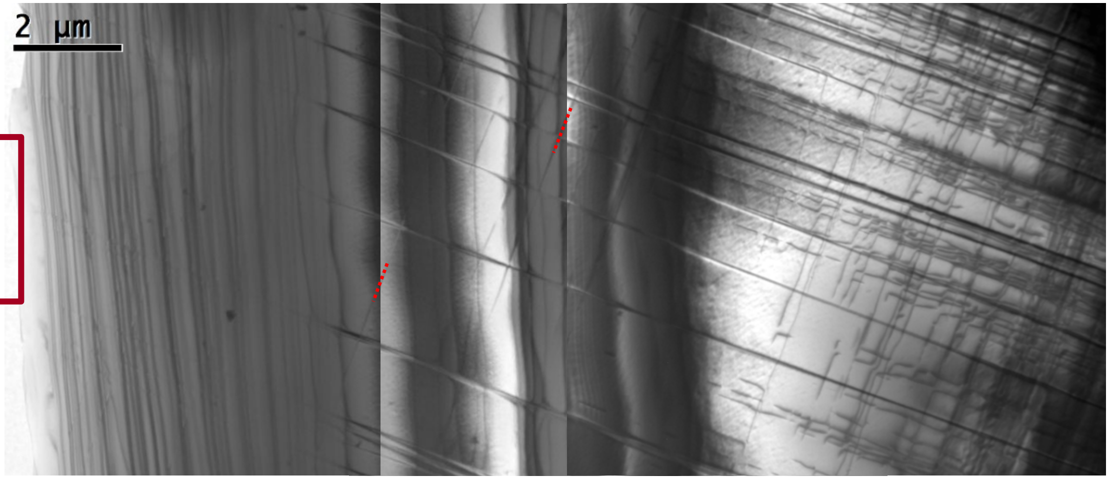
- **Low defect density ε-Ge layer**

PV-TEM





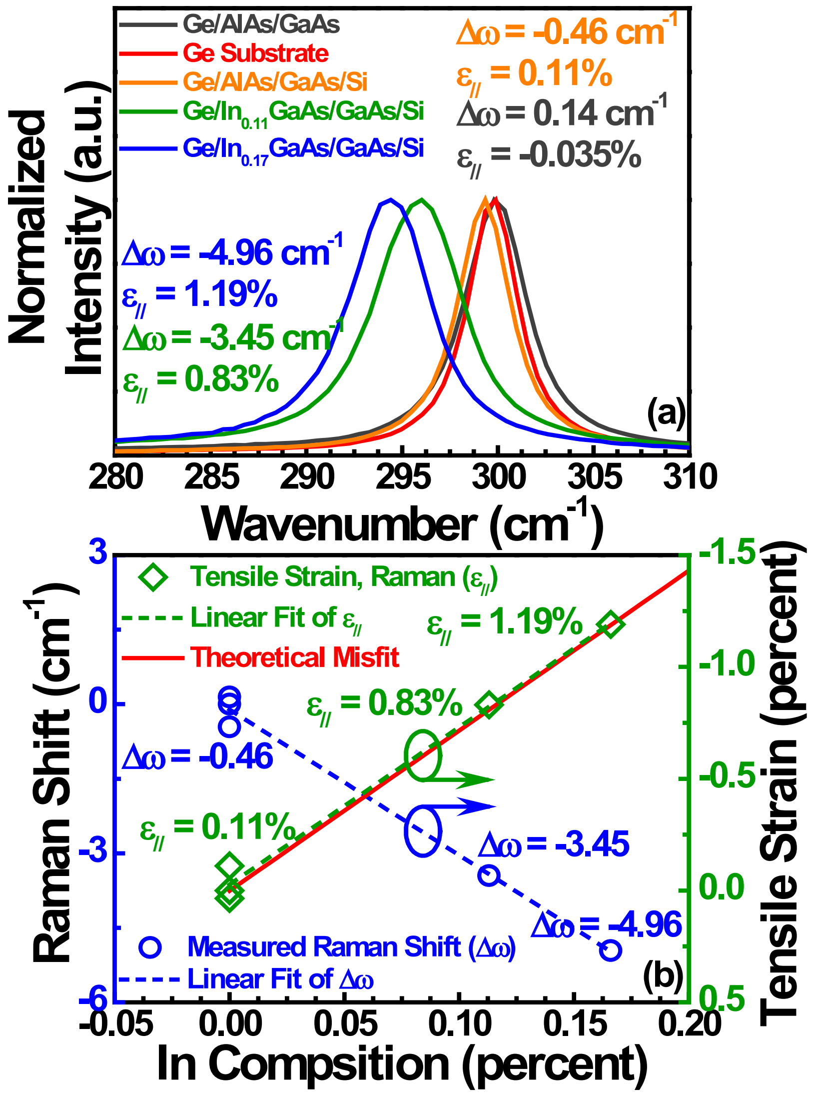
Defect-free ε-Ge?



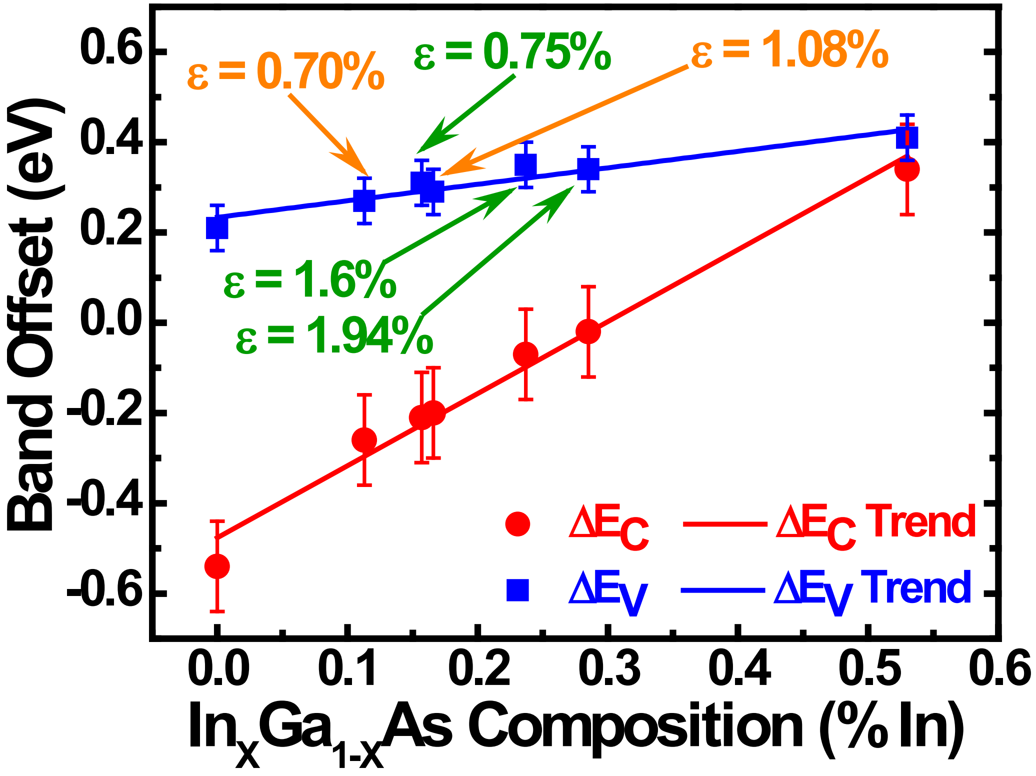
Clavel *et al*, *Phys. Rev. Appl.* ,2022, **18**, 064083-1-12.

Ge/InGaAs Tunnel Transistors: Experimental (Raman & XPS)

Strain Analysis

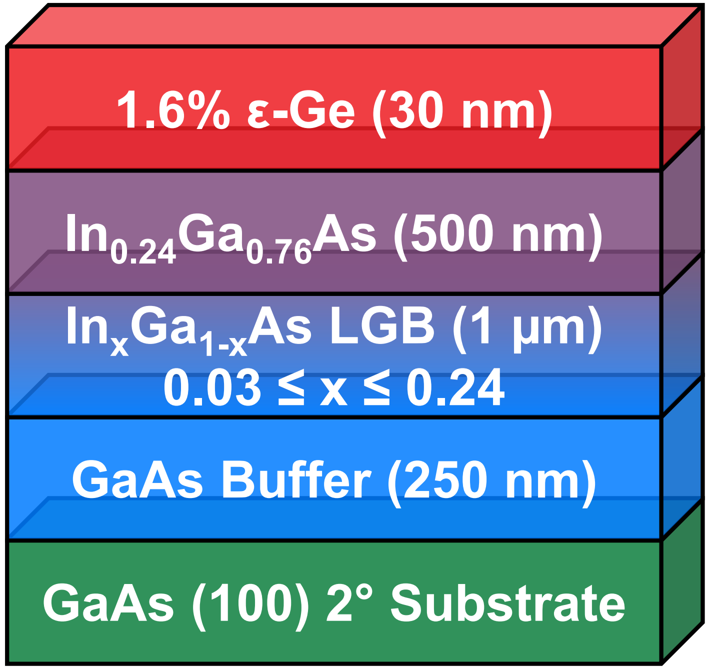


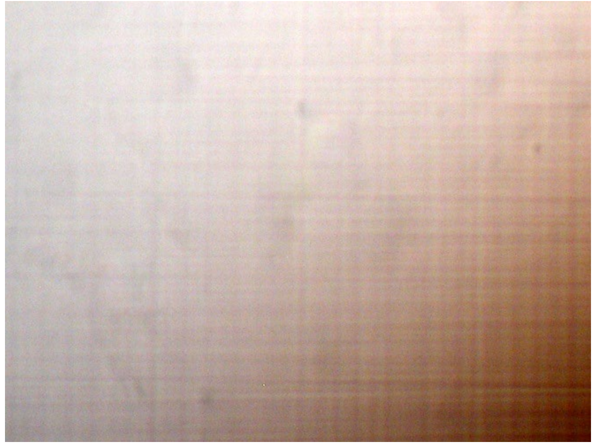
Band alignment & E_{beff}



M. Clavel et al, ACS Appl. Mater. Interfaces (2015); IEEE J-EDS (Special Issue TFET, 2015)

Temp Dependent Mobility in 1.6 % Strained Ge on InGaAs/GaAs





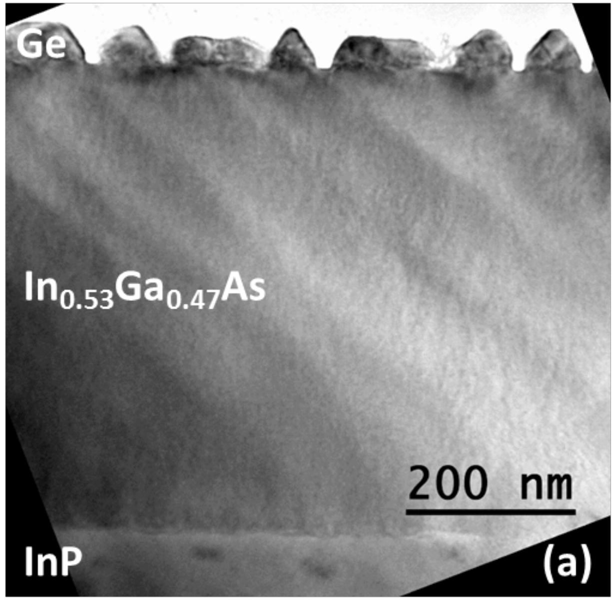
ADSEL0154

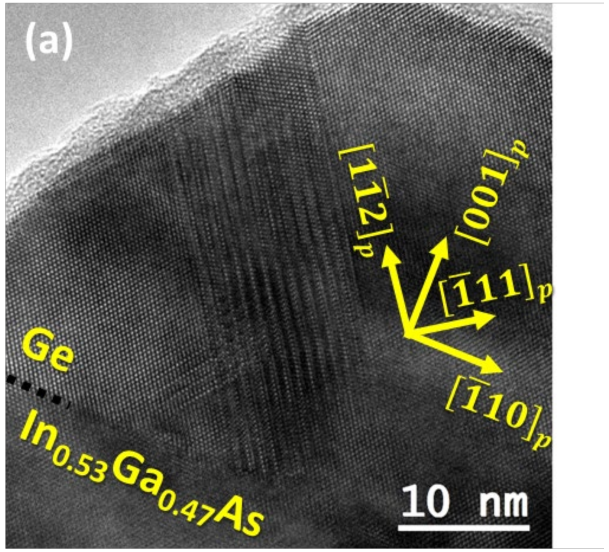
No	Temp(SV)	Current[A]	Bulk Con.	Sheet Con.	SheetResistance	Mobility
1	90	1.00E-03	-1.54E+18	-4.63E+12	1.58E+03	8.62E+02
2	115	1.00E-03	-1.61E+18	-4.82E+12	1.54E+03	8.50E+02
3	140	1.00E-03	-1.68E+18	-5.03E+12	1.49E+03	8.36E+02
4	165	1.00E-03	-1.76E+18	-5.27E+12	1.46E+03	8.13E+02
5	190	1.00E-03	-1.83E+18	-5.48E+12	1.46E+03	7.82E+02
6	215	1.00E-03	-1.92E+18	-5.77E+12	1.46E+03	7.44E+02
7	240	1.00E-03	-2.04E+18	-6.13E+12	1.42E+03	7.19E+02
8	265	1.00E-03	-2.28E+18	-6.85E+12	1.33E+03	6.88E+02
9	290	1.00E-03	-2.50E+18	-7.50E+12	1.26E+03	6.63E+02
10	315	1.00E-03	-2.45E+18	-7.36E+12	1.29E+03	6.56E+02

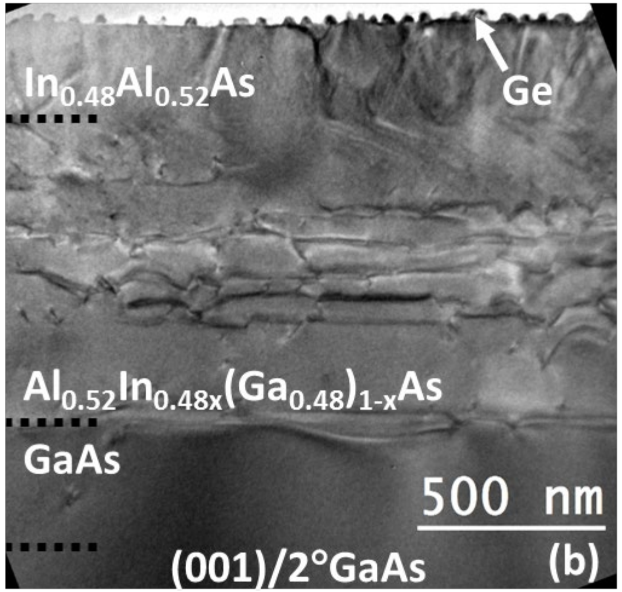
- Electron mobility increases with decreasing temperature
- Increase in mobility indicates superior quality ε-Ge

Clavel et al, Phys. Rev. Appl. (2022)

Highly Tensile Strained (4%) Ge on InGaAs or InAlAs buffers



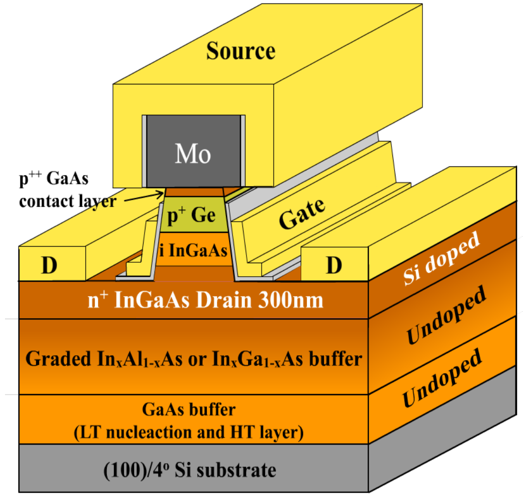




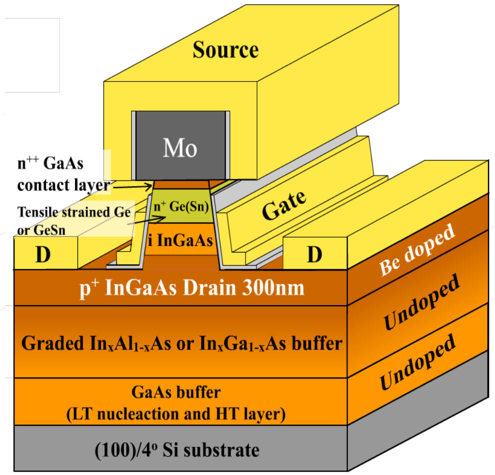
Ack: Patrick Goley

Schematics of Ge/$In_xGa_{1-x}As$ TFET Device Structures

(a) N-type

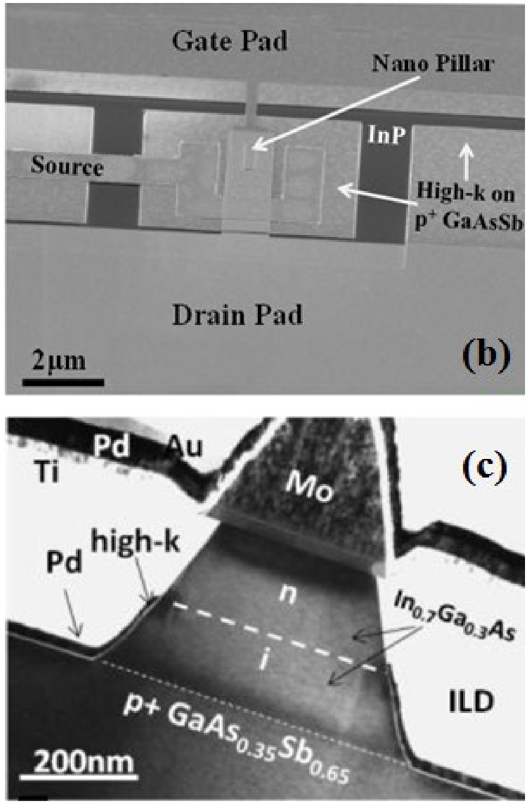


(b) P-type



(c) Process flow: Nano-pillar TFET

- Surface cleaning: Degreasing and native oxide removal
- Blanket deposit Mo on source contact
- Define Ti/Cr etch mask
- Dry etch Mo and source/channel layer to the drain
- Wet etch undercut source/channel layer
- Deposit high-κ gate dielectric
- Deposition and lift-off self aligned gate metal
- Device isolation
- Planarization with BCB and etch back
- Remove Pd and high-k on top of Mo
- Lift-off source, drain and gate contact pads

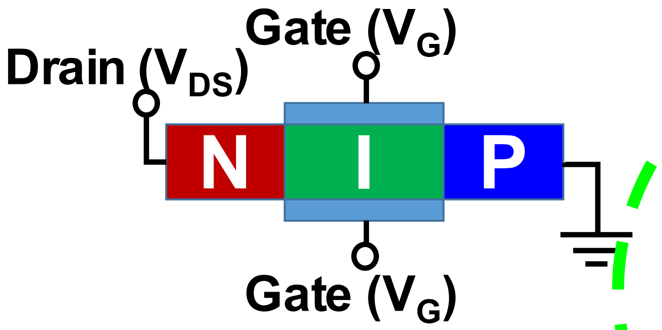


Collaboration with Prof. S. Datta @ Georgia Tech

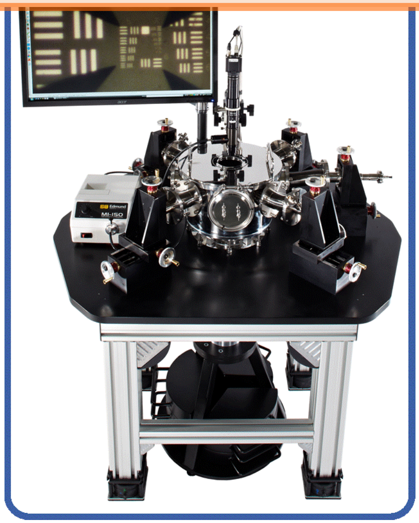
- Demonstrated better control of E_{beff} both simulation and experiment
- Developed a growth methodology that enable to increase the critical layer thickness and strain in Ge

Materials Synthesis-Device Properties-Trap Characterization of n-and p-channel $Ge/In_xGa_{1-x}As$ TFET Devices

TFET DESIGN



TFETs Characterization



TRAP CHARACTERIZATION & DEVICE BENCHMARK

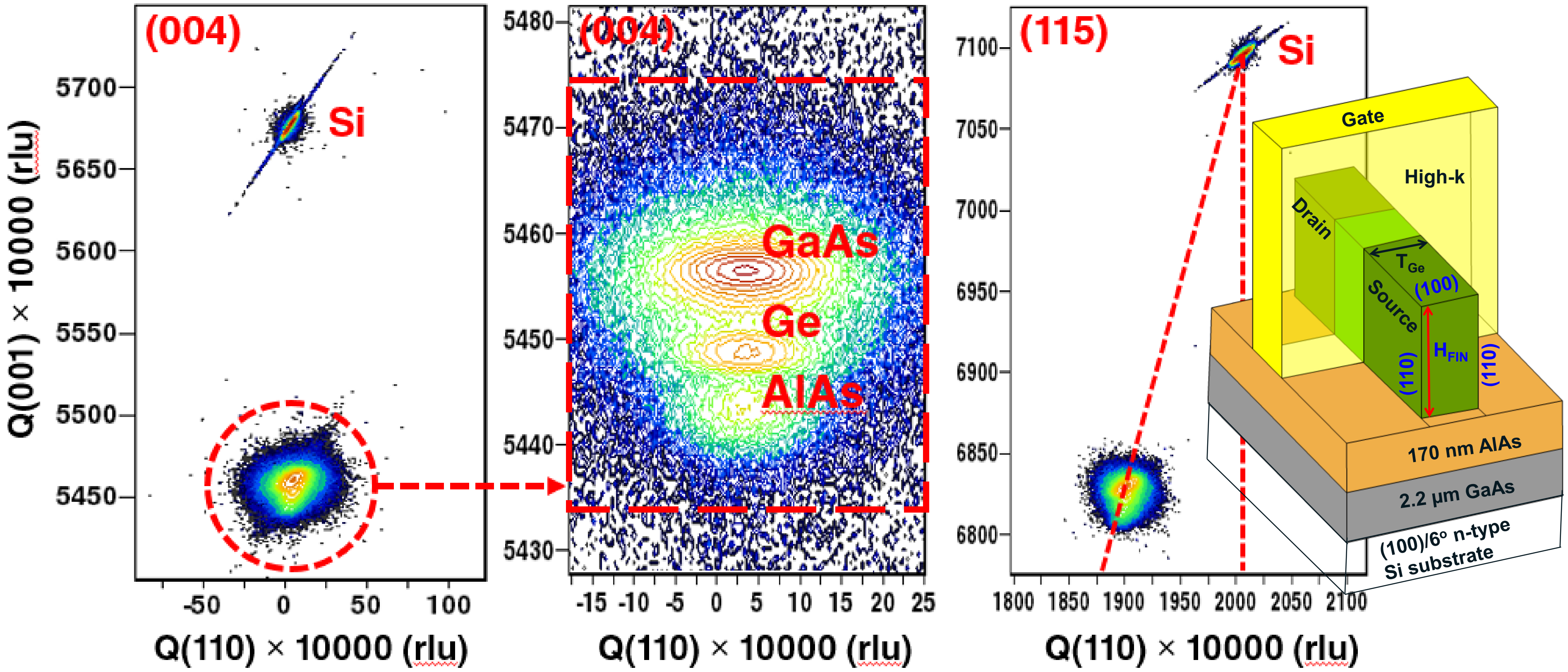
III-V/Ge MBE Epitaxial Growth

TFETs Fabrication

Materials Characterization

Electronics
FinFET

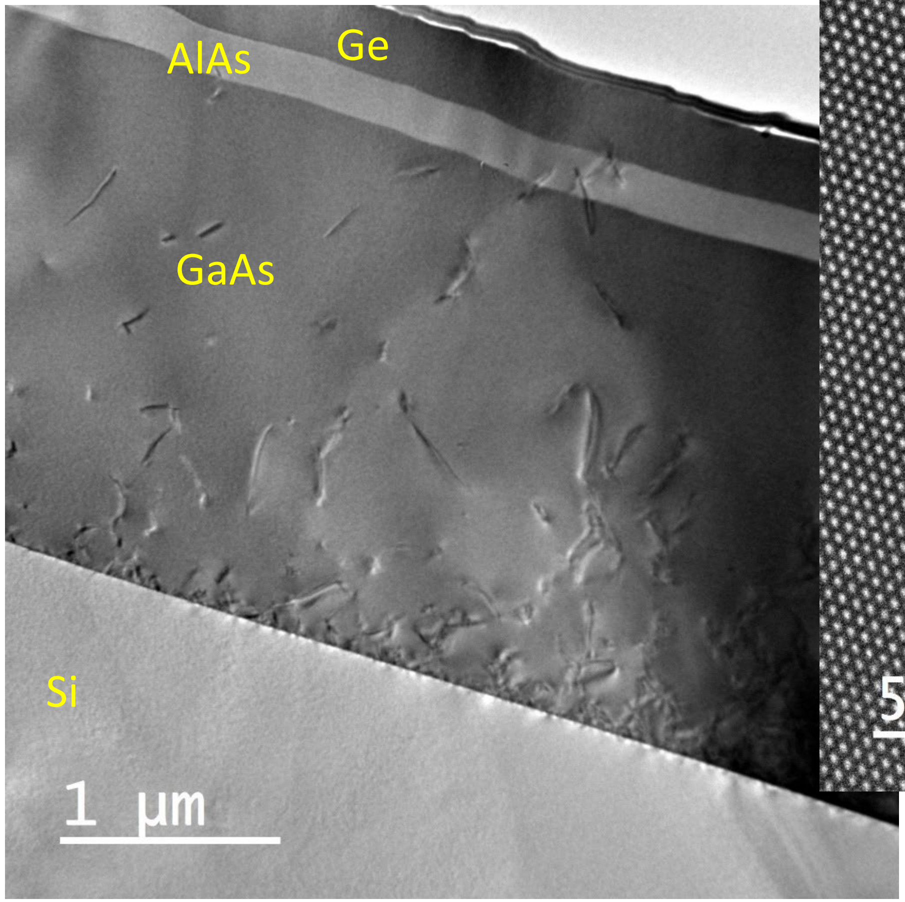
Epitaxial Ge on Si using GaAs and AlAs buffers for Ge FinFET

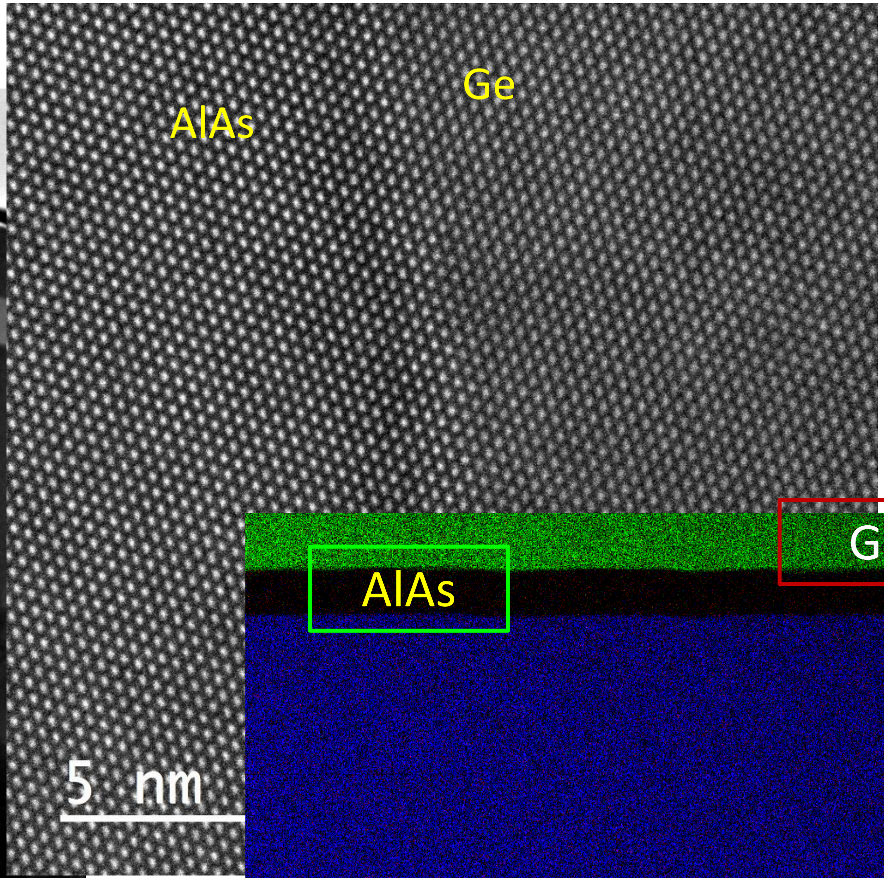


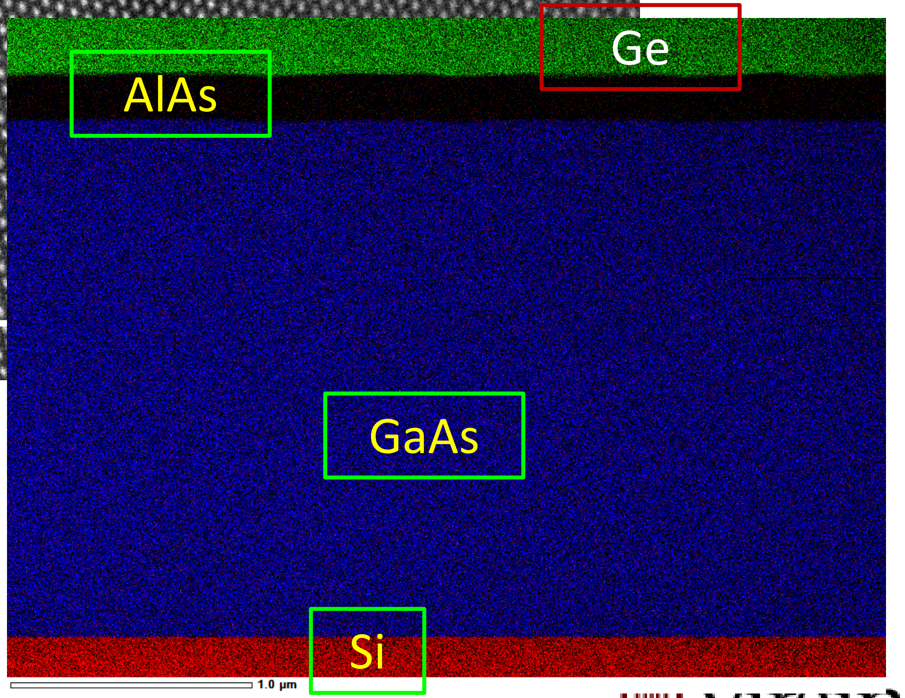
Our x-ray characterization capabilities can precisely determine each layer in our grown device structure

Hudait et al, Scientific Reports 4: 6964 (2014)

Atomic View of Ge/AlAs/GaAs/Si Heterostructure via TEM

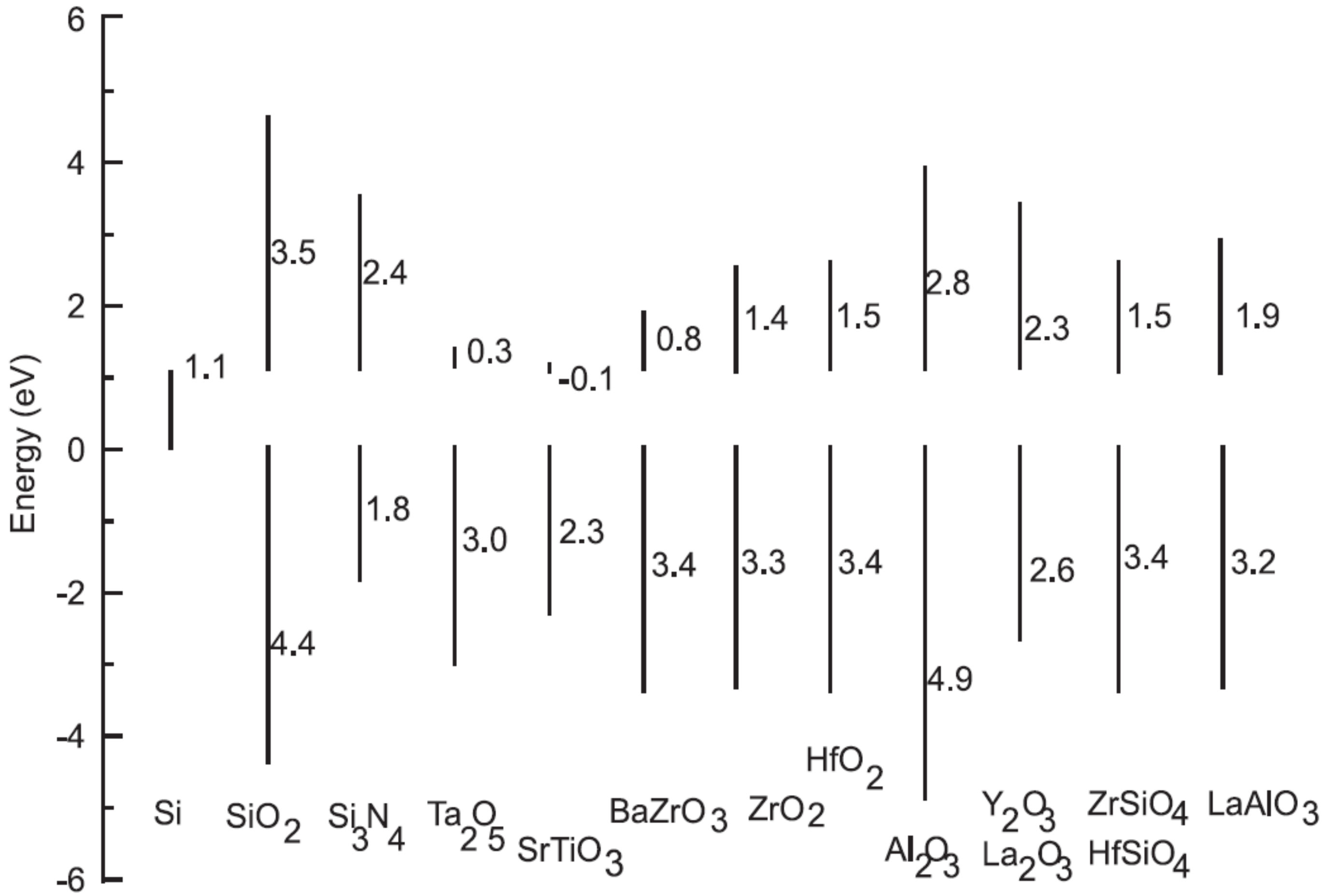






Hudait et al, Scientific Reports 4: 6964 (2014)

Band Offsets "Look-up Table" on Si



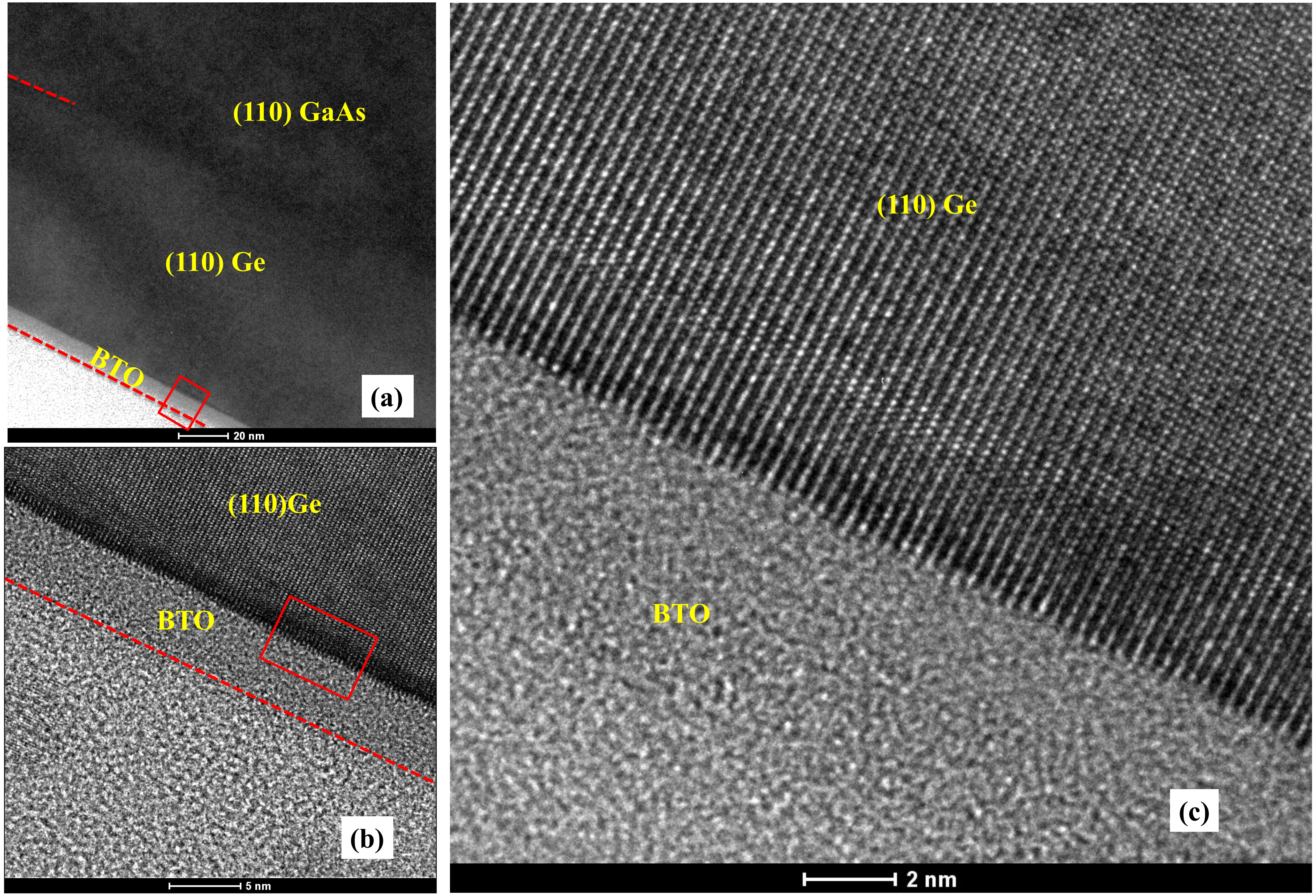
Can we have similar to (100)Ge and (110)Ge orientations?

Experimental?

Predicted barrier heights for a range of high-k gate oxides on Si

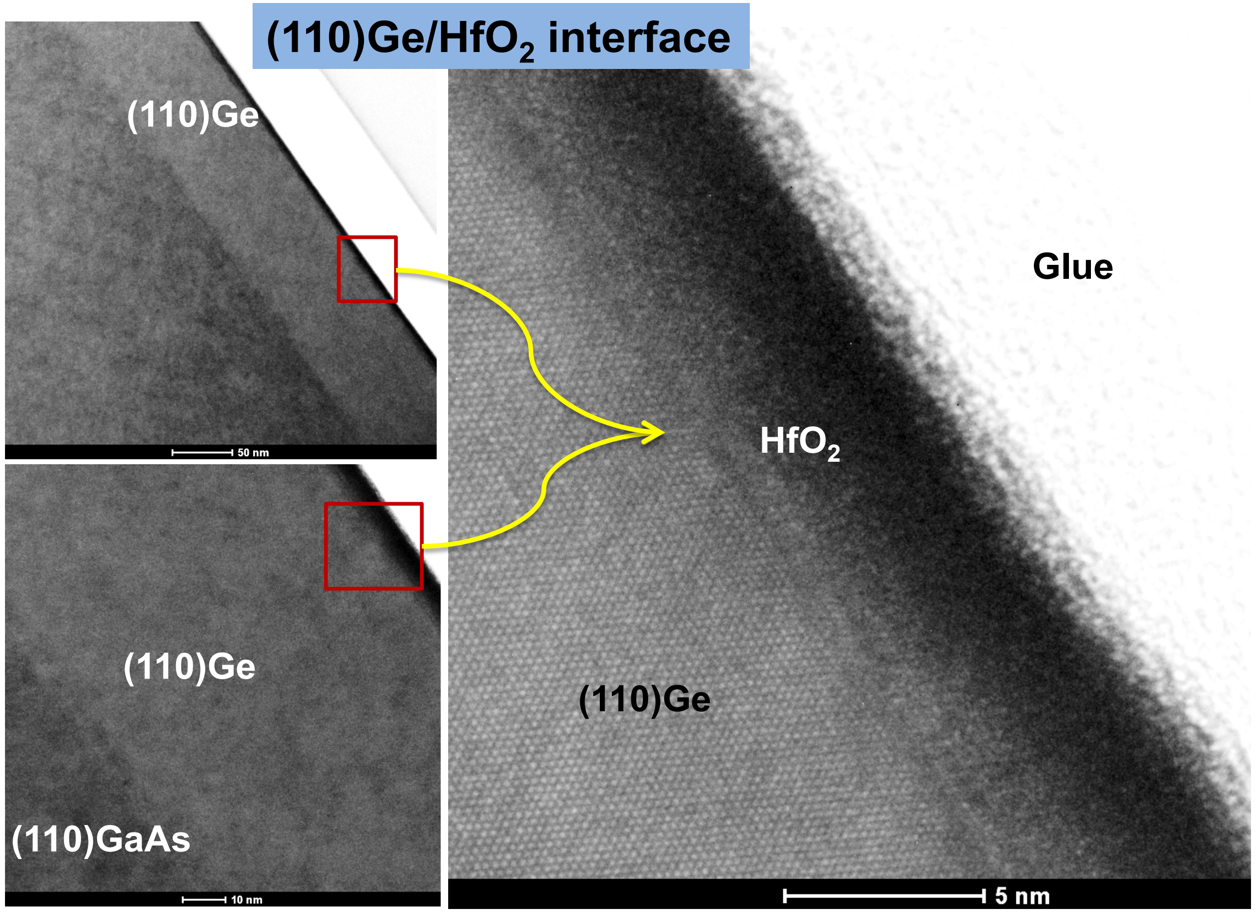
J. Robertson, Eur. Phys. J. Appl. Phys. 28, 265-291 (2004)

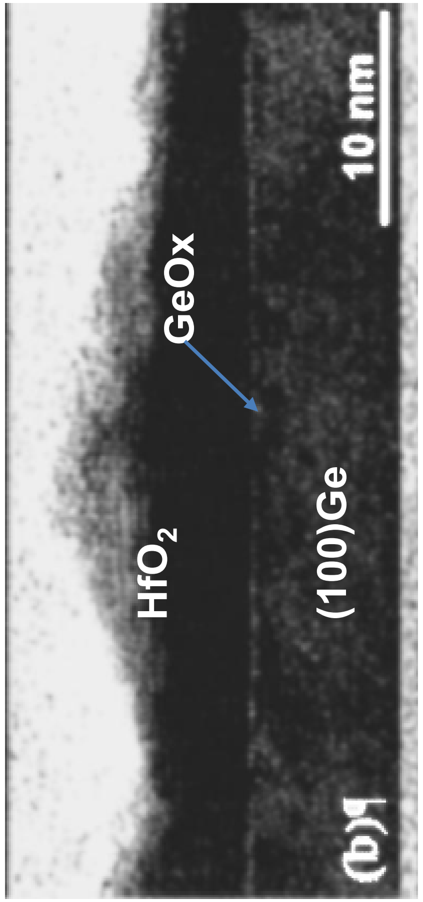
Perovskite, $BaTiO_3$ Integration on (110)Ge



Hudait et al, ACS Applied Materials & Interfaces, 5: 11446-11452 (2013)

Atomic Layer Deposited HfO_2 on (110)Ge



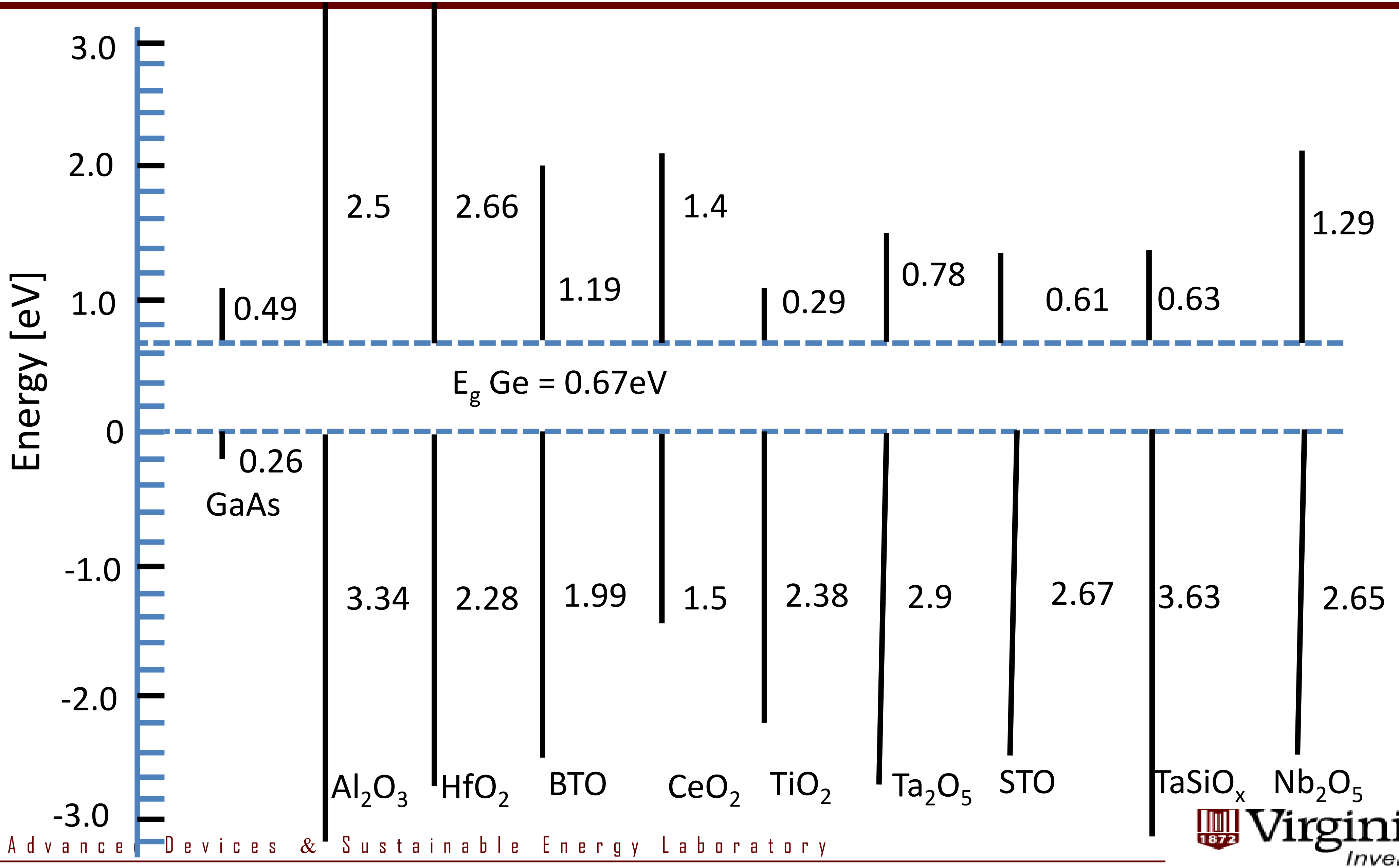


- HR-TEM micrograph shows absence of interfacial layer
- Sharp interface between HfO_2 and Ge as well as Ge and (110) GaAs

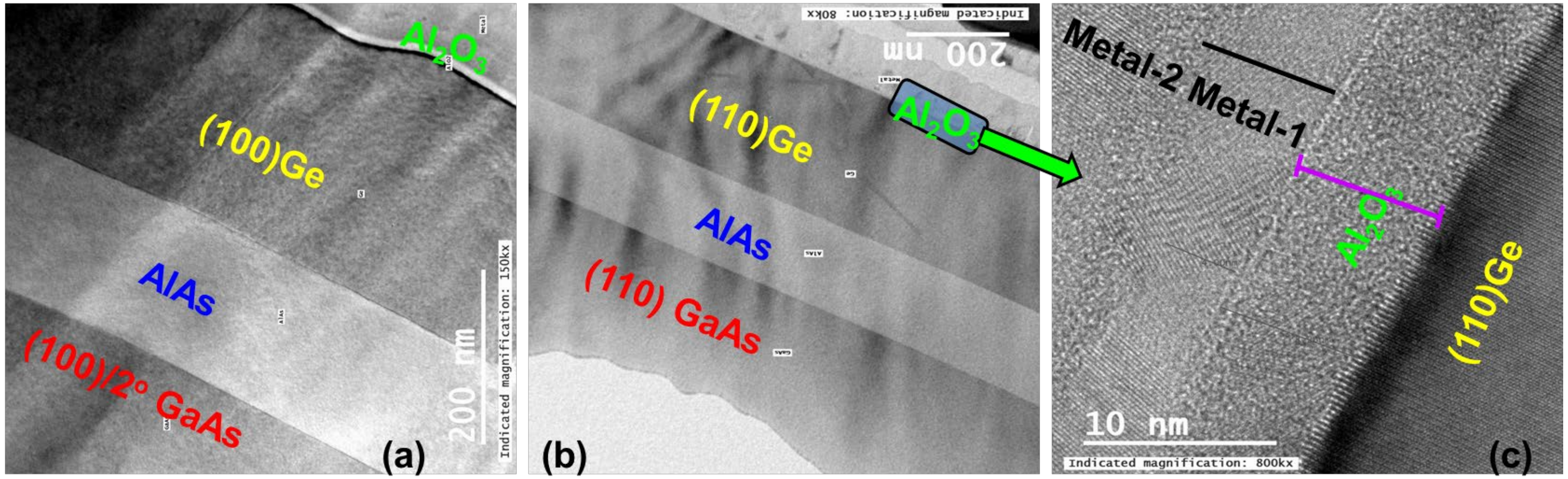
Ref: S. V. Elshocht, et al, "Deposition of HfO2 on germanium and the impact of surface pretreatments" Appl. Phys. Lett. 85, 3824 (2004).

Hudait et al, APL 102: 093109 (2013)

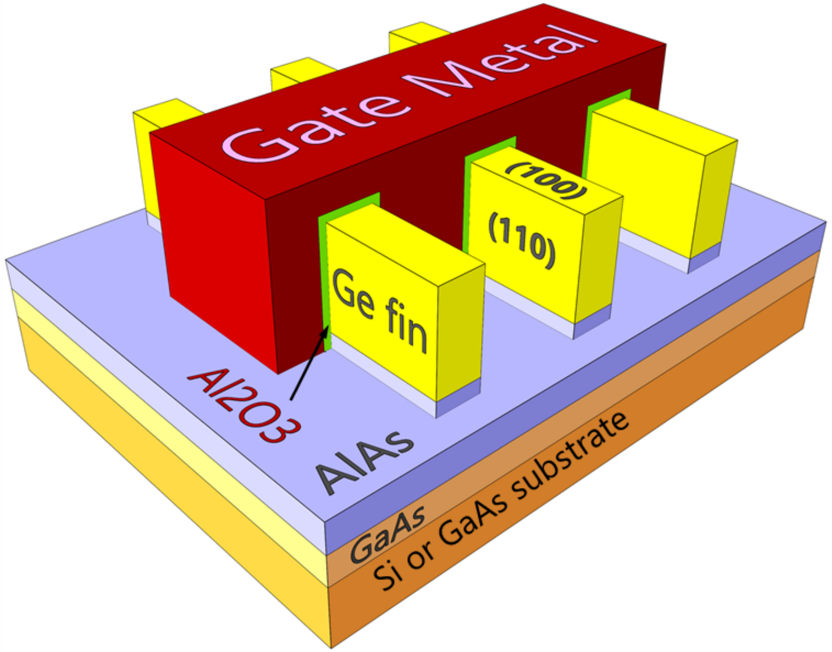
Experimental Band Offsets "Look-up Table" on (110)Ge

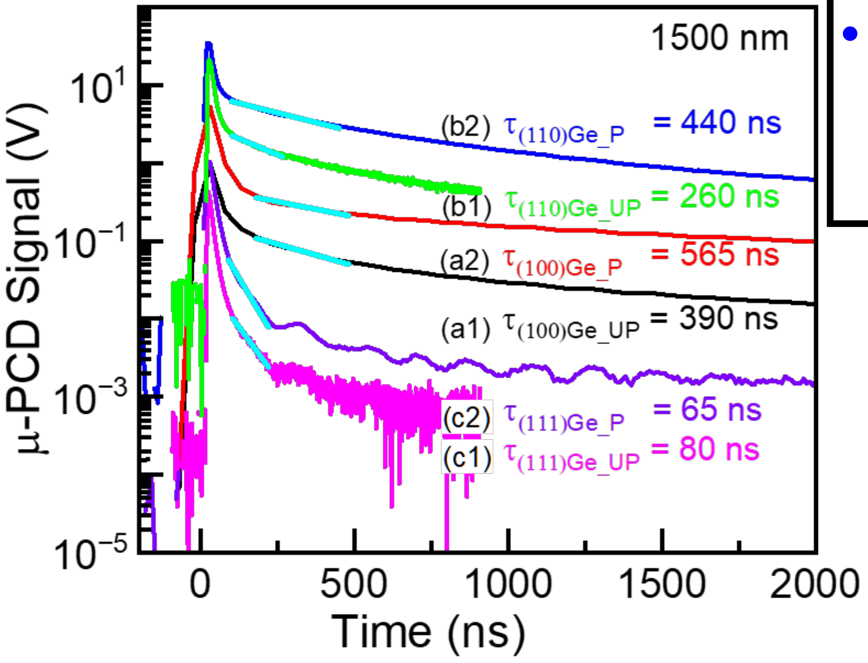


ALD Al_2O_3 on (100)Ge and (110)Ge: TEM & Carrier lifetime study



- Sharp heterointerface of high-k and Ge
- High carrier lifetime after Al_2O_3 deposition (Passivation)

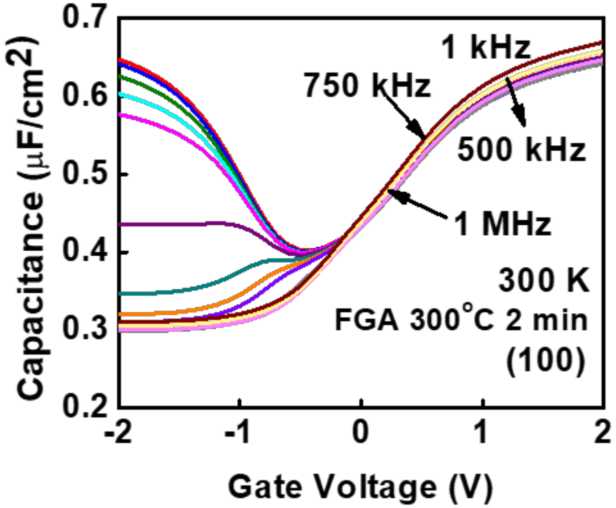


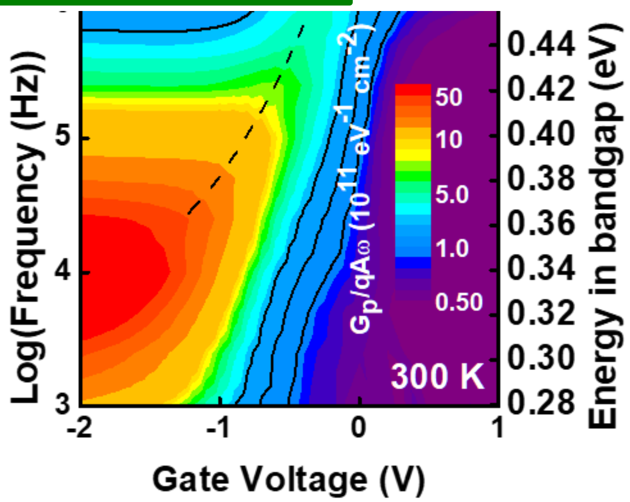


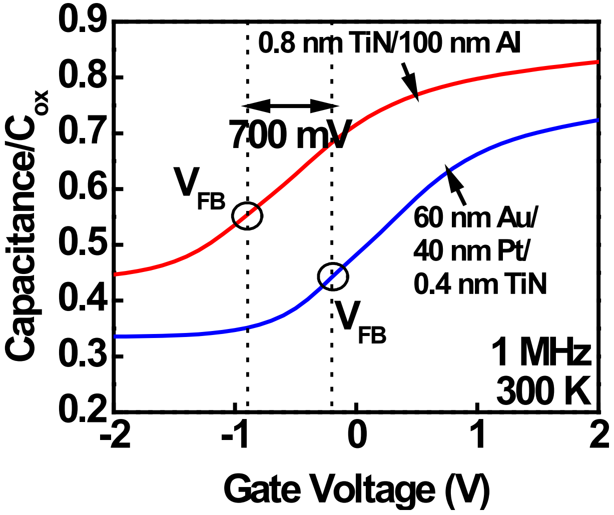
Hudait et al (under review, 2023)

C-V Characteristics of Al_2O_3/(100)Ge and (110)Ge MOS-Cs

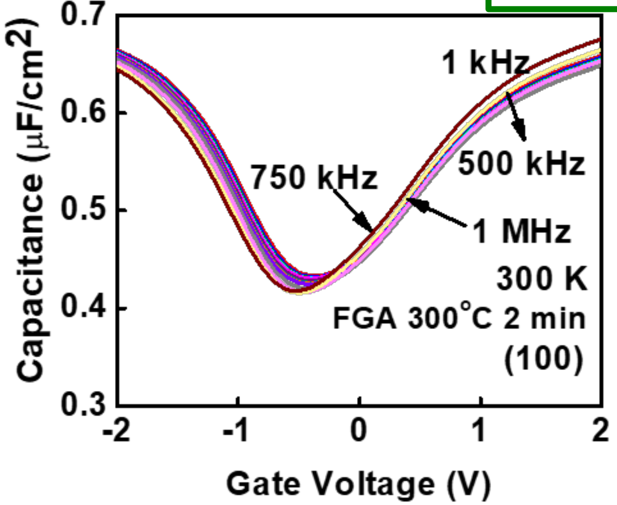
(100) Ge/AlAs/GaAs

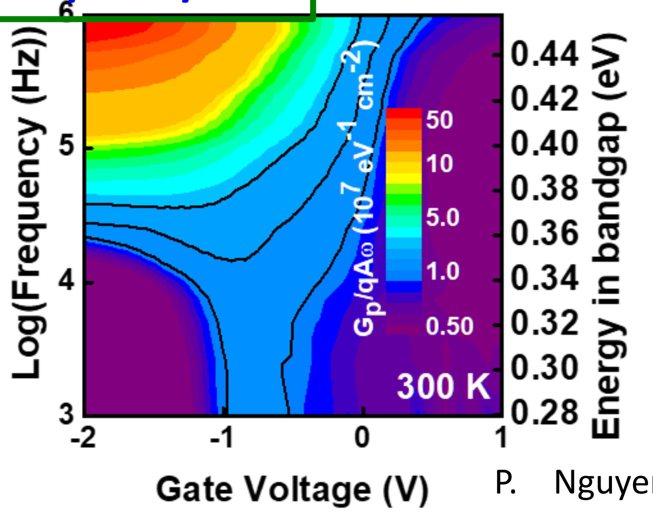


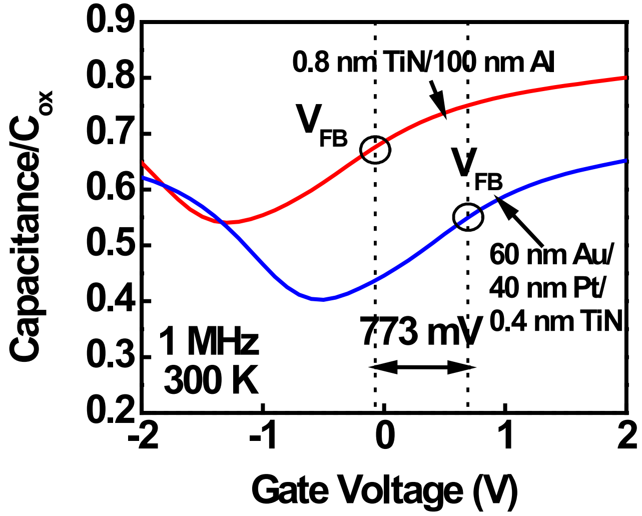




(110) Ge/AlAs/GaAs

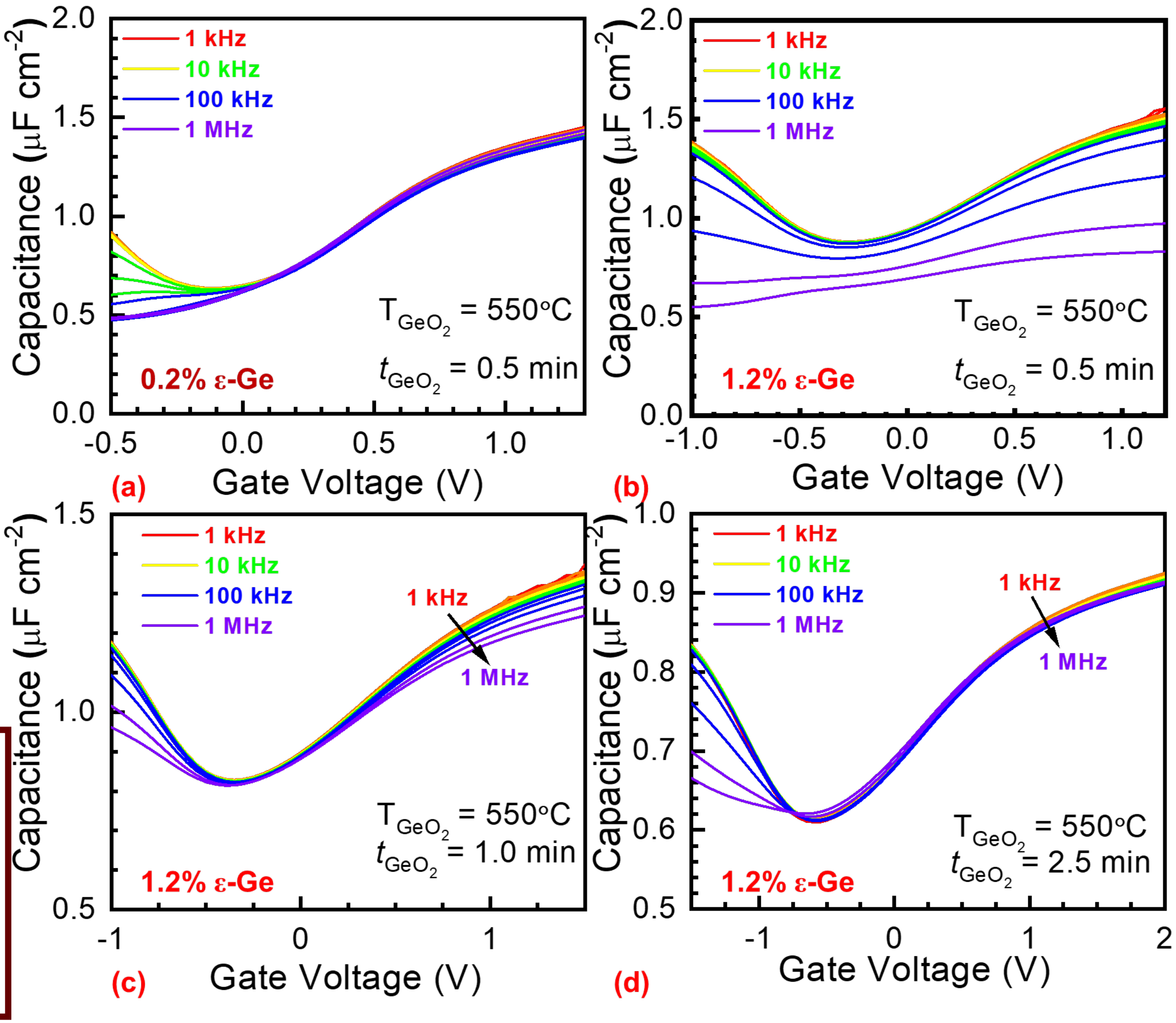






P. Nguyen et al, Microelectronic Engineering 199: 80-86 (2018)

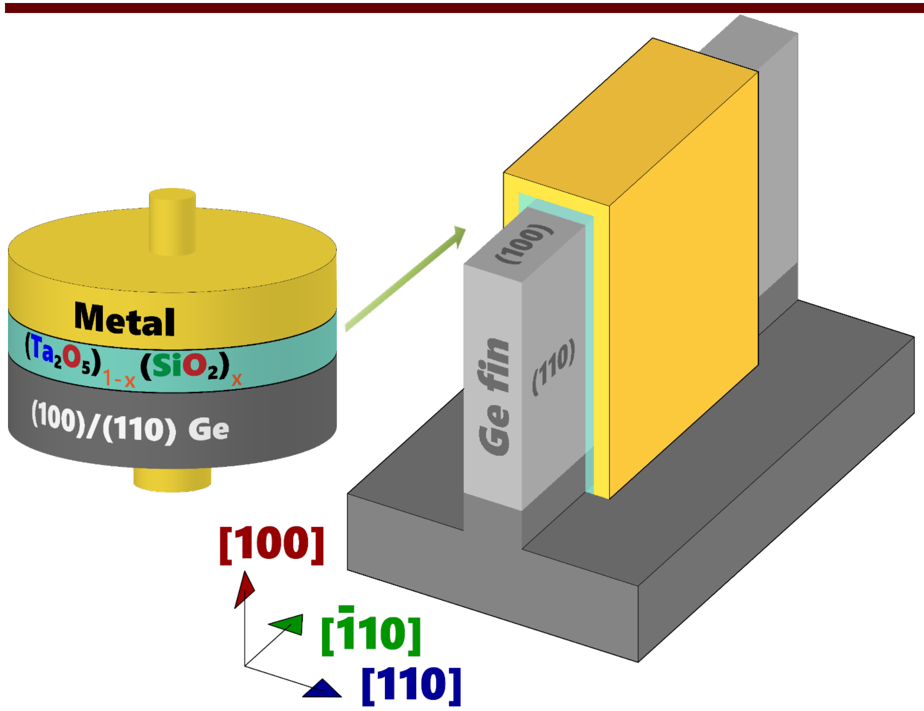
Composite Gate Dielectrics on Ge and ε-Ge

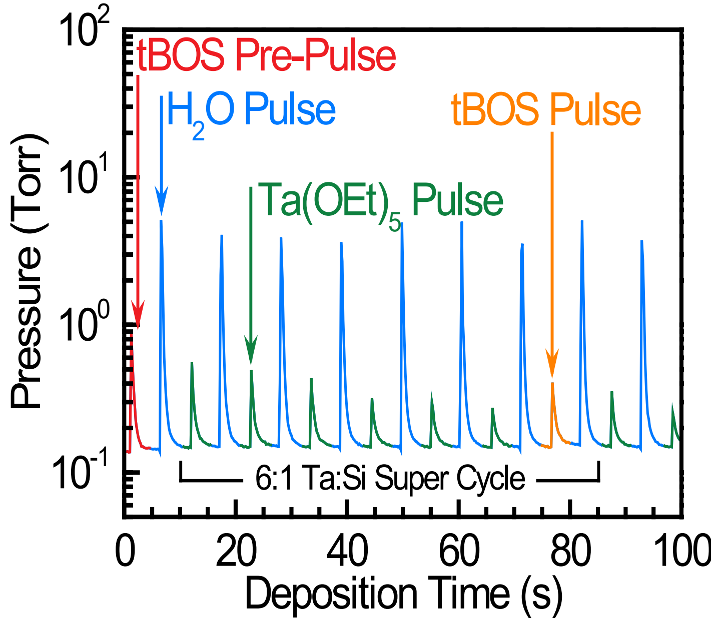


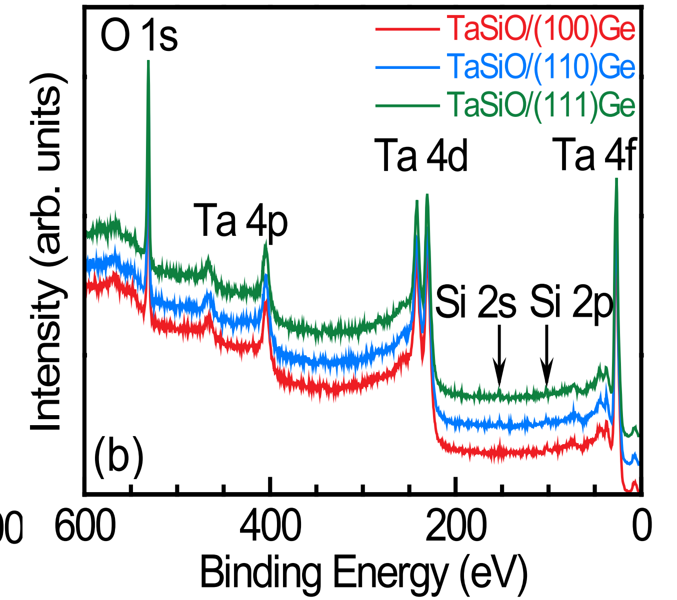
- **Composite dielectric constant is lower than HfO_2 on Ge**
- **Change in process parameters for unstrained Ge and strained Ge**

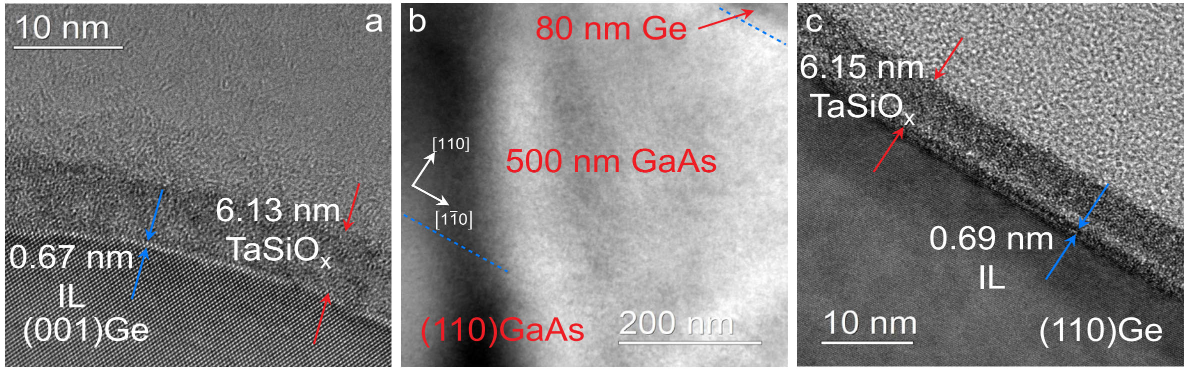
Hudait et al (under review, 2023)

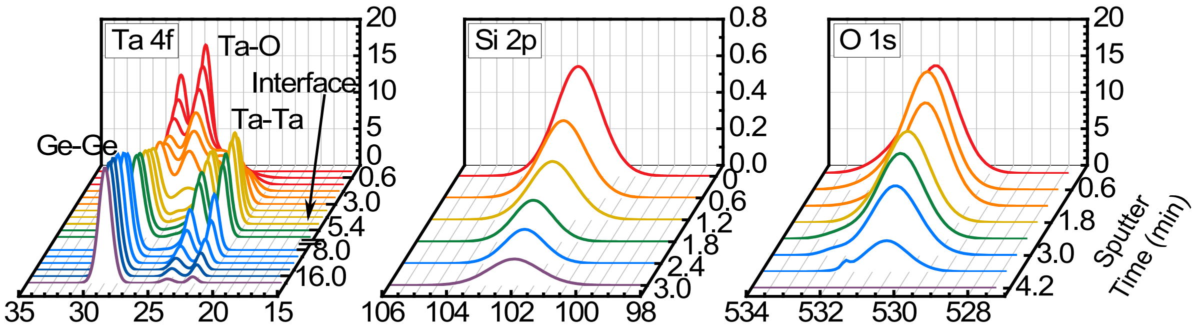
In-situ Si Passivation Layer on Ge via ALD Si Precursor





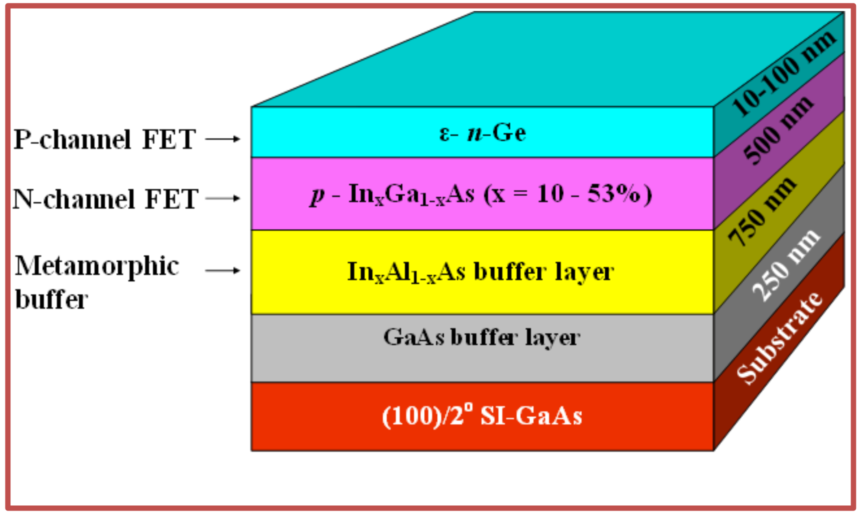




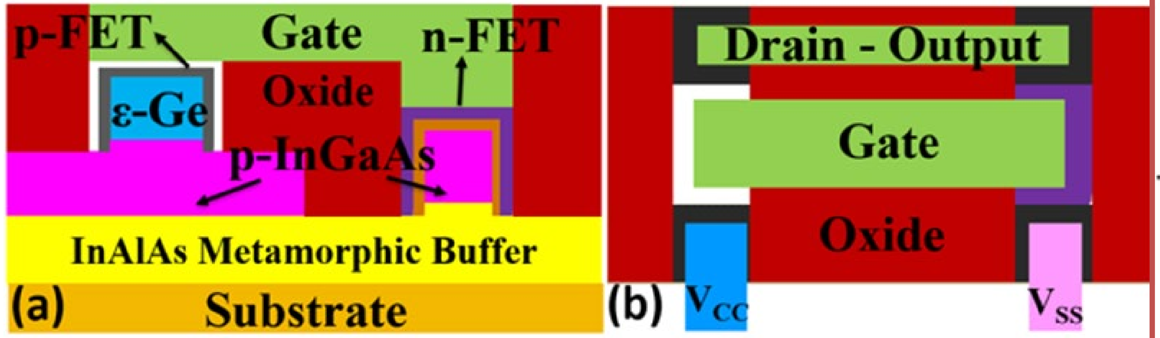


M. B. Clavel *et al*, *RSC Materials Advances* 2022.

Monolithically Integrated Ultra-low power Ge/InGaAs CMOS

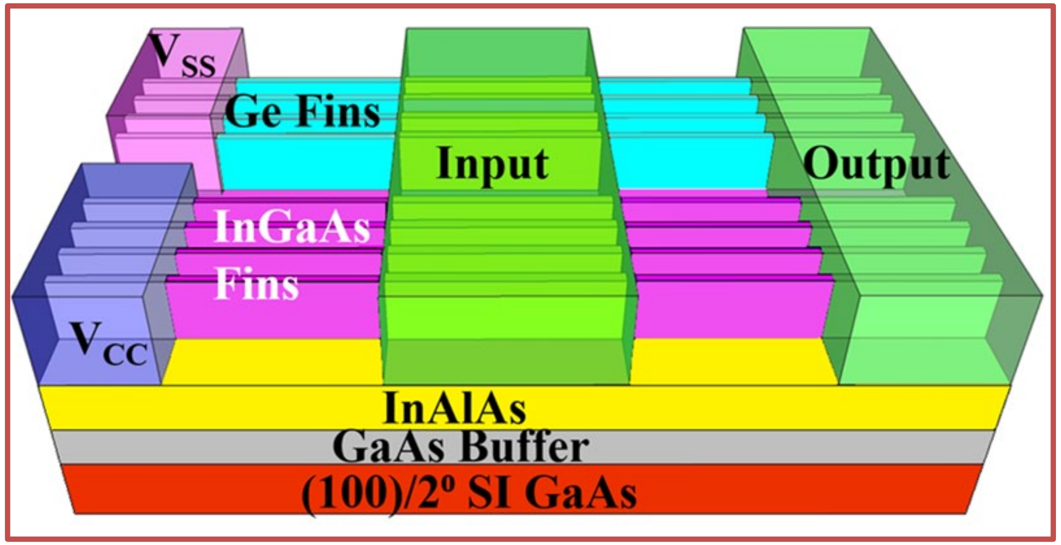


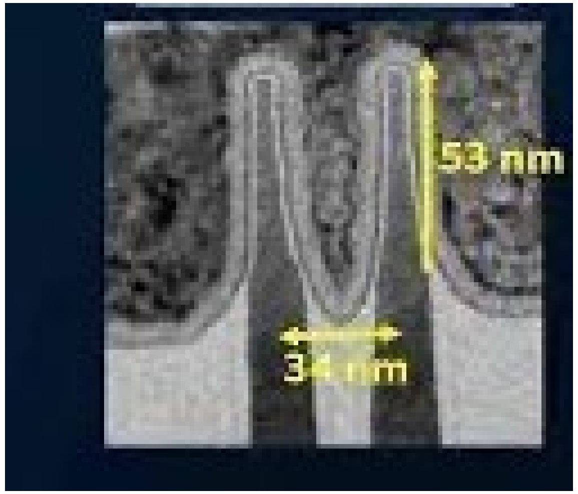
Proposed Cointegrated Stack



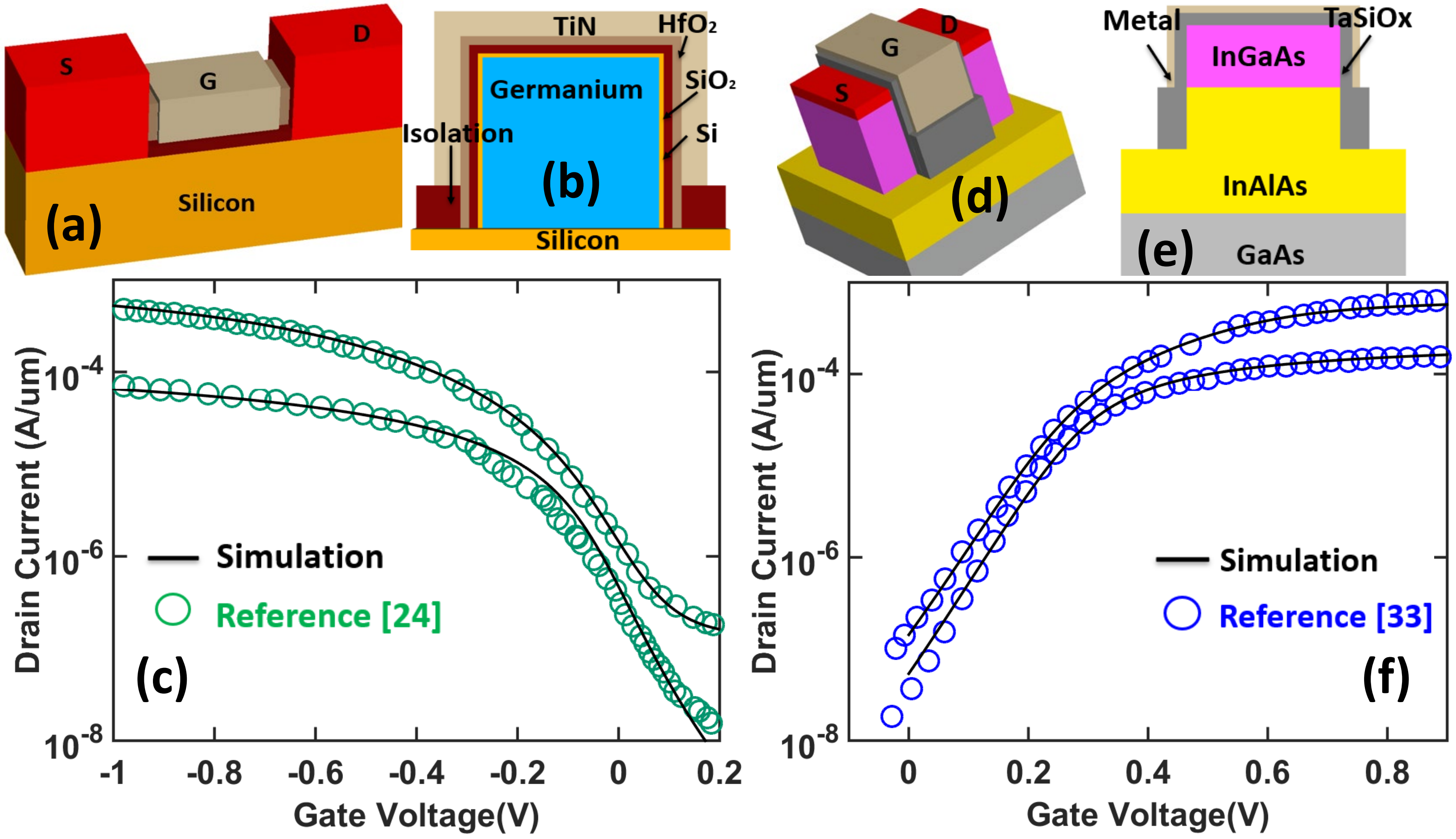
Cross-sectional view

Top layout view





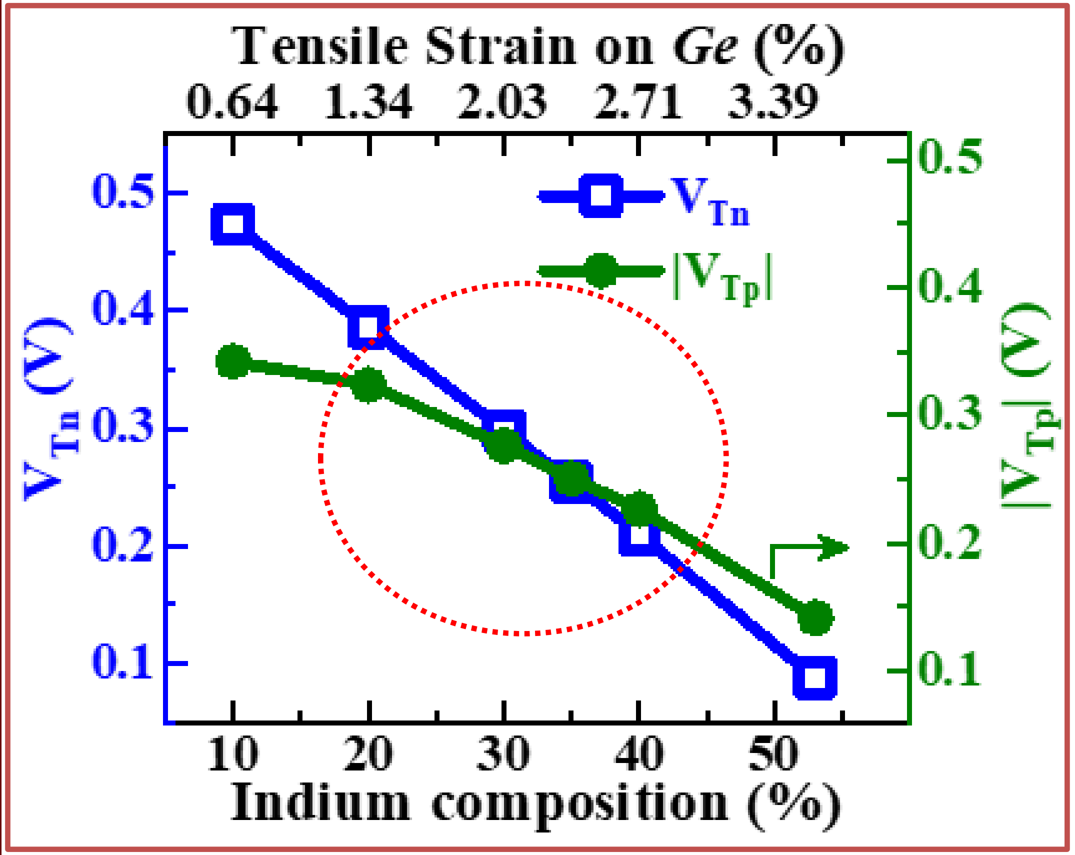
p-Ge and n-InGaAs FinFET Calibration

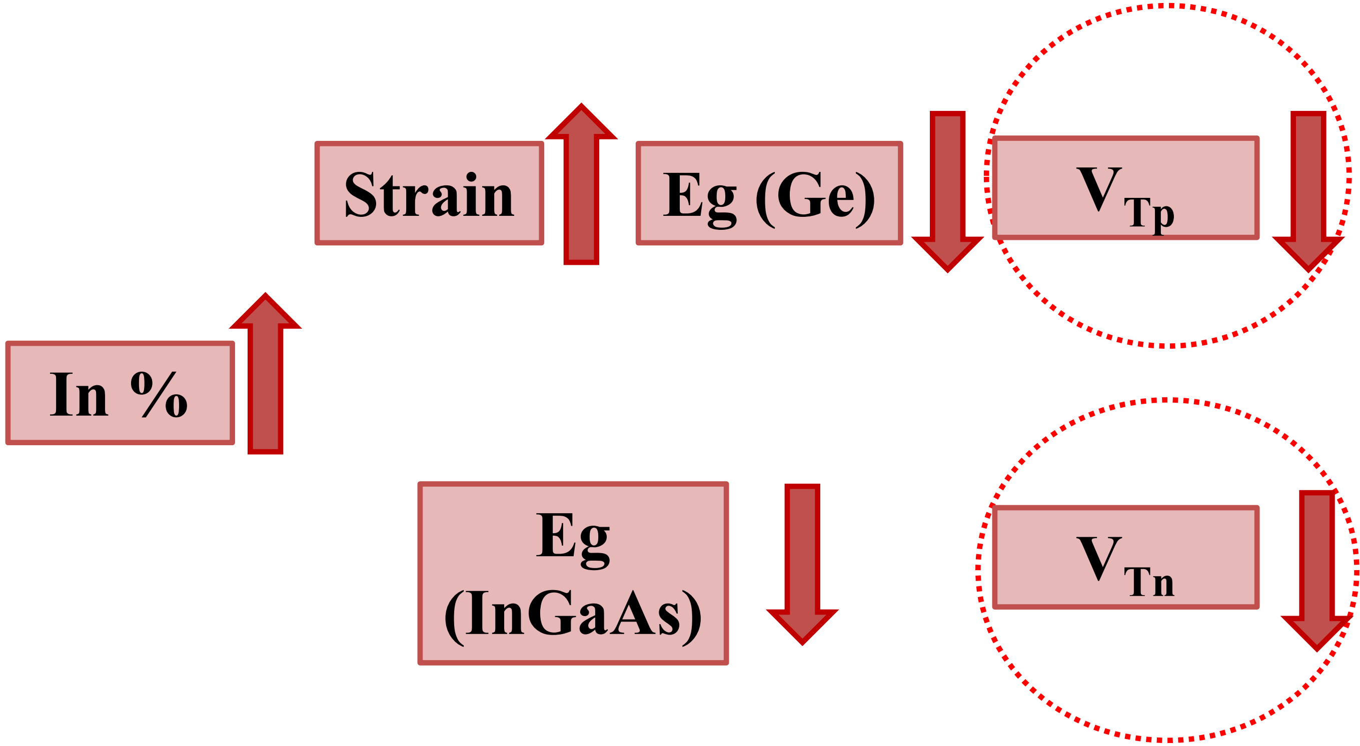


Rutwik Joshi *et al, IEEE TED 69 (8): 4175-4182 (2022).*

Ge/InGaAs FinFETs: Threshold Voltage

- V_{TH} : Leakage

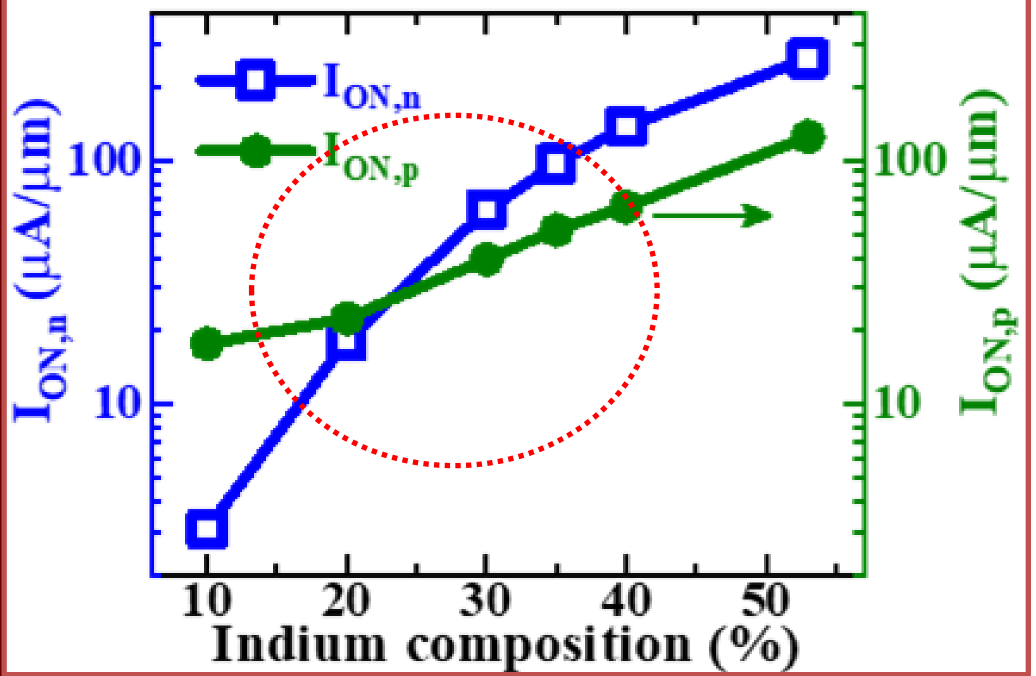




Rutwik Joshi *et al, IEEE TED 69 (8): 4175-4182 (2022).*

Ge/InGaAs FinFETs: ON Current

- I_{ON} : Drive capability and speed



In % ↑

Strain ↑ μ_h ↑ I_{ONp} ↑

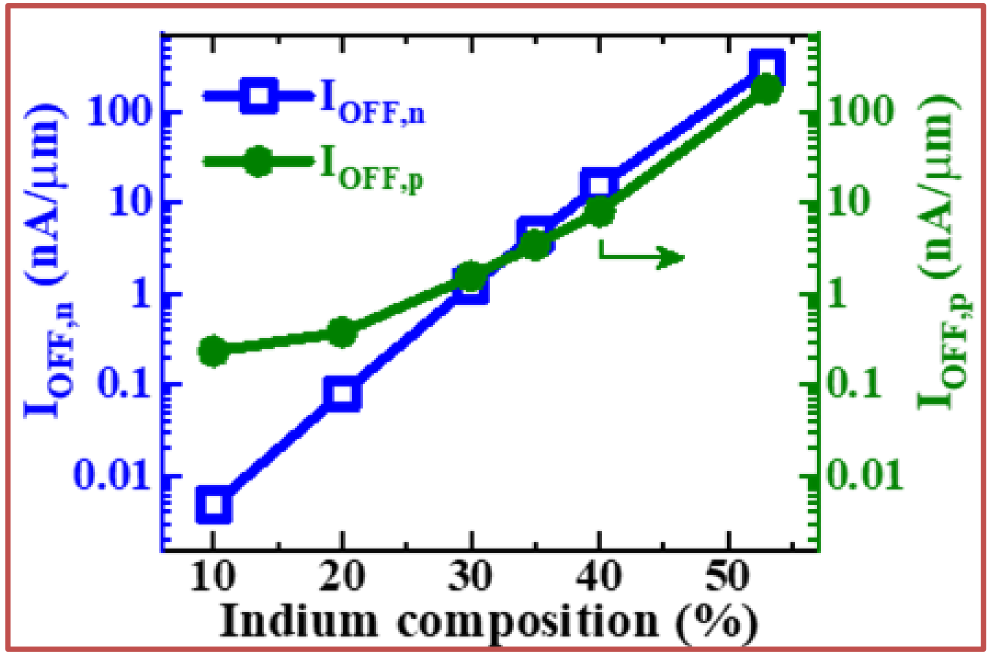
μ_e ↑ I_{ONn} ↑

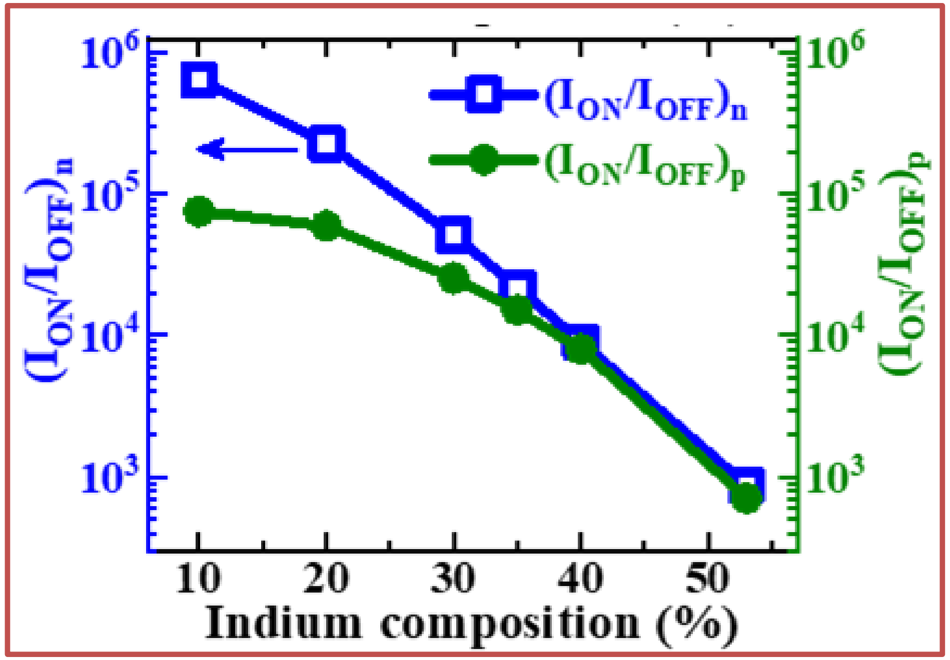
1. V_T change will affect currents.
2. Effective mass change will affect QC, in turn affecting V_T and currents

Rutwik Joshi *et al, IEEE TED 69 (8): 4175-4182 (2022).*

Ge/InGaAs FinFETs: OFF Current

- I_{ON}/I_{OFF} ratio : Leakage and dissipation



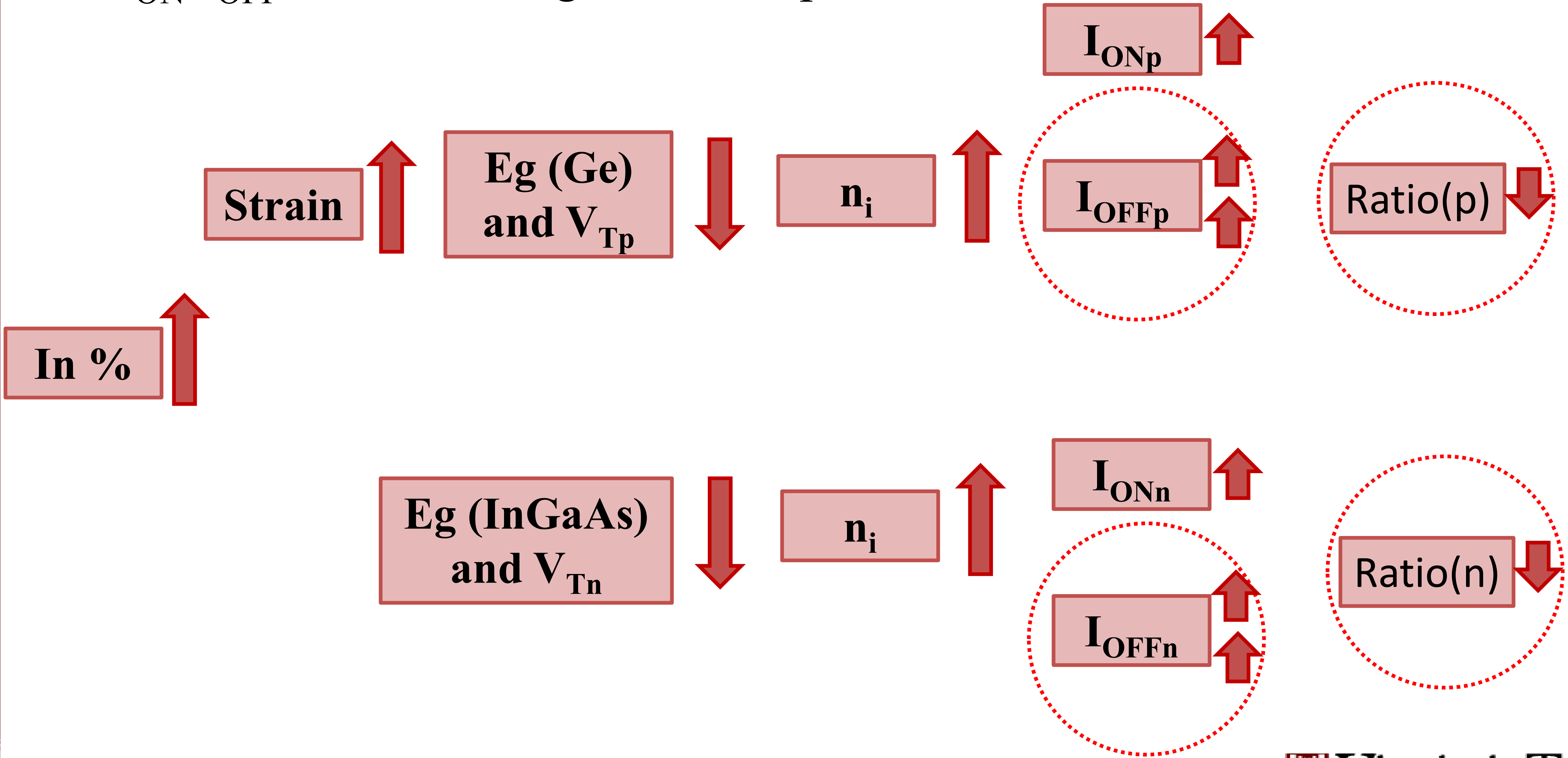


Let's understand why ……

Rutwik Joshi *et al, IEEE TED 69 (8): 4175-4182 (2022).*

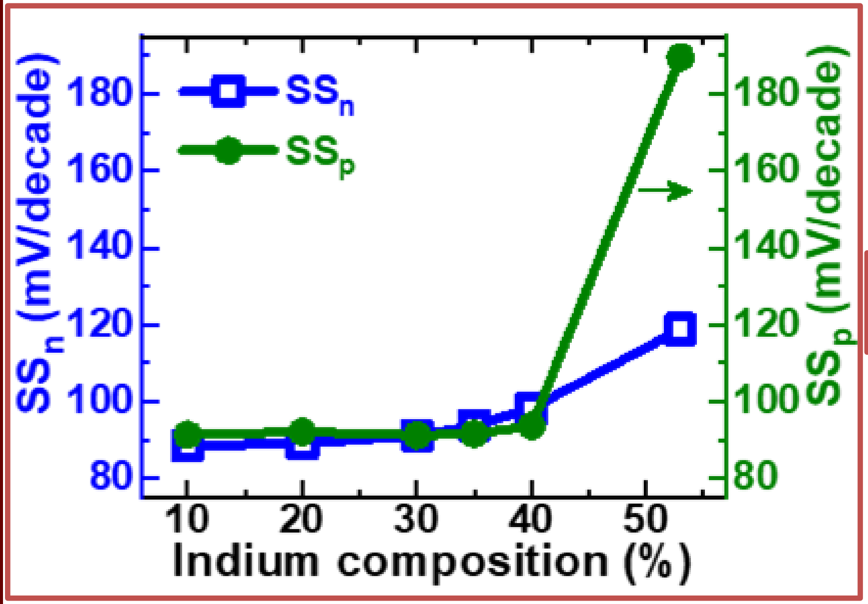
Ge/InGaAs FinFETs: ON/OFF Ratio

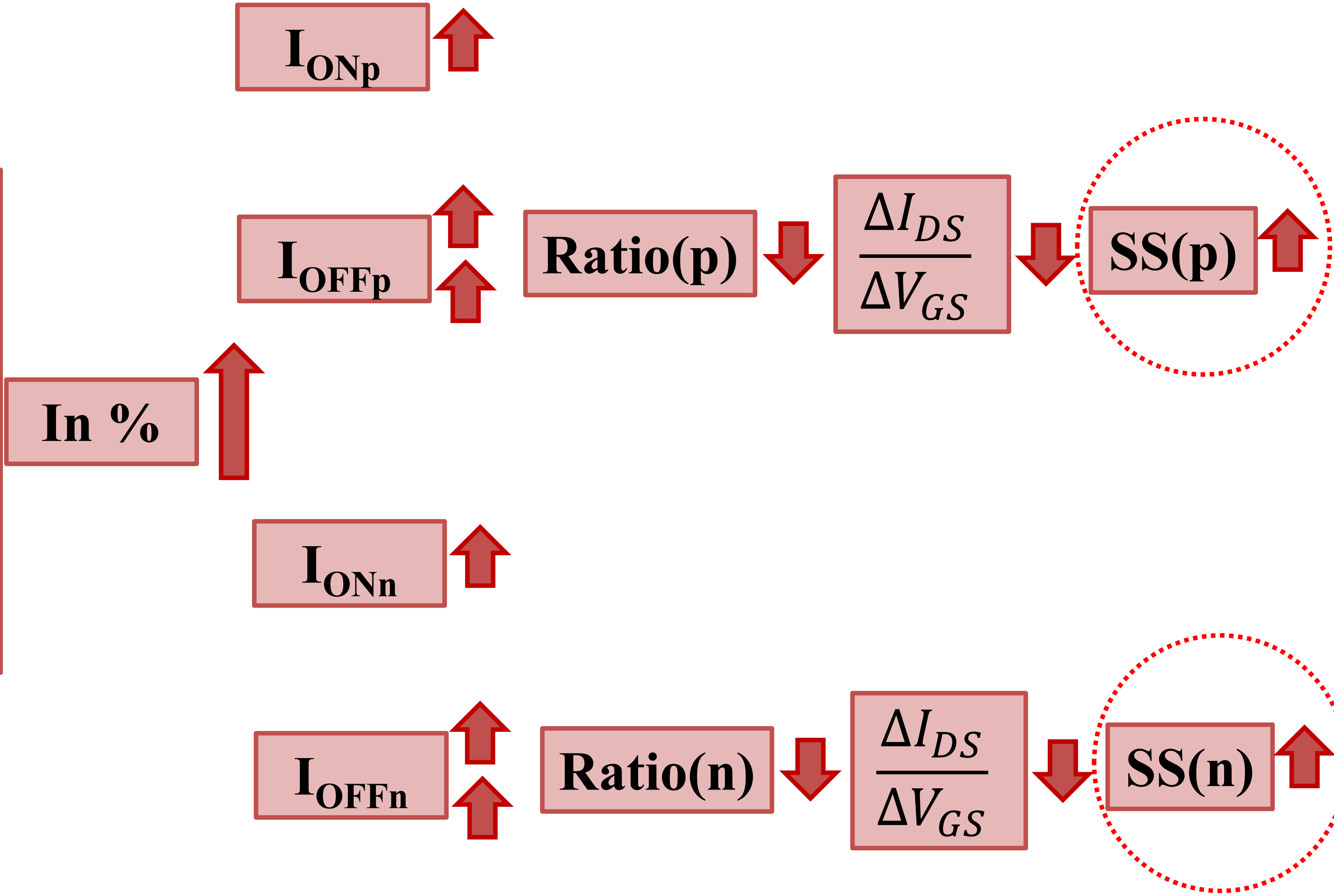
- I_{ON}/I_{OFF} ratio : Leakage and dissipation



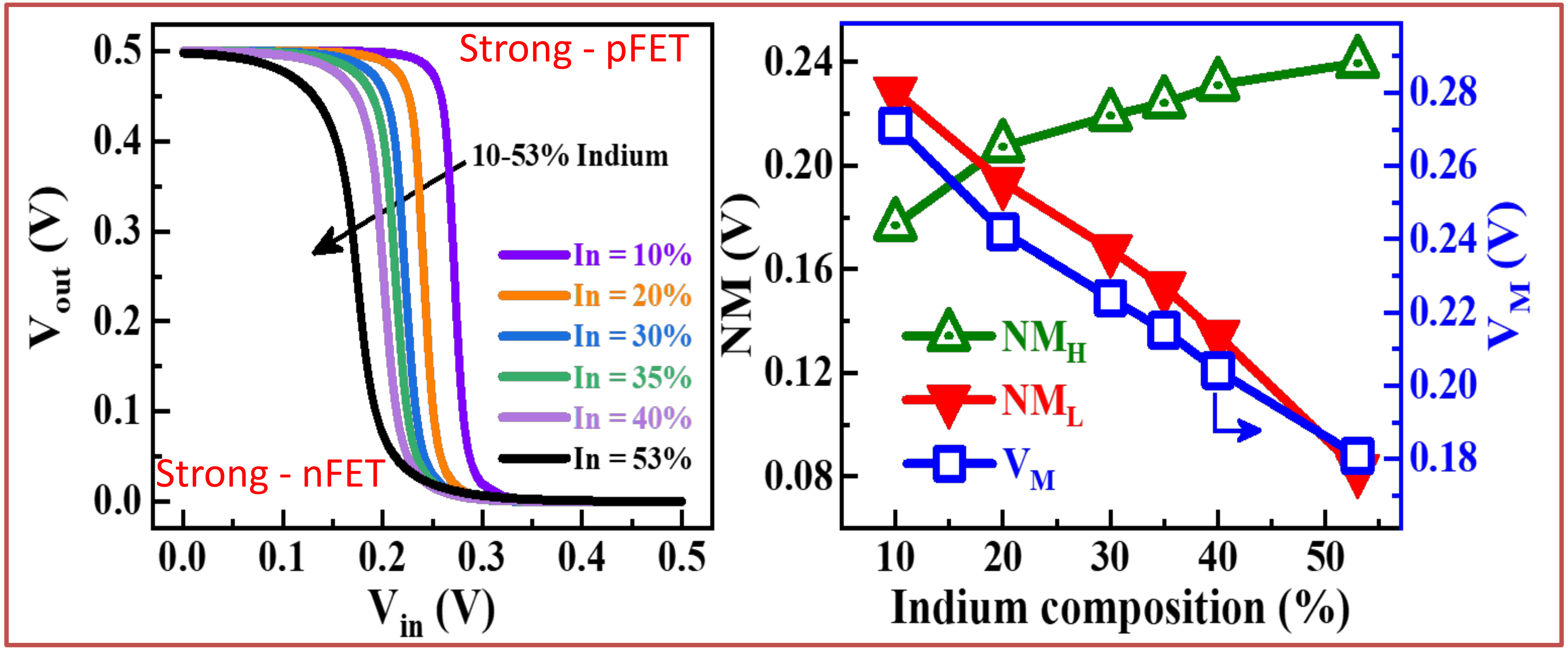
Ge/InGaAs FinFETs: Subthreshold Swing

- SS : Speed and Power





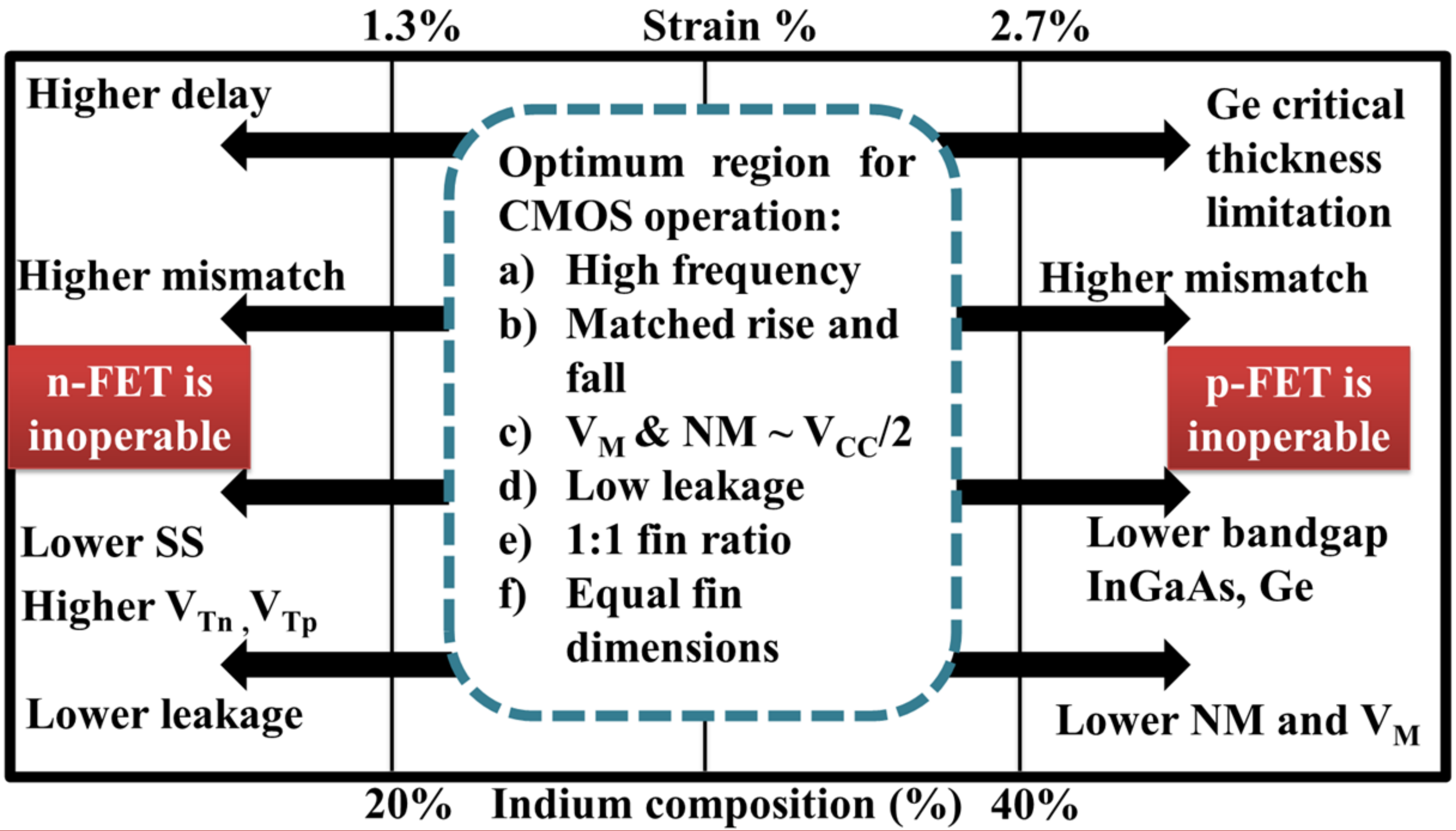
Ge/InGaAs CMOS: Inverter Characteristics



1. Sharp transition at 0.25V.
2. In = ~ 20 % is the region where response is most noise immune.

Rutwik Joshi *et al, IEEE TED 69 (8): 4175-4182 (2022).*

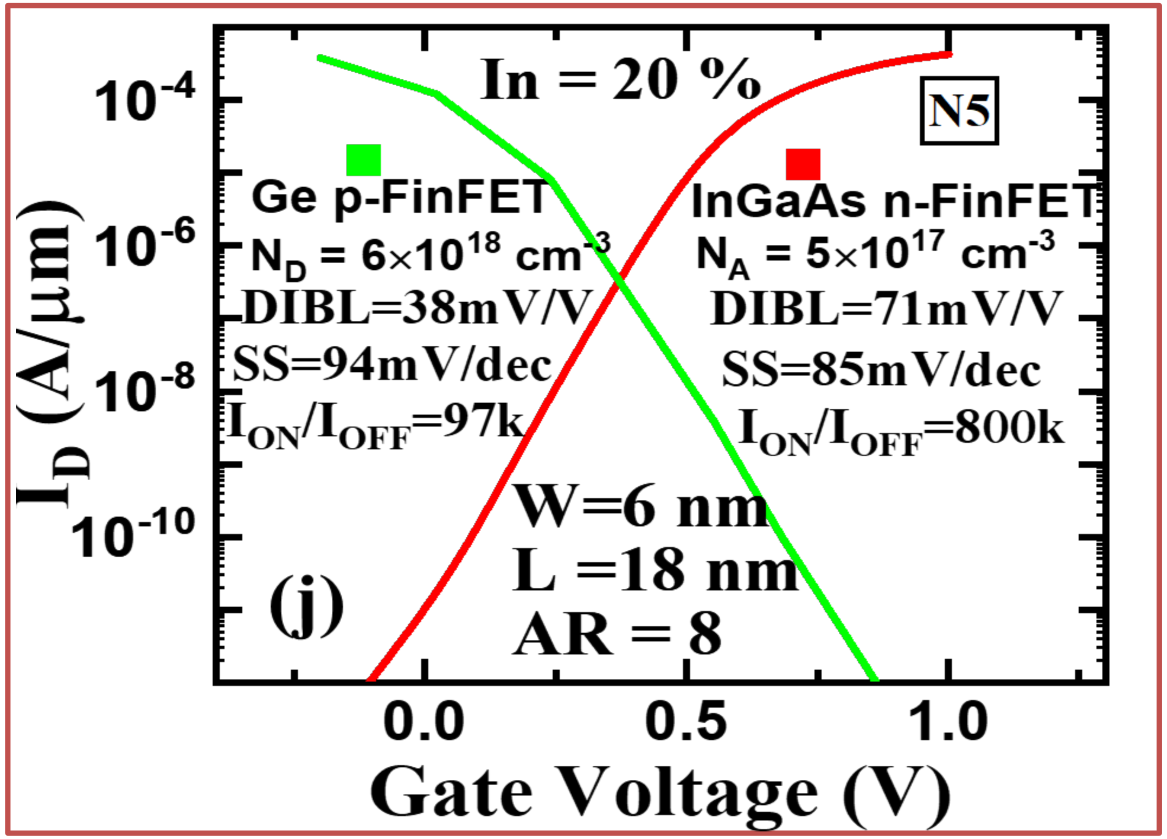
Summary: Ge/InGaAs CMOS



1. In =20 % is an optimum design choice in terms of CMOS performance
2. In compositions in InGaAs predicts the individual FinFET operation

Rutwik Joshi *et al, IEEE TED 69 (8): 4175-4182 (2022).*

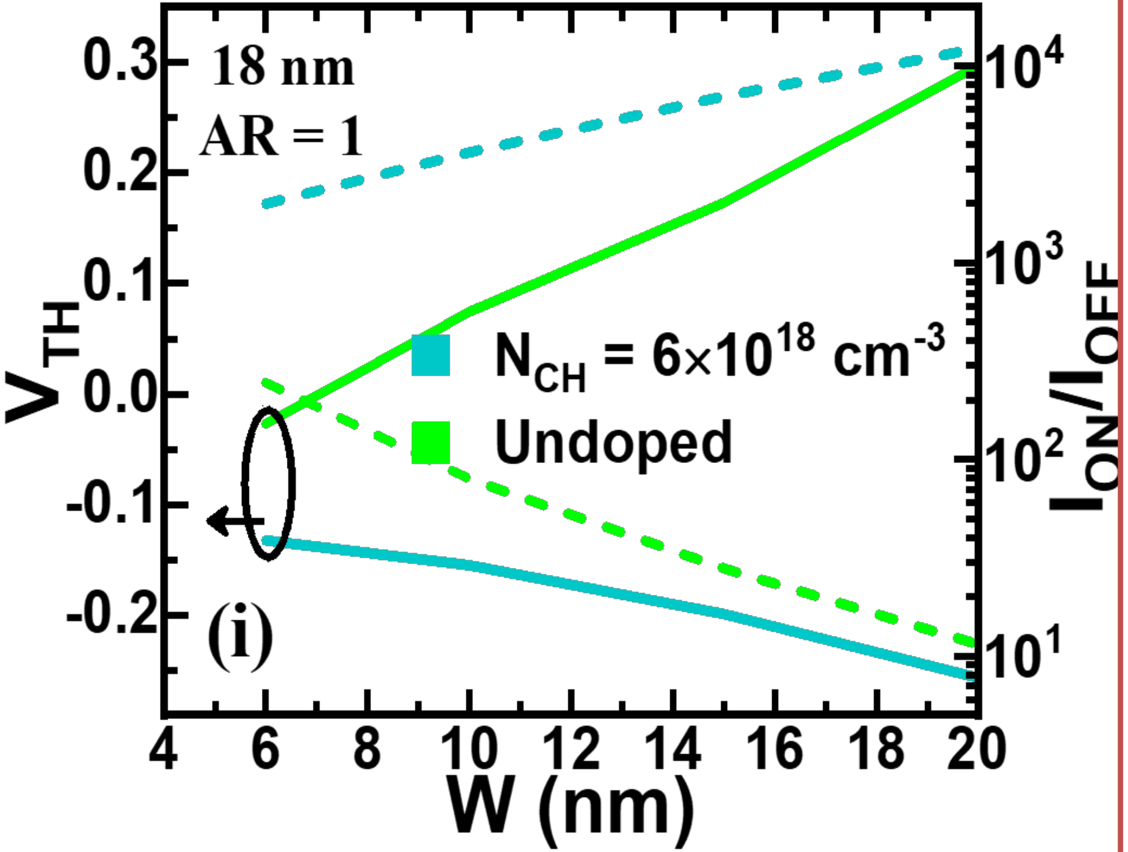
Ge/InGaAs CMOS at N5 Node with QC effect



1. Symmetric complementary response
2. Sharp transitions
3. A **relatively high doping in Ge** is needed due to low Eg to maintain negative V_T

Rutwik Joshi *et al, IEEE TED 69 (12): 6616-6623 (2022).*

QC Effect on Ge/InGaAs CMOS: Vth & ON/OFF Ratio

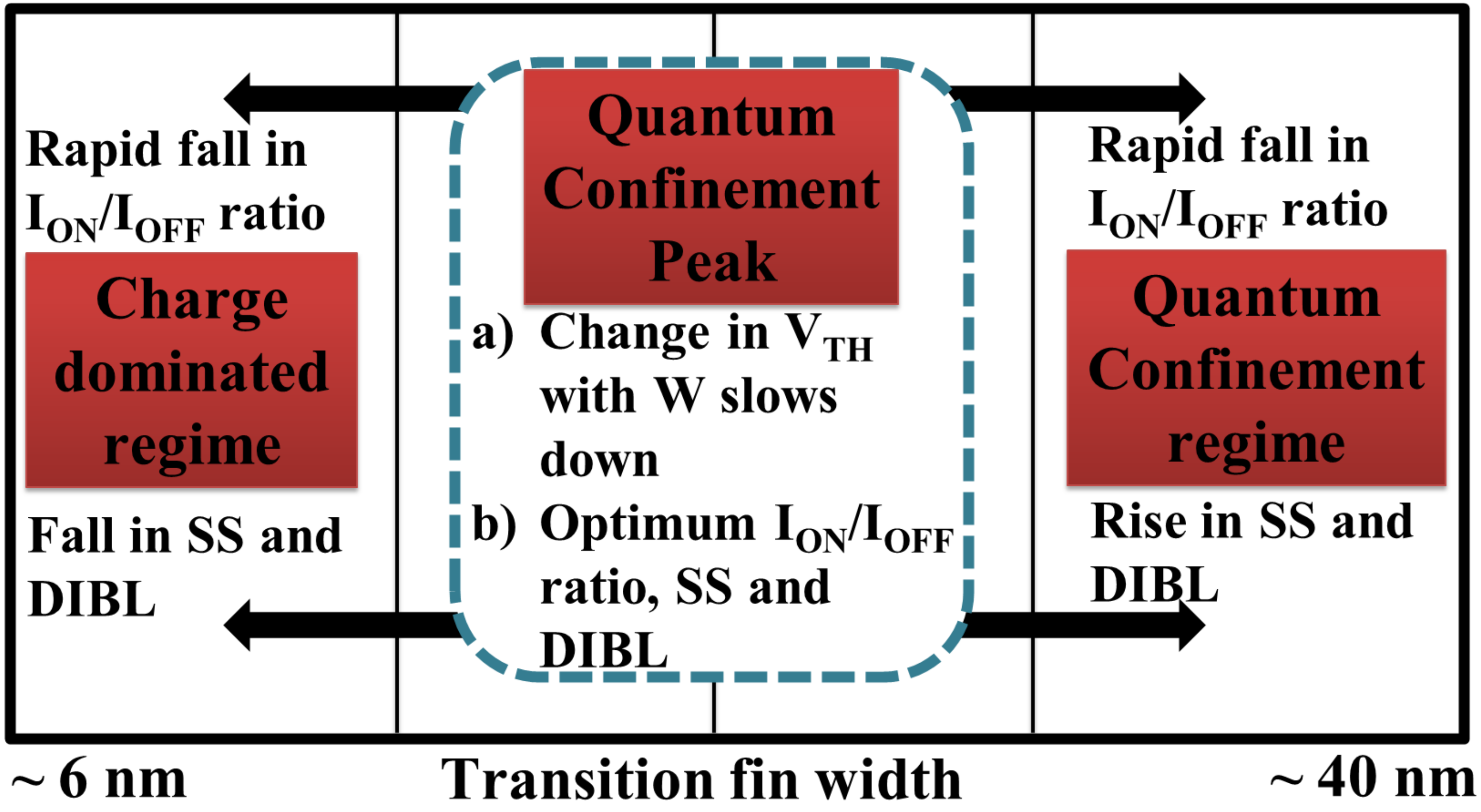


$$V_{TH} = V_{TH_i} + \frac{qN_{CH}\,w_d}{C_{ox}} + \Delta\varphi_{QM}(W)$$

Channel doping has a significant QC effect, so it must be treated as a design variable

Rutwik Joshi *et al, IEEE TED 69 (12): 6616-6623 (2022).*

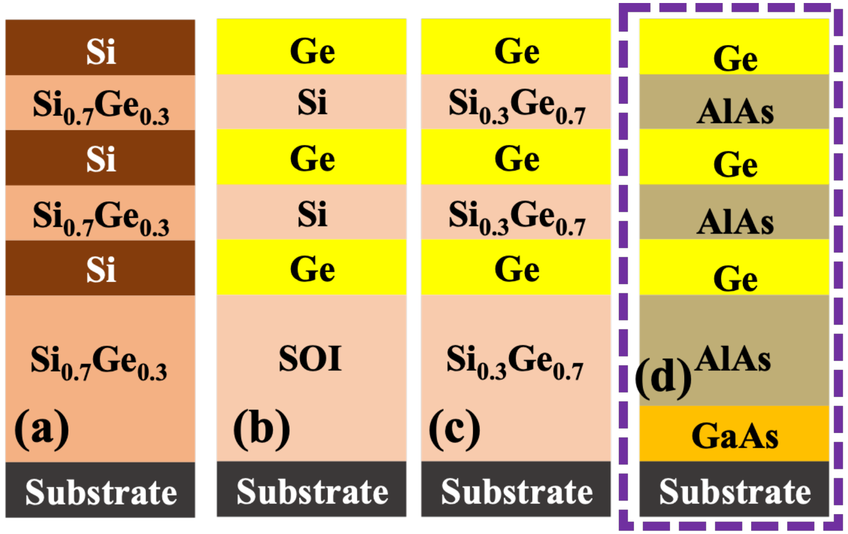
Summary: Effect of QC on Ge/InGaAs CMOS

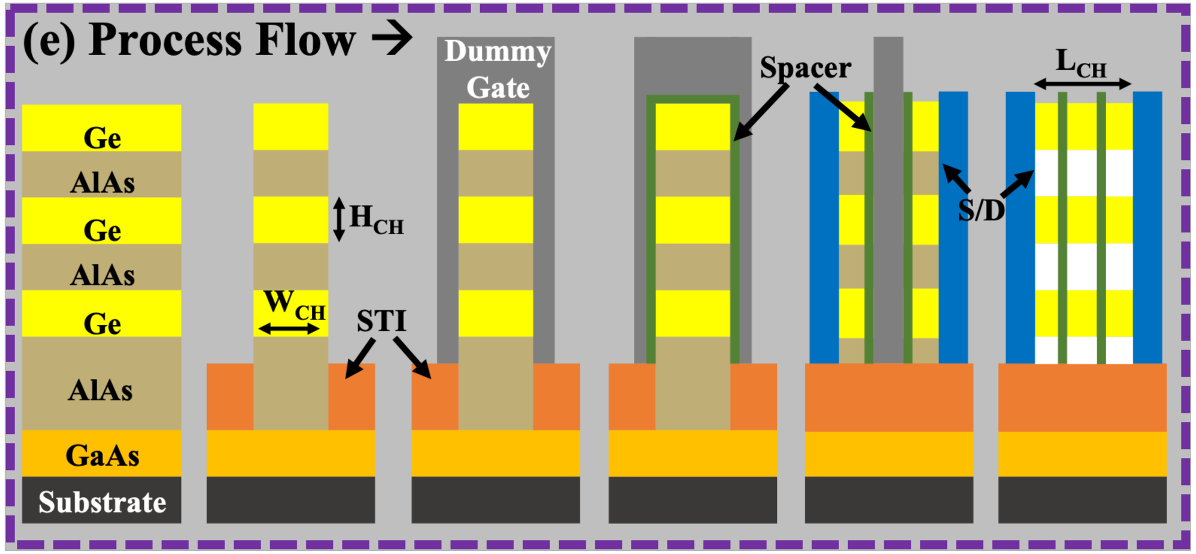


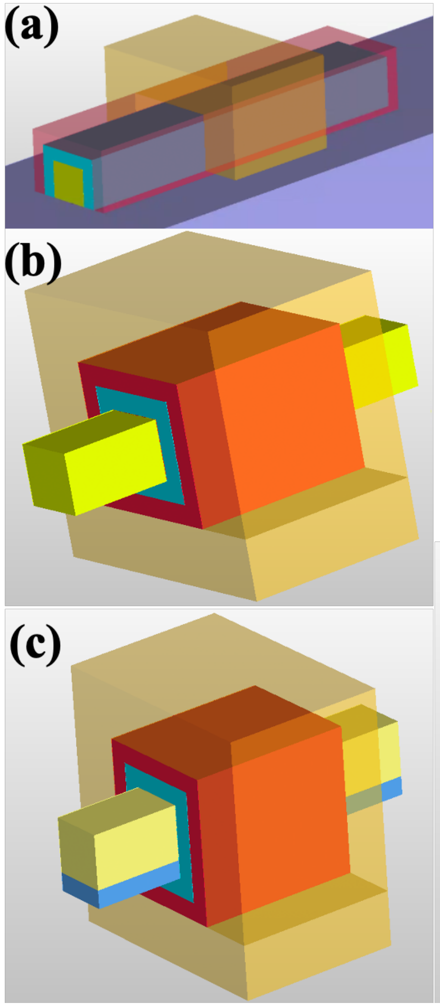
Rutwik Joshi *et al, IEEE TED 69 (12): 6616-6623 (2022).*

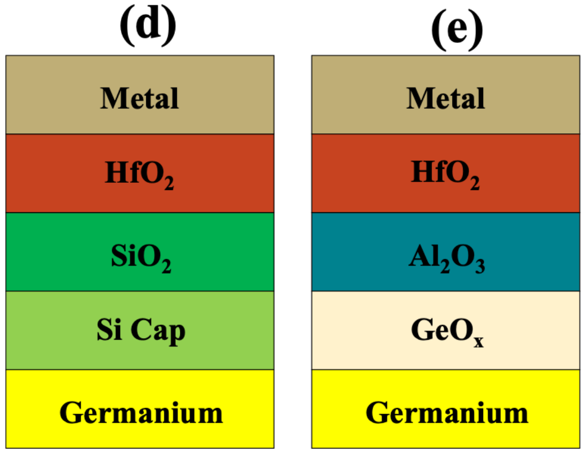
Ge NSFET

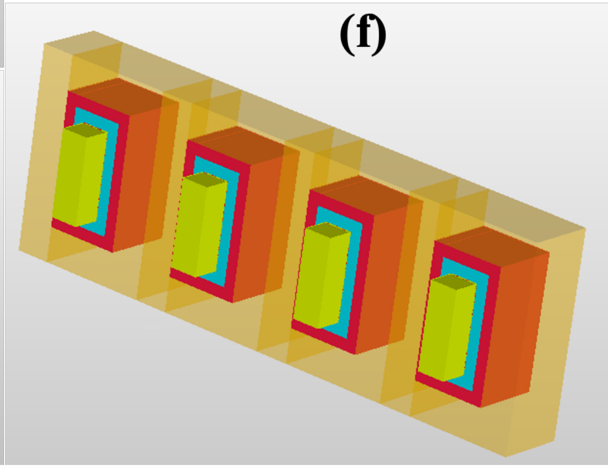
Ge Nanosheet FET on AlAs





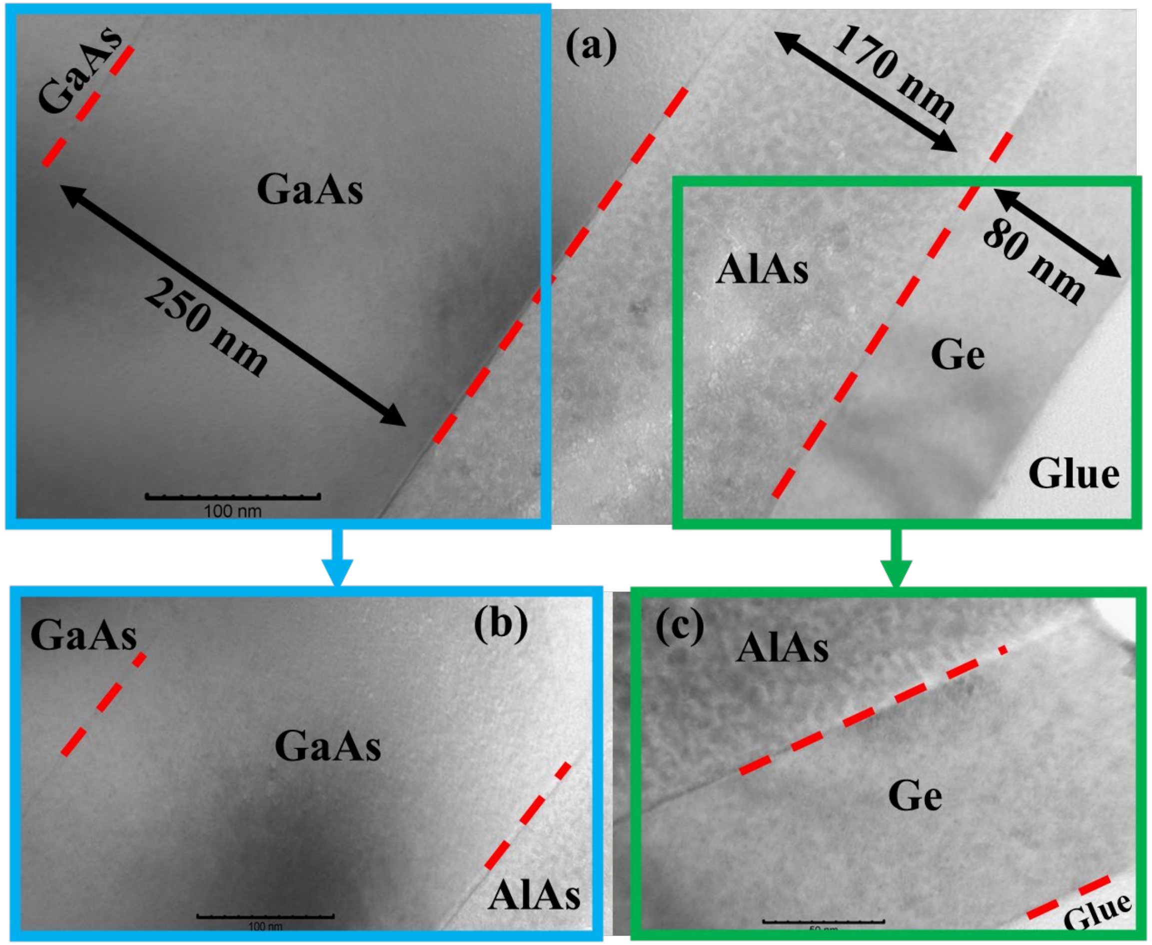






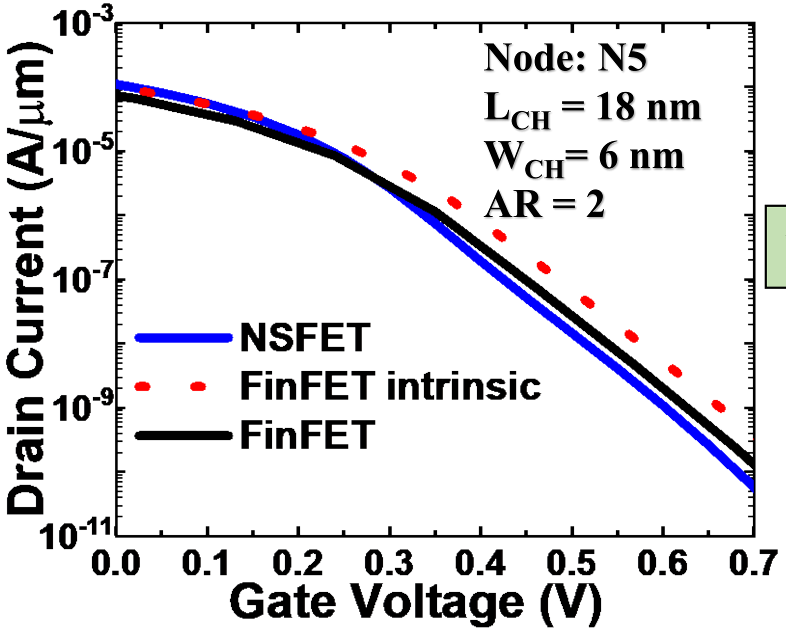
Rutwik Joshi *et al, IEEE TED 70 (3): 899-907 (2023).*

Ge Nanosheet FET on AlAs : TEM of Epitaxial Ge/AlAs



Rutwik Joshi *et al, IEEE TED 70 (3): 899-907 (2023).*

Ge Nanosheet FET Boost Over FinFET: Simulation



FinFET (Trigate)

12 % boost I_{ON} | 9.5 % boost SS

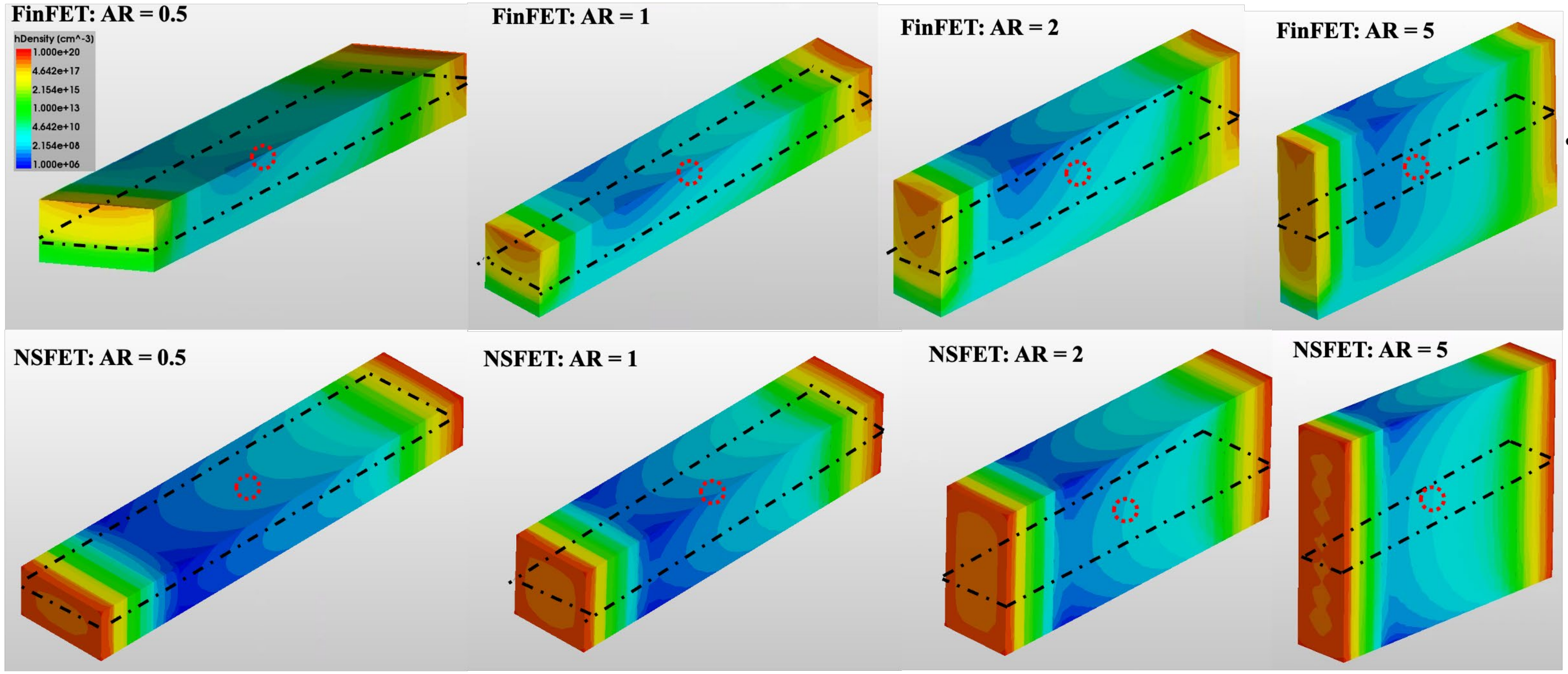
5.3x increase in I_{ON}/I_{OFF}

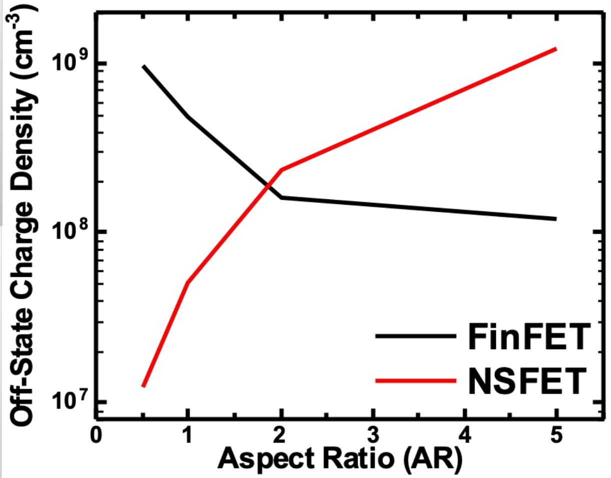
NSFET (Quad-gate/GAA)

Architecture	Work-function (eV)	Channel Type	On-Current (μA/μm)	SS (mV/dec)	Ratio	DIBL (mV/V)
FinFET	4.5	Doped	73.62	93	2.7k	37.7
FinFET	4.4	Undoped	98	95	1.4k	34
NSFET	4.4	Undoped	110	86	7.5k	42

Rutwik Joshi *et al, IEEE TED 70 (3): 899-907 (2023).*

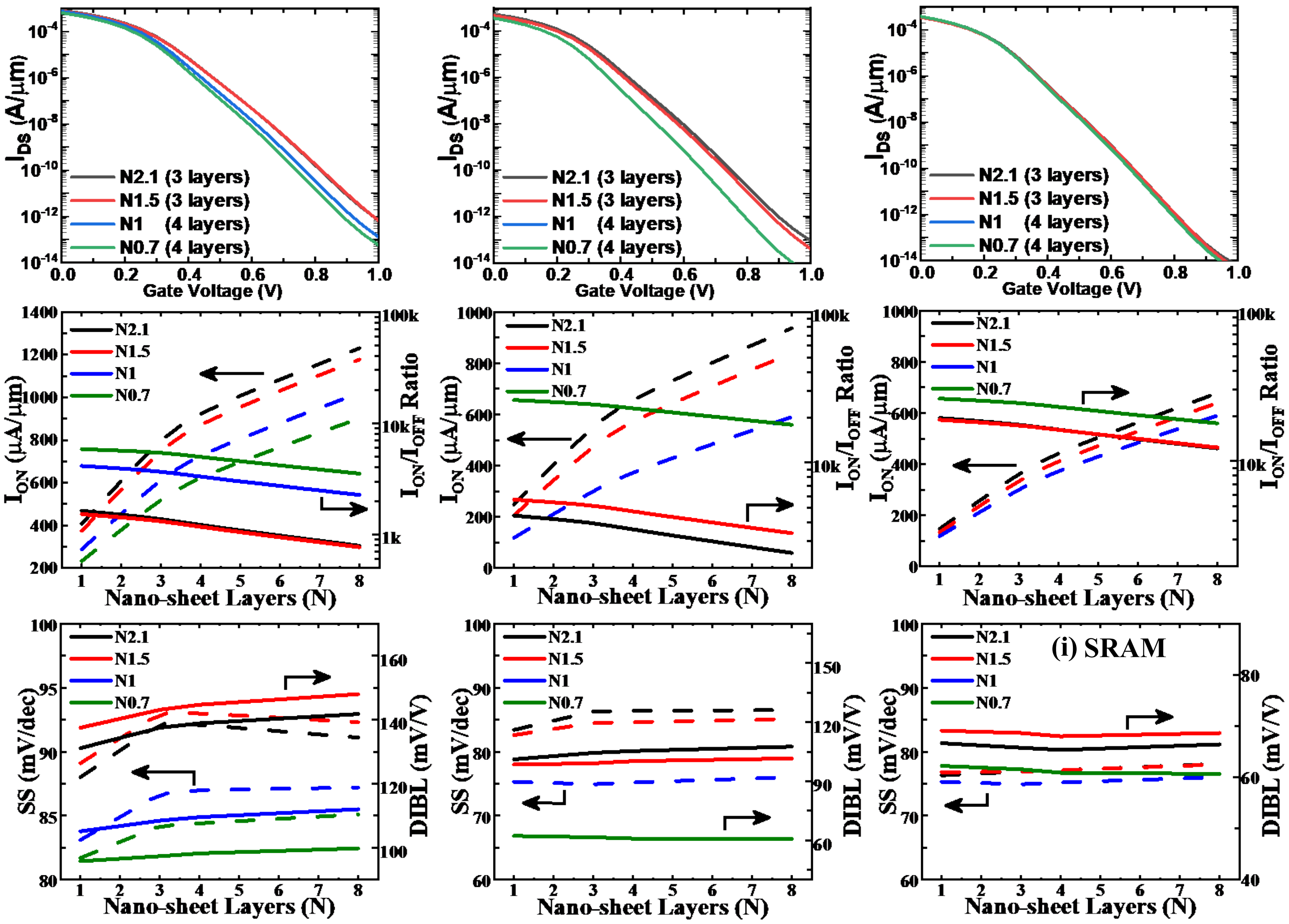
Ge Nanosheet FET vs FinFET: Leakage





Rutwik Joshi *et al, IEEE TED 70 (3): 899-907 (2023).*

Ge Nanosheet FET: HP, HD, SRAM Performances



Node	Nanosheet Dimensions (L,H,W) in nm
N2.1 HP	(14,7,30)
N2.1 HD	(14,7,15)
N2.1 SRAM	(14,7,7)
N1.5 HP	(12,6,25)
N1.5 HD	(12,6,11)
N1.5 SRAM	(12,6,6)
N1 HP	(12,5,20)
N1 HD	(12,5,6)
N1 SRAM	(12,5,6)
N0.7 HP	(12,5,15)
N0.7 HD	(12,5,6)
N0.7 SRAM	(12,5,6)

Rutwik Joshi *et al, IEEE TED 70 (3): 899-907 (2023).*

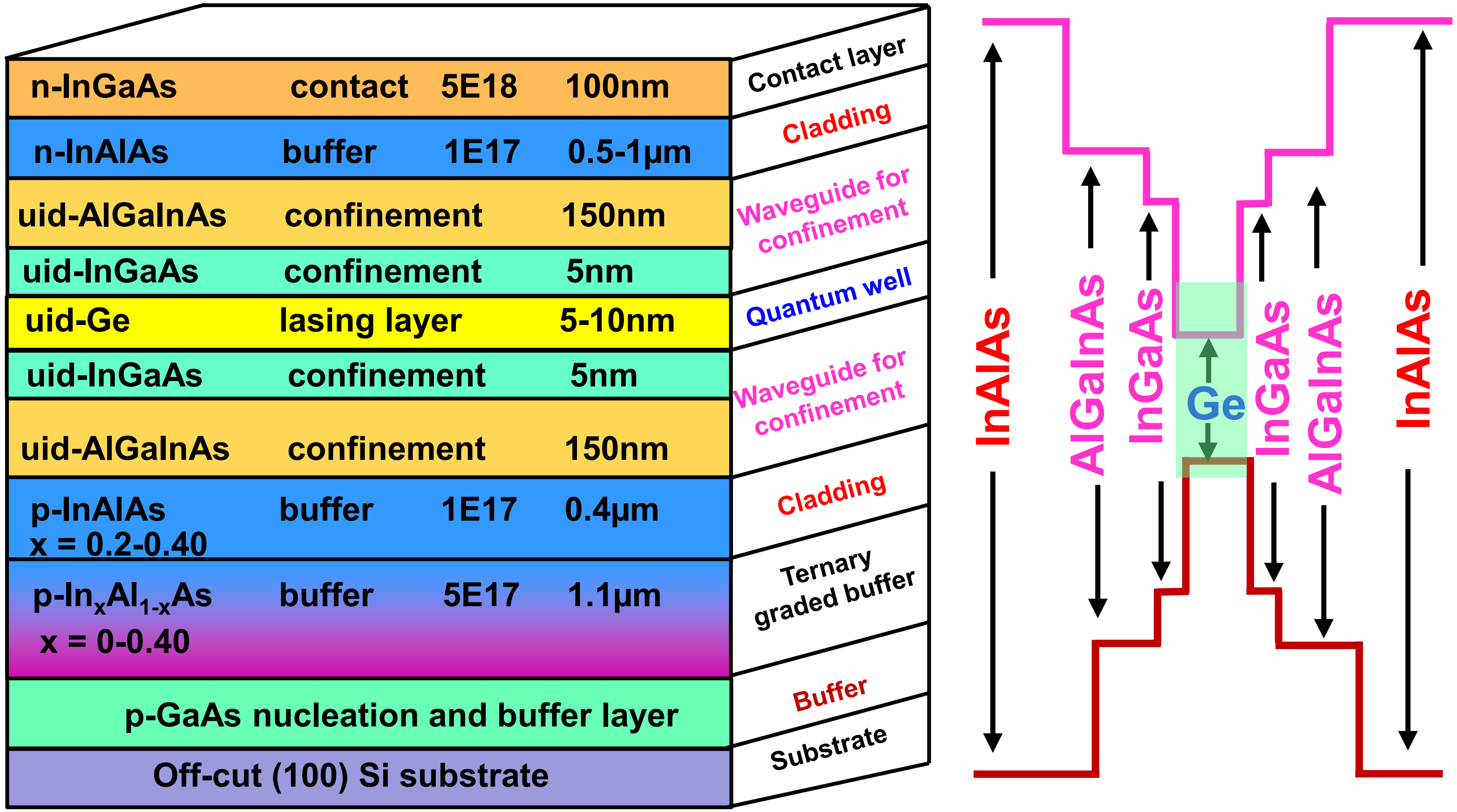
Ge Nanosheet FET: Benchmarking

Ref.	Material	Architecture (p-FET)	L (nm)	W [or D] (nm)	H [or D] (nm)	No. of sheets [or wire]	I_{ON} (µA/µm)	I_{ON}/I_{OFF}	SS (mV/dec)	Supply (V)
[12] and [17]	Ge	NSFET	90	80	40	3	1650	10^4	130	1
	Ge	NSFET	90	80	40	1	717	10^5	105	1
[33]	Si	NSFET	45	30	8	7	3000	10^6	64	1
[9]	ε-Ge	Nanowire	45	13	13	1	500	10^3	75	0.5
[34]	GeSn	GAA	40	20	5	3	58	–	110	0.5
[36]	SiGe	NSFET	25	100	5	1	508	5×10^3	79	0.5
	SiGe	NSFET	55	100	5	1	300	3×10^3	67	0.5
[36]	GeSn	NSFET	90	30	2.4	8	170	1.6×10^7	64	0.5
[37]	GeSn	NSFET	120	87	12	4	42	2×10^4	89	0.5
[38]	Ge	Nanowire	40	9	9	2	524	5.24×10^3	81	0.5
This work (N5)										
NSFET A	Ge	NSFET	18	6	6	1	69	2.18×10^4	78	0.5
NSFET B	Ge	NSFET	18	6	6	1	99	6.32×10^4	70	0.5
NSFET C20	ε-Ge	NSFET	18	6	6	1	129	5.34×10^3	80	0.5
NSFET C40	ε-Ge	NSFET	18	6	6	1	221	1.07×10^3	81.2	0.5

Rutwik Joshi *et al, IEEE TED 70 (3): 899-907 (2023).*

Strained Ge Photonics

Structural Design of Tensile Strained Tunable ε-Ge/InGa(Al)As

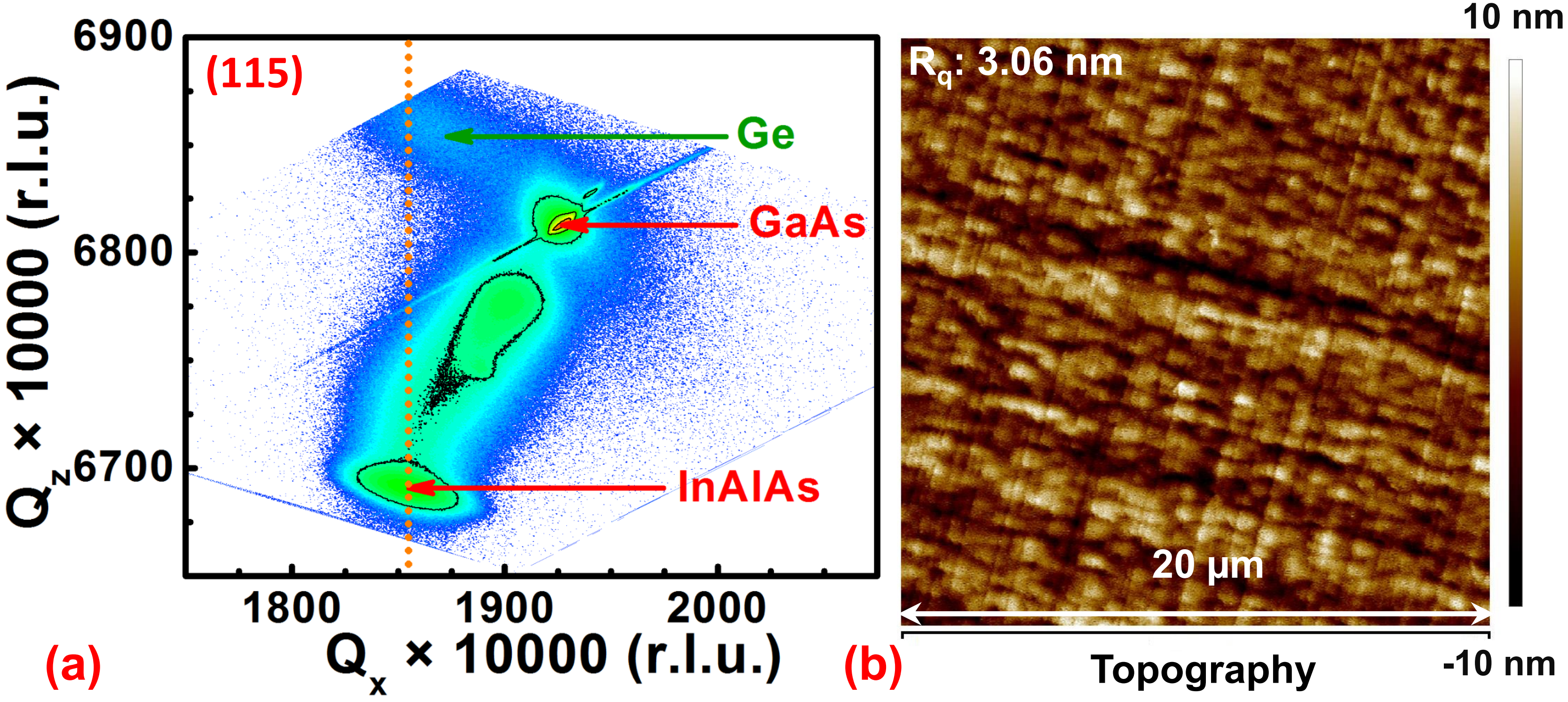


Increase strain in Ge

Direct band gap

M. Hudait *et al*, *ACS Appl. Electron. Mater., 10(3): 4535-4547 (2021)*

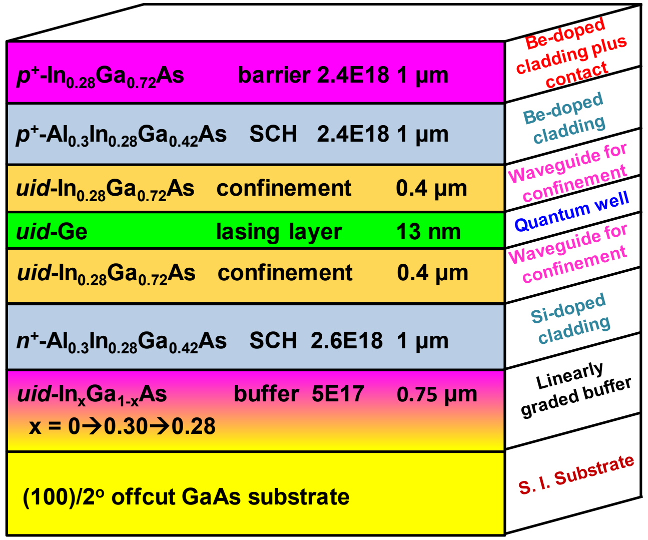
ε-Ge on GaAs with Graded $In_xAl_{1-x}As$ Buffer: X-ray and AFM

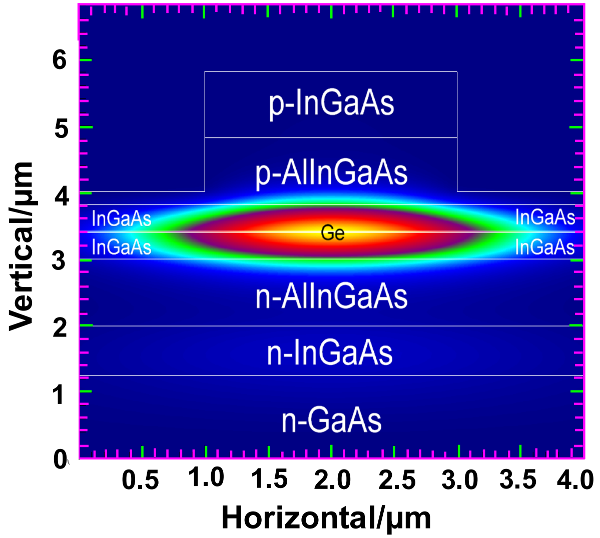


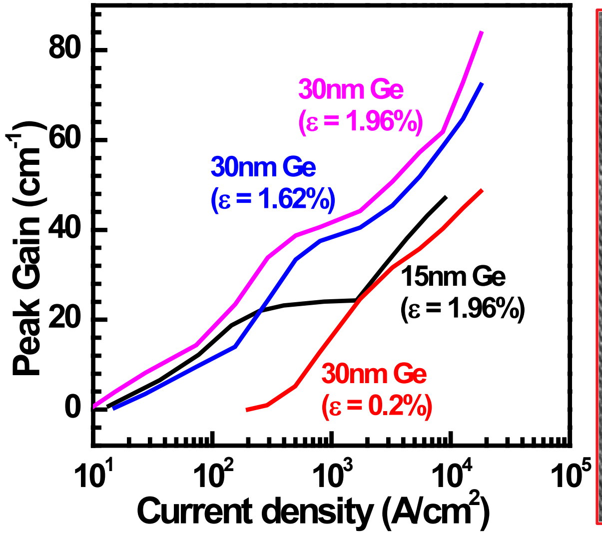
- (115) reciprocal space map exhibited tensile strained Ge on InAlAs
- AFM morphology demonstrate the cross-hatch morphology

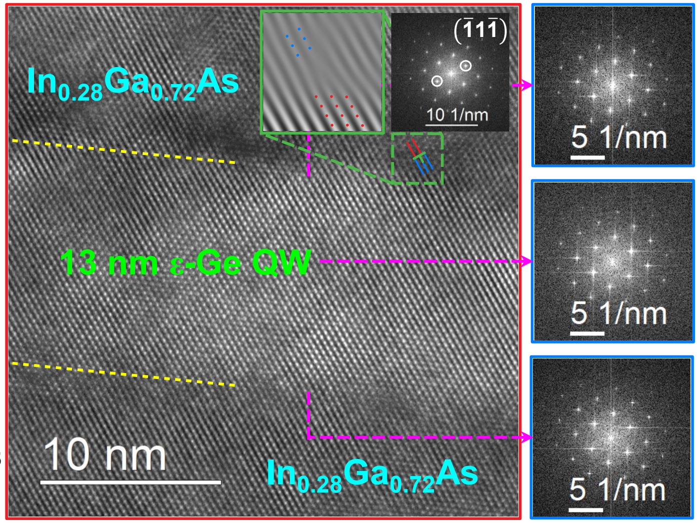
M. Clavel et al, ACS Omega (2022)

InGaAs/ε-Ge/InGaAs QW Laser Structure



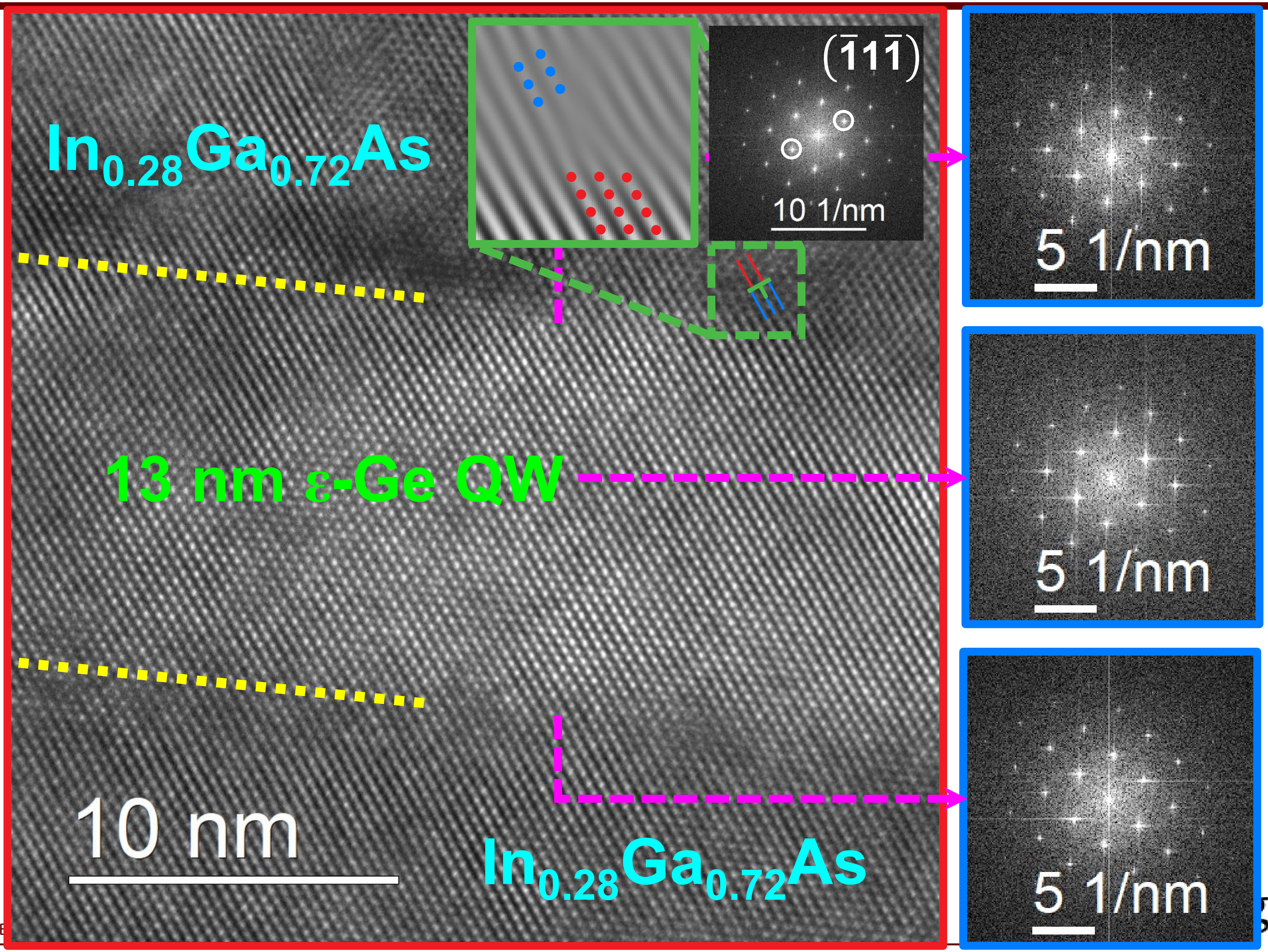




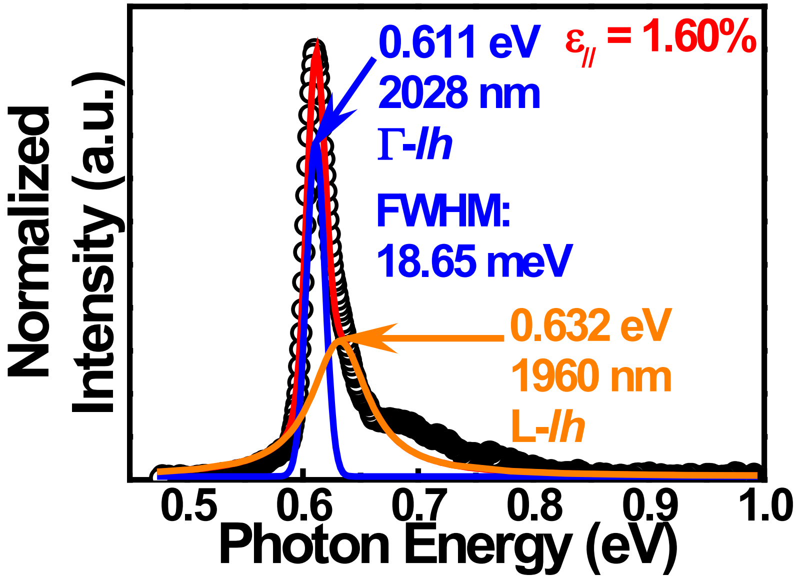


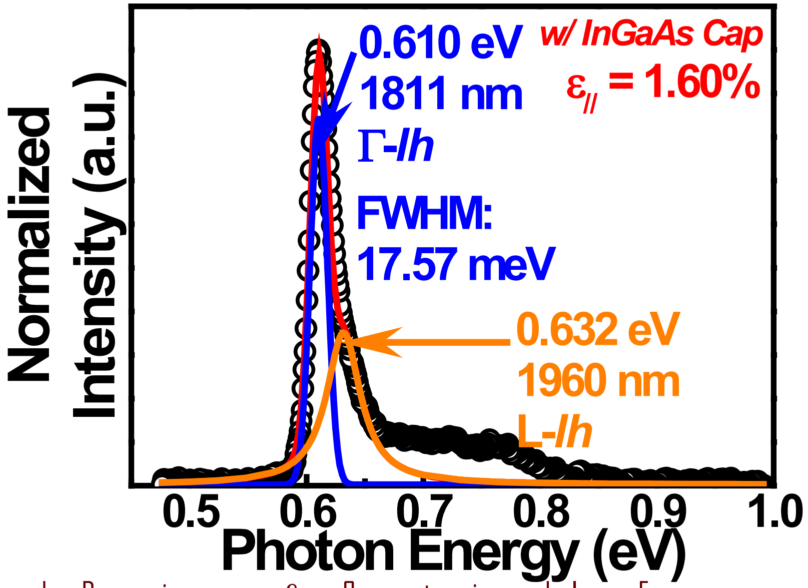
M. Hudait *et al, ACS Appl. Electron. Mater., 10(3): 4535-4547 (2021)*

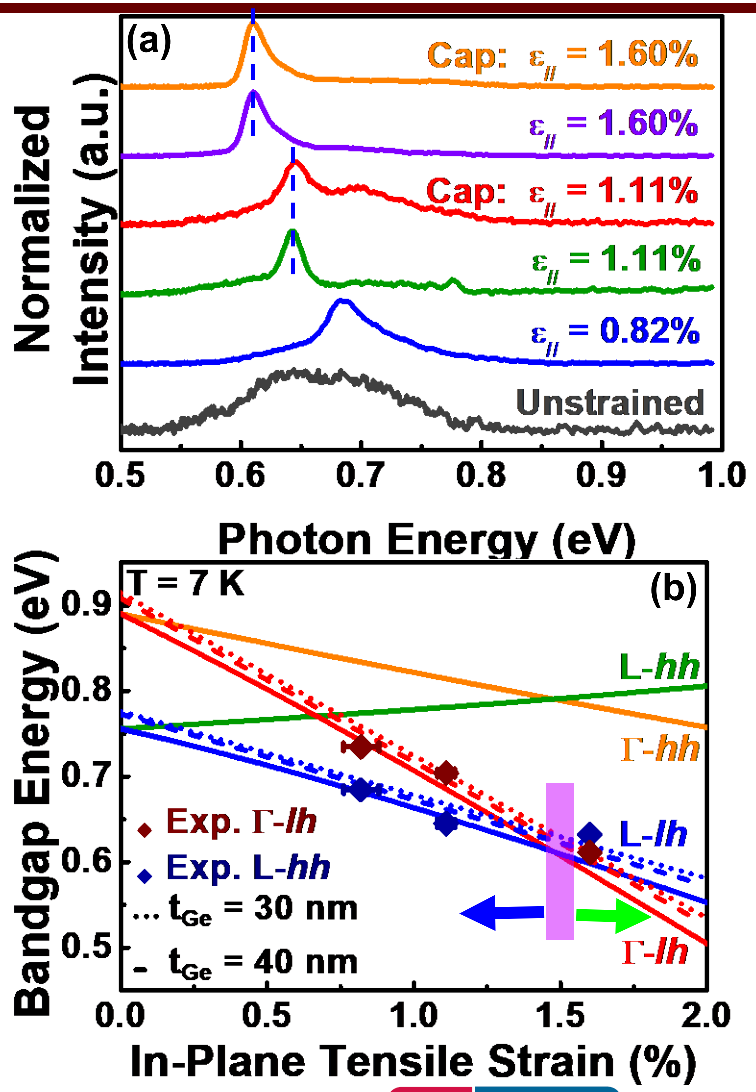
XTEM Analysis of InGaAs/ε-Ge/InGaAs QW Laser Structure



PL Analysis: Strain-Induced PL Peak Red-shifts

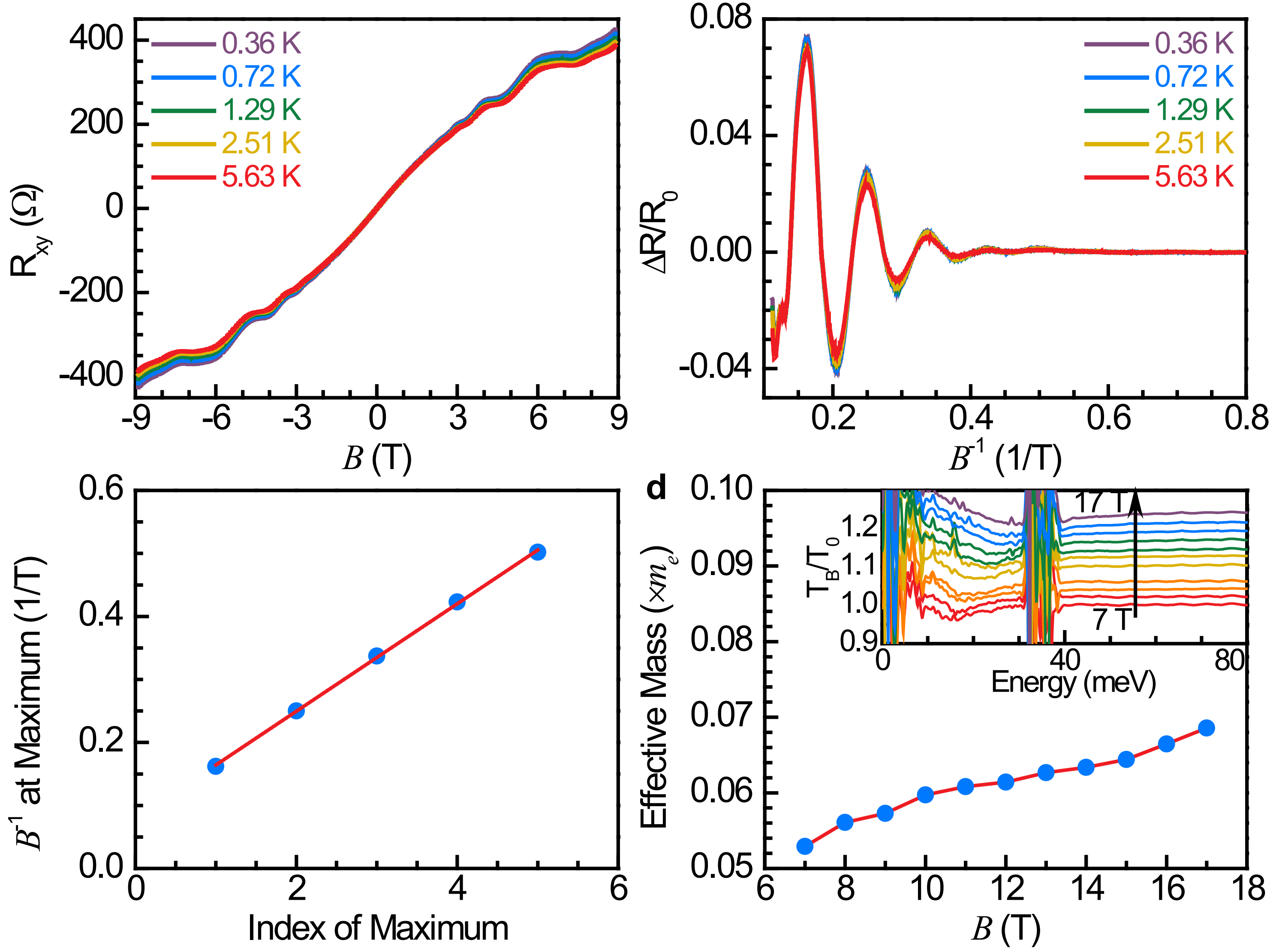






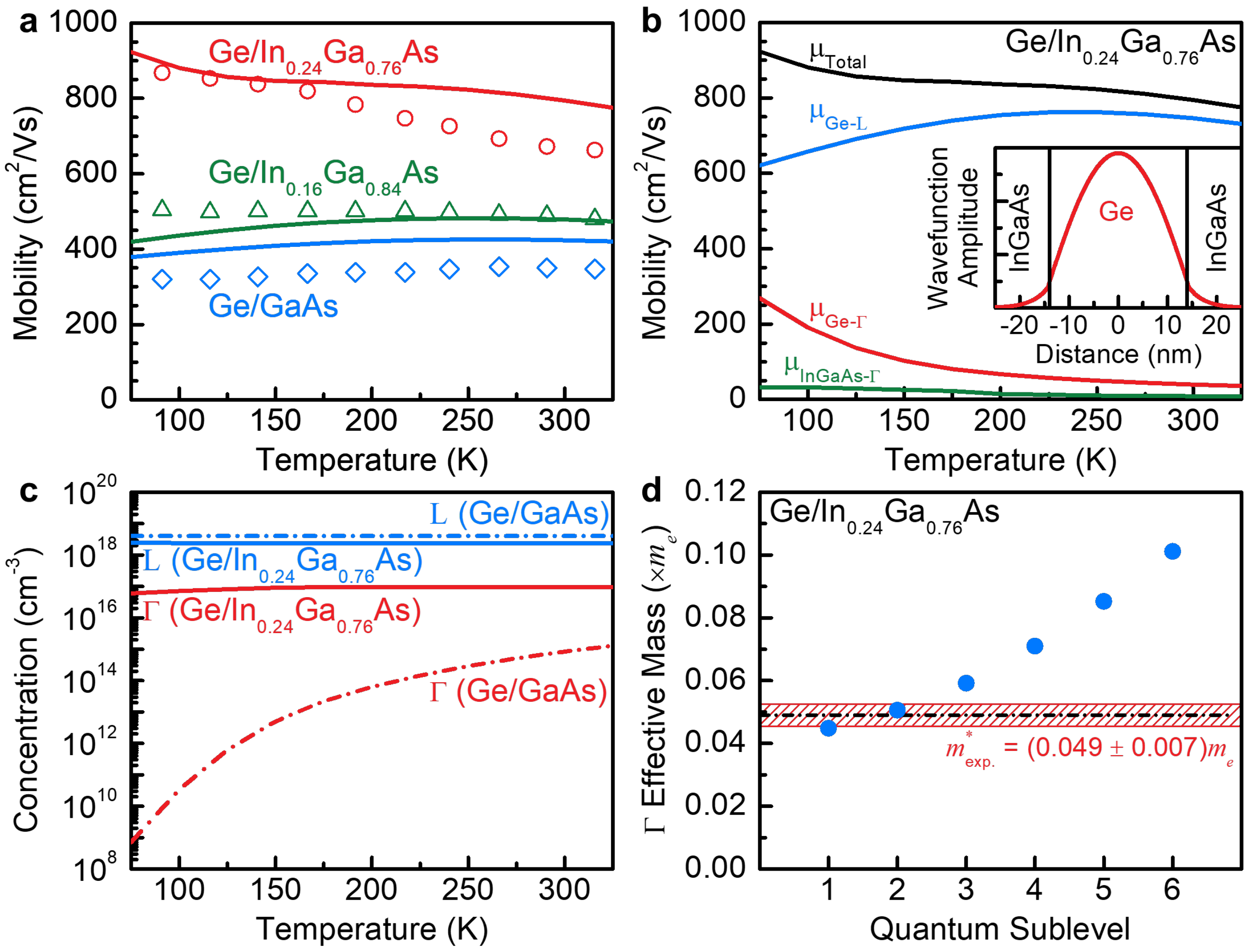
M. Clavel et al, ACS AMI (2015)

Magnetotransport Study of 1.6% ε-Ge



M. B. Clavel *et al*, *Phys. Rev. Appl.* ,2022, **18**, 064083-1-12.

Carrier Transport (Mobility & density): Ge and Tunable ε-Ge



1.6% ε-Ge on $In_{0.24}Ga_{0.76}As$

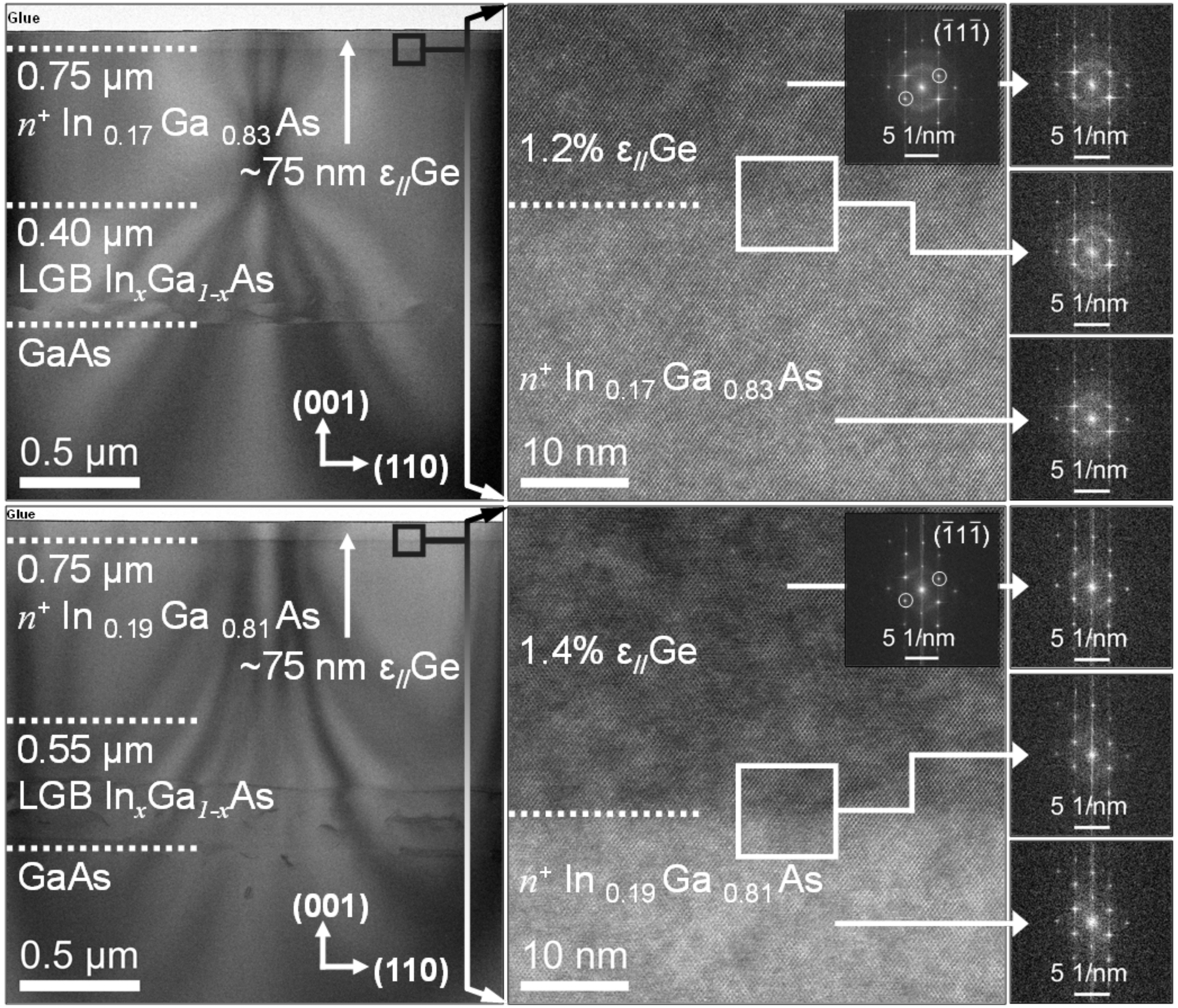
- ☑ 2 × μ_n boost compared to unstrained Ge
- ☑ Increase in mobility of L-valley electrons !!
- ☑ Carriers are confined within the 1.6 % ε-Ge
- ☑ No mobility contribution from underlying $In_{0.24}Ga_{0.76}As$ stressor layer
- ☑ Effective mass of 0.049 m_e

M. B. Clavel *et al*, *Phys. Rev. Appl.* ,2022, **18**, 064083-1-12.

Defect Microstructures : Epitaxial Tunable ε-Ge

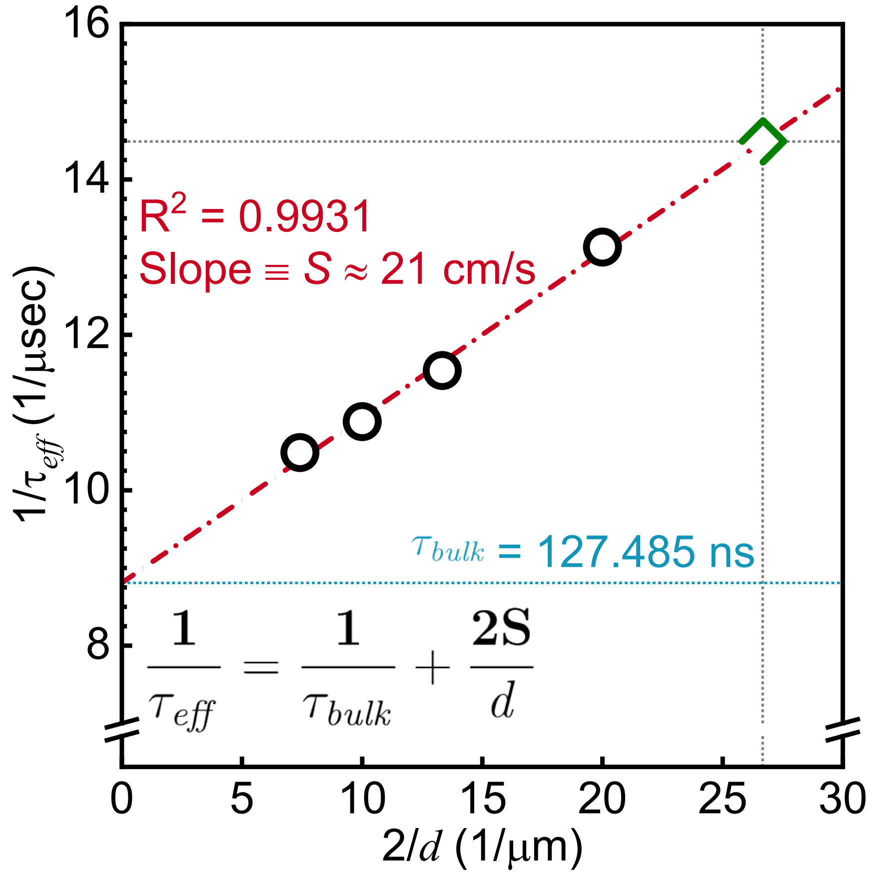
1.2% ε-Ge

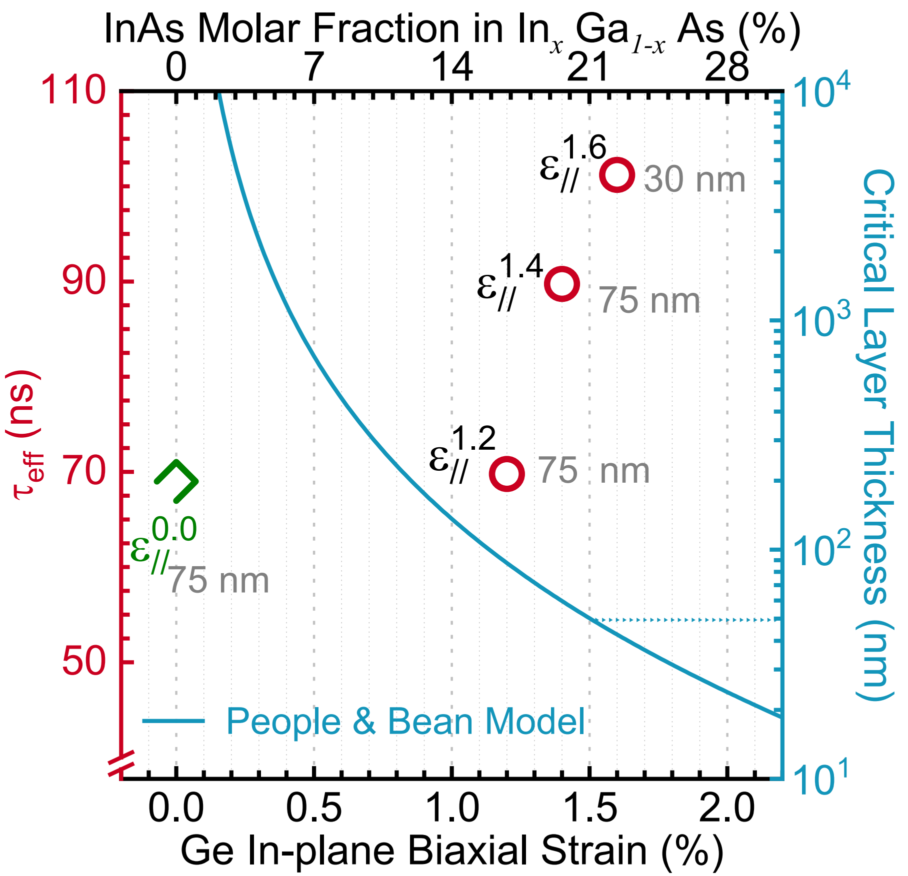
1.4% ε-Ge



S. Bhattacharya *et al, ACS Appl. Electronic Materials (Under Review, 2023)*

Carrier Recombination: Ge & Tunable ε-Ge





☑ SRV of 21 cm/s was achieved from unstrained Ge

☑ Bulk lifetime of ~127 ns was determined

☑ Carrier lifetime increases with increasing strain

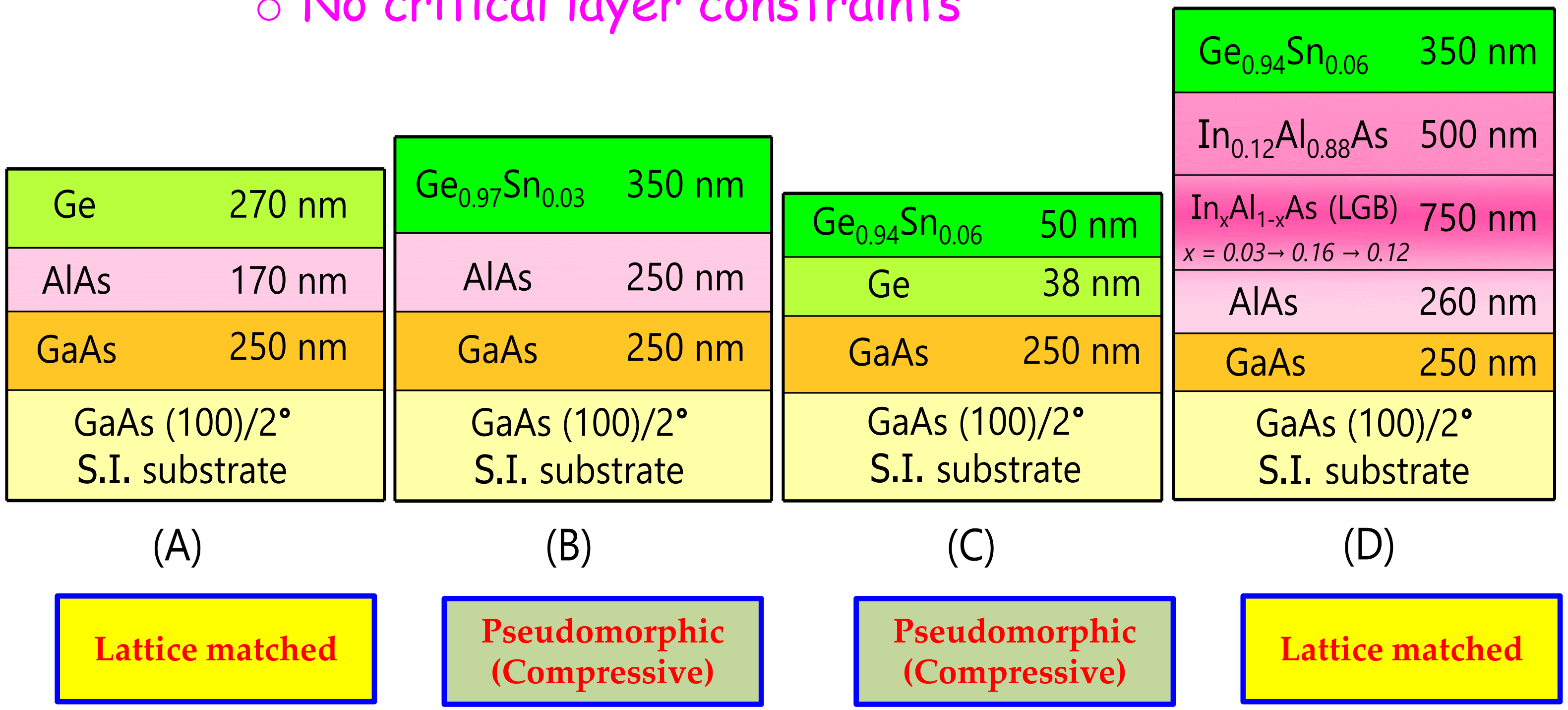
S. Bhattacharya *et al, ACS Appl. Electronic Materials (Under Review, 2023)*

GeSn Photonics

Epitaxial GeSn Material Synthesis

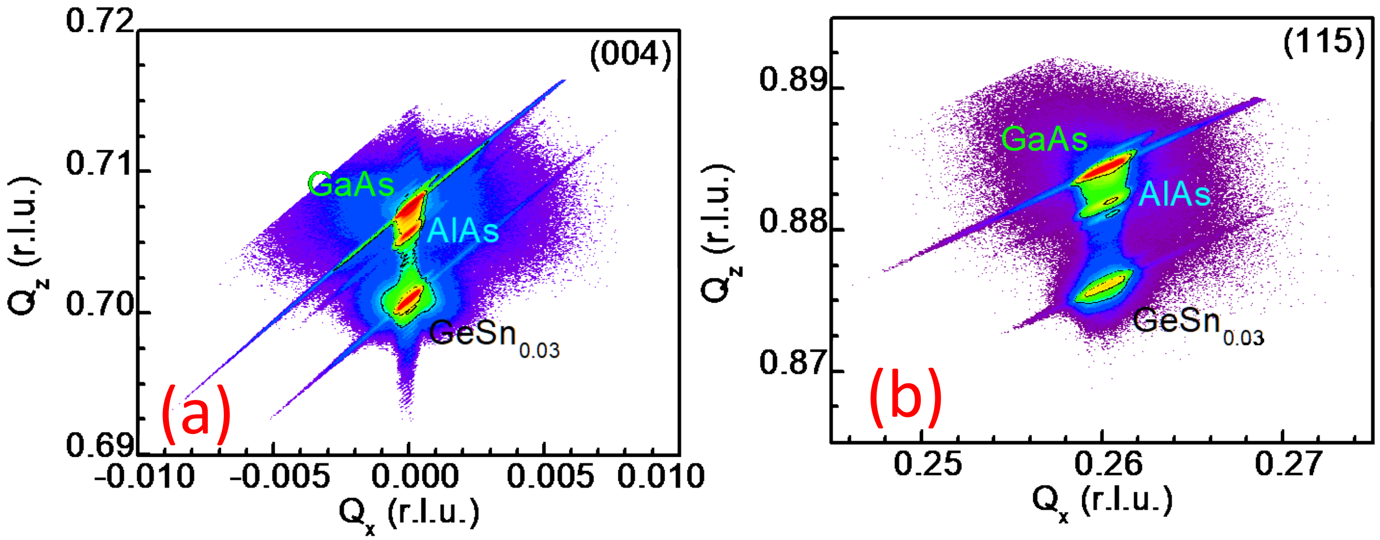
$Ge_{1-y}Sn_y$ grown on $In_xAl_{1-x}As$

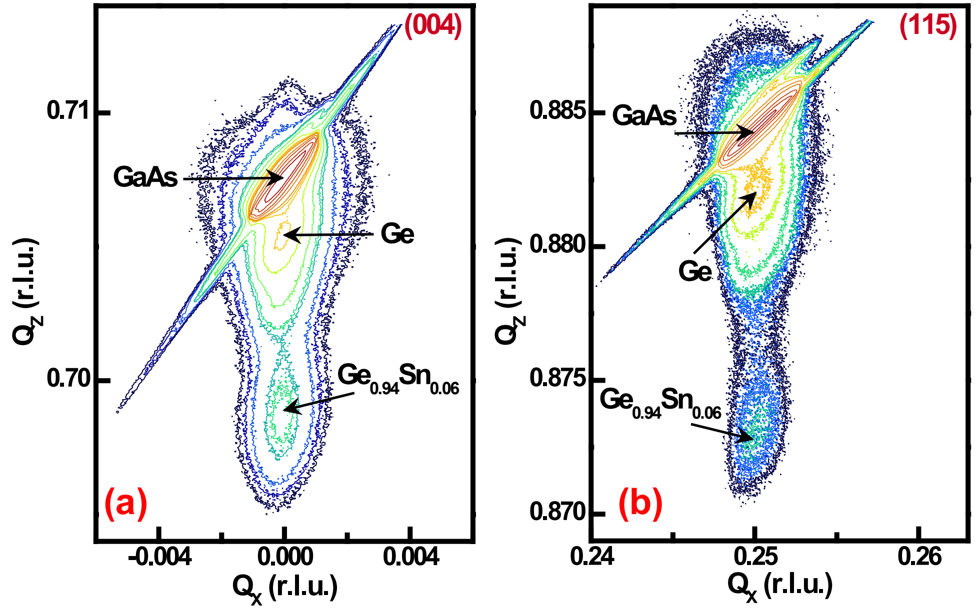
- ☑ Large band offsets
- ☑ Superior confinement
- ☑ Lattice matched (virtually defect-free)
  - No critical layer constraints



0-6% Sn in GeSn/In(Al)As

Material Analysis of GeSn: X-ray RSMs





Sample B

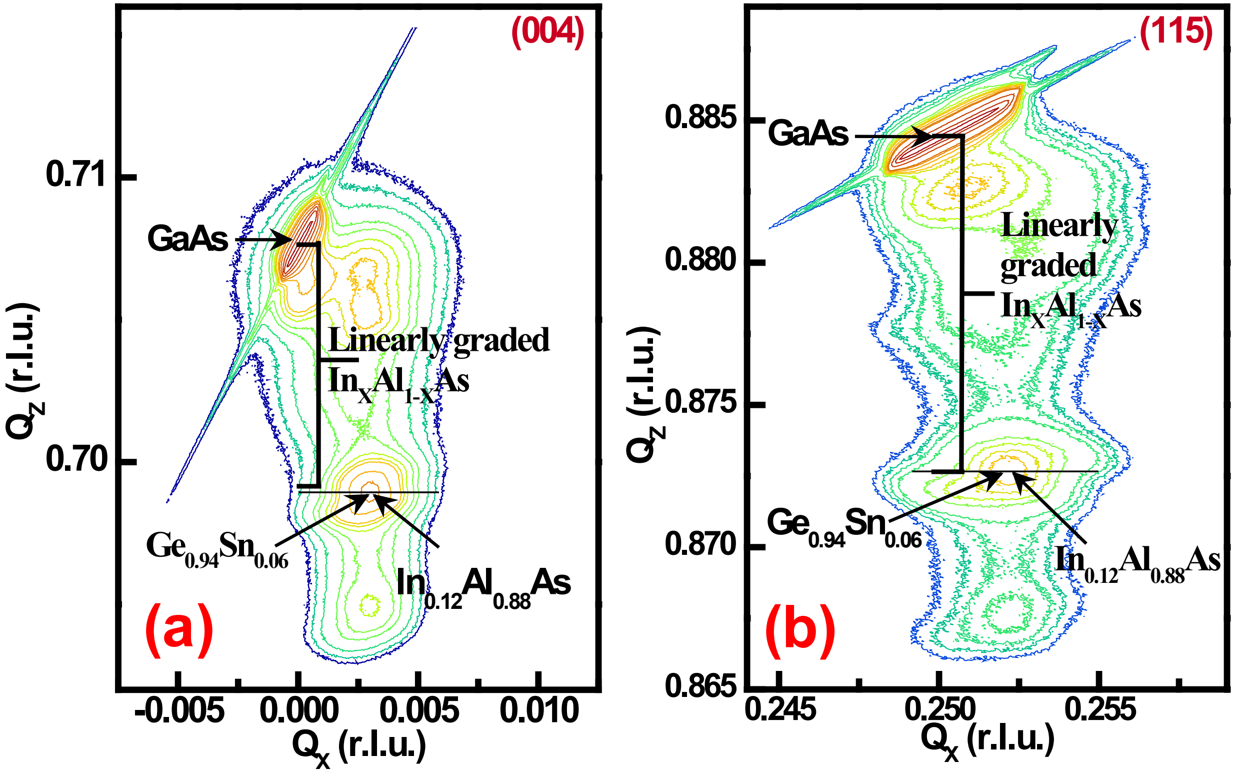
$Ge_{0.97}Sn_{0.03}$	350 nm
AlAs	250 nm
GaAs	250 nm
GaAs (100)/2° S.I. substrate	

Sample C

$Ge_{0.94}Sn_{0.06}$	50 nm
Ge	38 nm
GaAs	250 nm
GaAs (100)/2° S.I. substrate	

M. K. Hudait *et al.*, *JMC-C*, 2022, **10**, 10530–10540.

X-ray Analysis of Lattice matched $GeSn_{0.06}/In_{0.12}AlAs$



Sample D

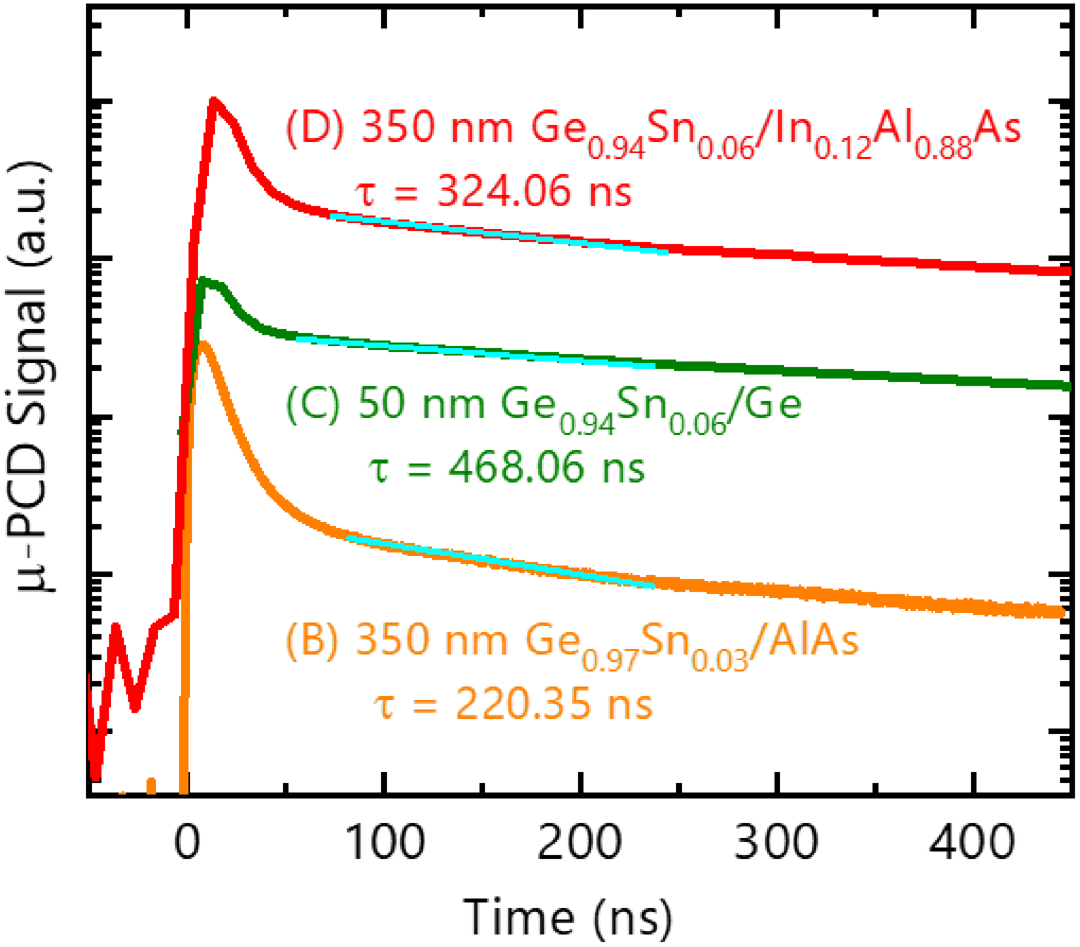
Layer	Thickness
$Ge_{0.94}Sn_{0.06}$	350 nm
$In_{0.12}Al_{0.88}As$	500 nm
$In_xAl_{1-x}As$ (LGB) *x = 0.03→ 0.16 → 0.12*	750 nm
AlAs	260 nm
GaAs	250 nm
GaAs (100)/2° S.I. substrate	

- ❑ $Ge_{0.94}Sn_{0.06}$ overlapping with $In_{0.12}Al_{0.88}As$
  ↓
  lattice matched
  ($a_{Ge_{0.94}Sn_{0.06}}$ = 5.70786 Å at 300 K)
- ❑ Q_z and Q_x symmetricity at $Ge_{0.94}Sn_{0.06}$ shows no or minimal defects
- ❑ $In_xAl_{1-x}As$ linearly graded buffer constraints mismatch induced defects

M. K. Hudait *et al.*, *JMC-C*, 2022, **10**, 10530–10540.

Minority Carrier Lifetime of GeSn (0-6% Sn)

Microwave Reflection Photoconductive decay (μ−PCD) technique @ NREL

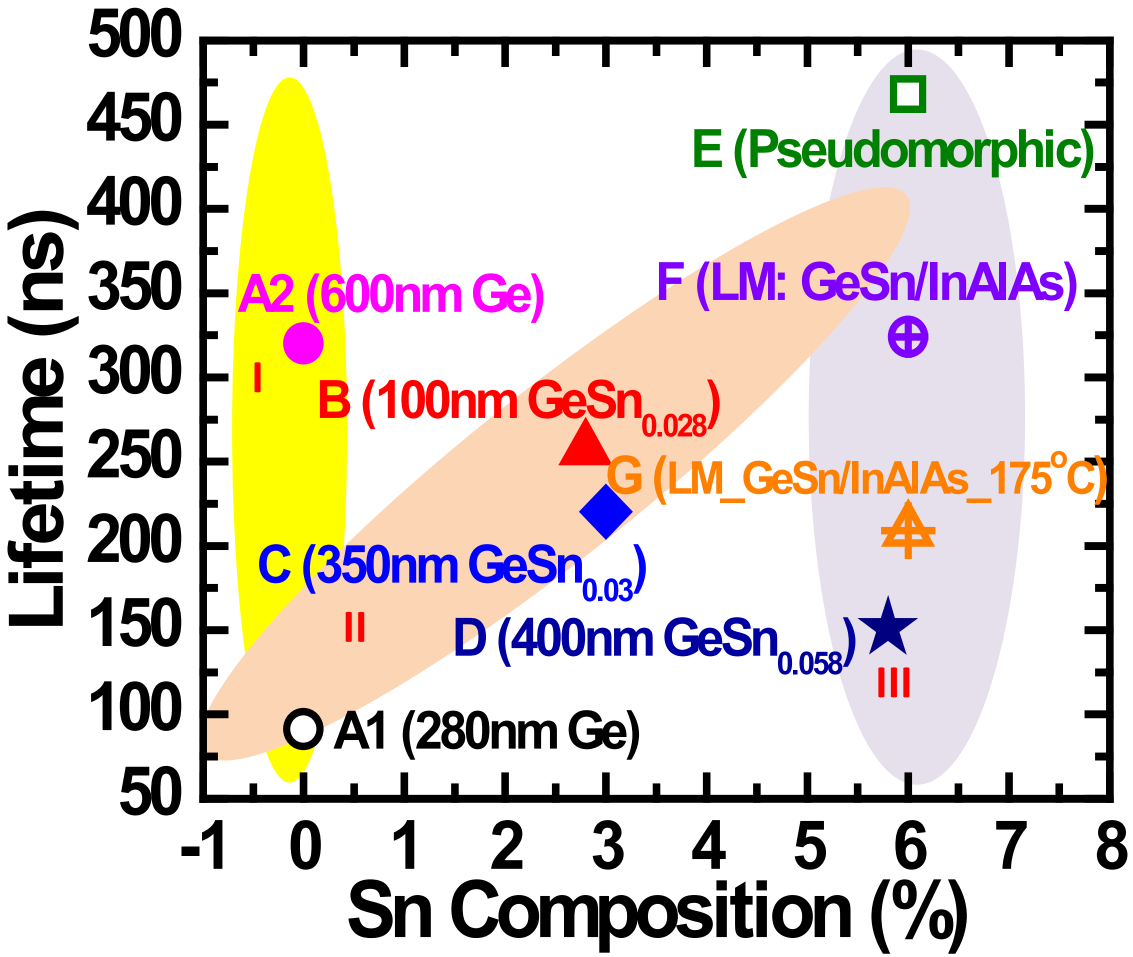


- ❑λ =1500 nm (20 mW, ~10^{13} cm^{-3} injection density), E_{ph} ≈ 0.83 eV carriers in *L*- and *Γ*-valleys
- ❑Low surface states induced recombination → high lifetime
- ❑SRH recombination (defect assisted) reduces carrier lifetime
- ❑High minority carrier lifetimes of 220 ns to 468 ns.

Low defects !!! ☑

High carrier lifetime !!! ☑

Minority Carrier Lifetimes of Ge and GeSn



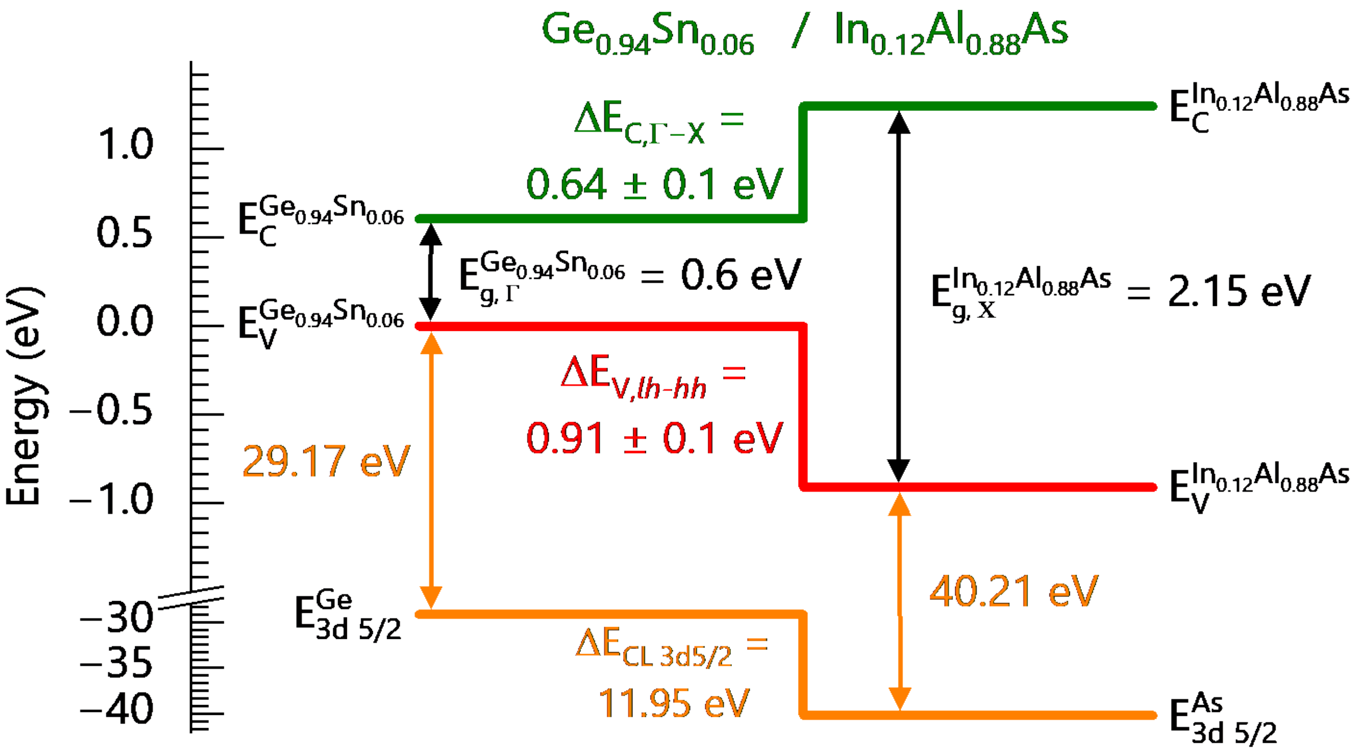
✓ High carrier lifetime of GeSn

✓ Leverage by superior growth

M. K. Hudait *et al.*, *JMC-C*, 2022, **10**, 10530–10540.

Energy band alignment of GeSn → Type-I

E. A. Kraut *et al.*, *Phys. Rev. Lett.*, 1980, **44**, 1620–1623.



Sample D - $Ge_{0.94}Sn_{0.06}/In_{0.12}Al_{0.88}As$

Karthikeyan *et al.*, *JMC-C (Submitted, 2023)*

Kraut *et al.* method:

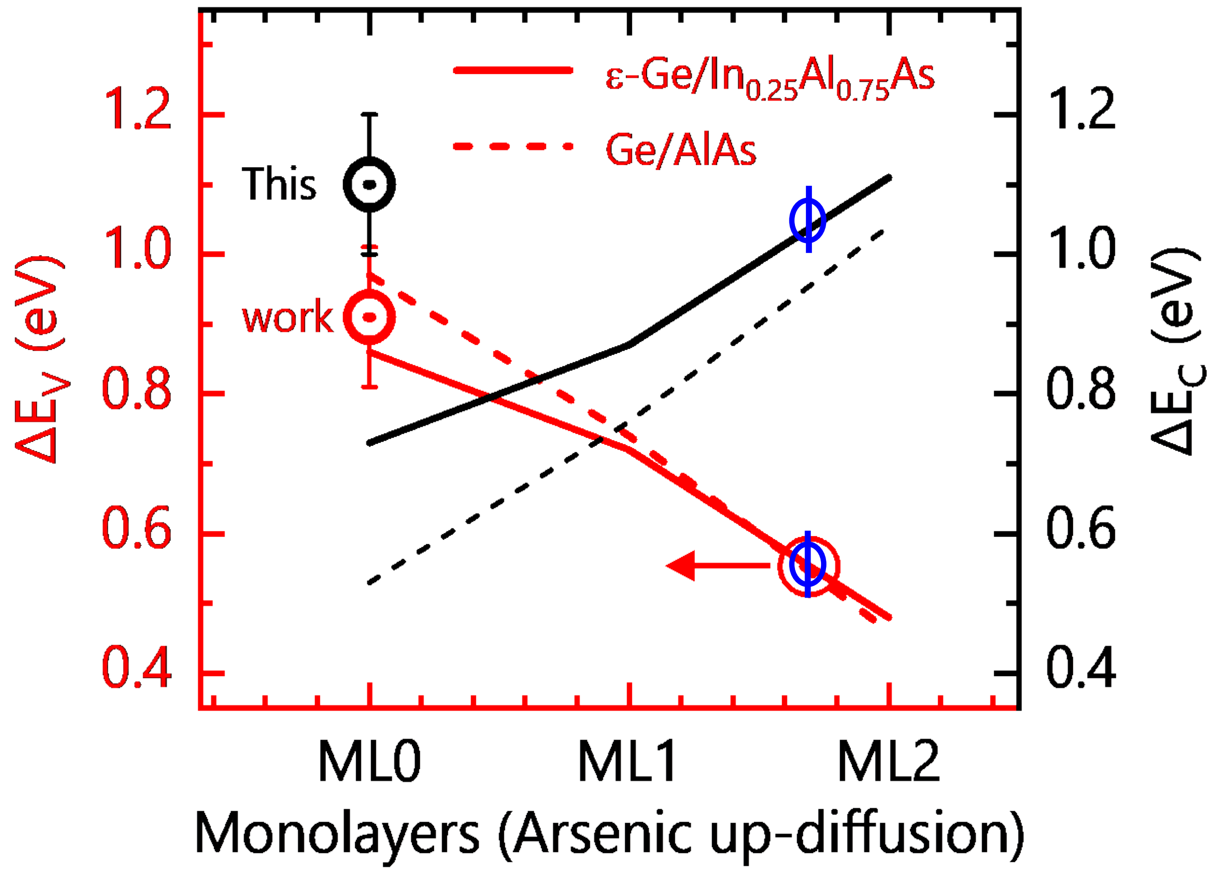
$$\Delta E_V = \left(E_{Ge\ 3d\ 5/2} - E_{VBM}\right)^{Ge_{0.94}Sn_{0.06}} - \left(E_{As\ 3d\ 5/2} - E_{VBM}\right)^{In_{0.12}Al_{0.88}As} - \left(E_{As\ 3d\ 5/2} - E_{Ge\ 3d\ 5/2}\right)^{interface}$$

$$\Delta E_{C,\Gamma-X} = E_{g,X}^{InAlAs} - E_{g,\Gamma}^{GeSn} - \Delta E_V$$

- ❑Type –I!! ☑
- ❑Large Band offsets!! ☑
- ❑Superior confinement!! ☑

VirginiaTech Invent the Future

Band offset – Atomic Interdiffusion



1.75% ε-Ge on $In_{0.26}Al_{0.74}As$

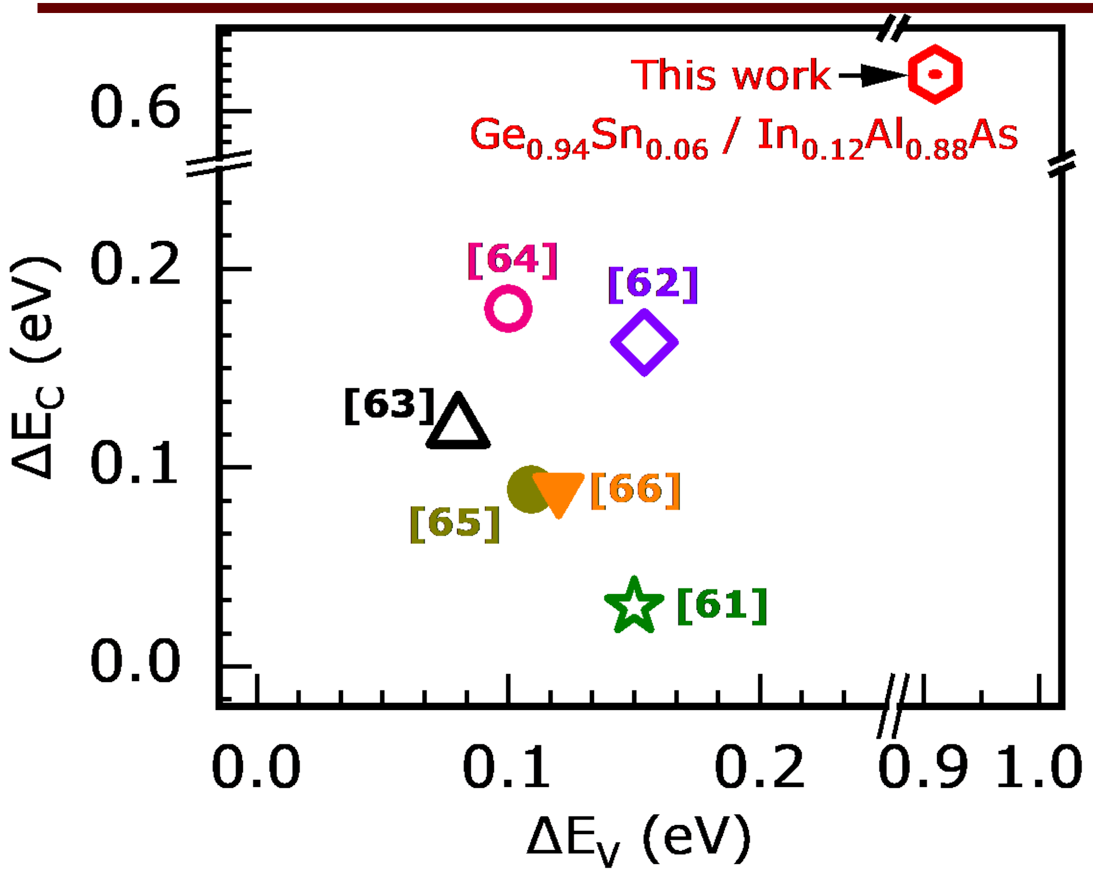
First principles calculation-based analysis:

- Abrupt interface ☑
- No interdiffusion ☑
- ΔE_V and ΔE_C large enough to hold carriers within $GeSn_{0.06}$ layer ☑
- GeSn (225˚C) lower growth temperature than Ge (400˚C) reduces interdiffusion ☑

Karthikeyan *et al.*, *JMC-C (Submitted, 2023)*

G. Greene-Diniz and M. Grüning, *Phys. Rev. Appl.*, 2018, **10**, 044052-1-16
M. B. Clavel *et al*, *ACS Omega* , 2022, **7**, 5946

Band offset – Benchmarking



Large band offset of lattice matched $Ge_{0.94}Sn_{0.06}/In_{0.12}Al_{0.88}As$ Heterostructure:

- ❑ $\Delta E_V = 0.91$ eV
- ❑ $\Delta E_{C,\,G\text{–}X} = 0.64$ eV

- ❑ Band offsets of GeSn grown on Ge or SiGeSn < 0.2 eV

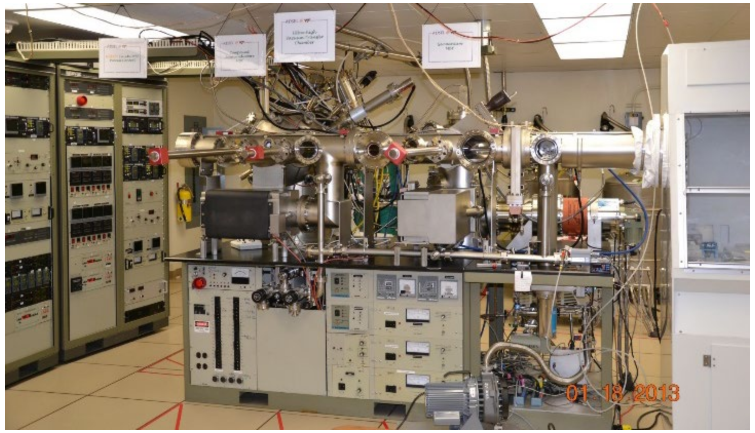
Ref.	Structure
[61]	$Ge_{0.92}Sn_{0.08}$ / Ge
[62]	$Ge_{0.85}Sn_{0.15}$ / Ge
[63]	$Ge_{0.92}Sn_{0.08}$ / Ge
[64]	$Ge_{0.84}Sn_{0.16}$ / $Si_{0.10}Ge_{0.75}Sn_{0.15}$
[65]	$Ge_{0.92}Sn_{0.08}$ / Ge
[66]	$Ge_{0.92}Sn_{0.08}$ / Ge

S. Karthikeyan *et al.*, *JMC-C (Submitted, 2023)*

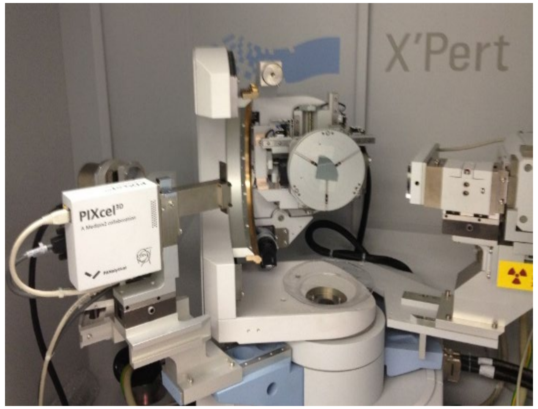
Facilities and Outreach

Capabilities

Materials Growth



High-resolution X-ray System

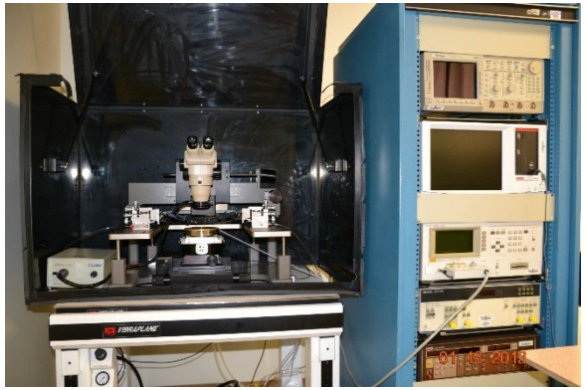


AFM System

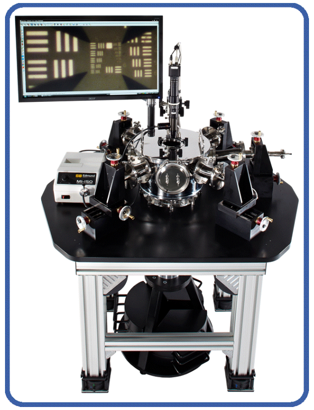
TEM System

Mobility Measurement System

Electrical Transport Measurement System

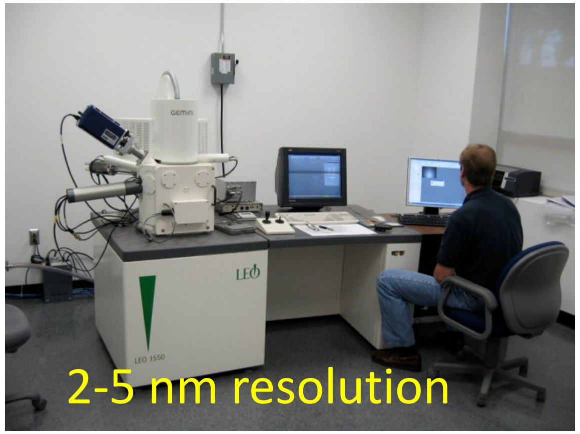


Cryogenic Probe Station

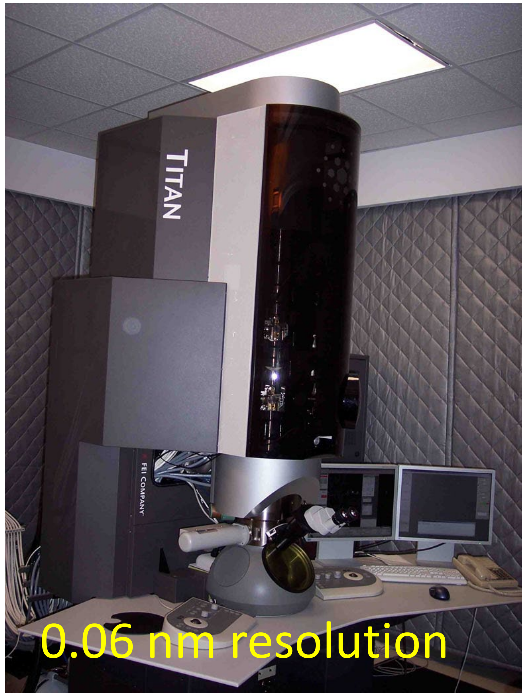


VT Nano Fabrication Shared Facilities

VT-ICTAS Measurement and Analysis Equipment



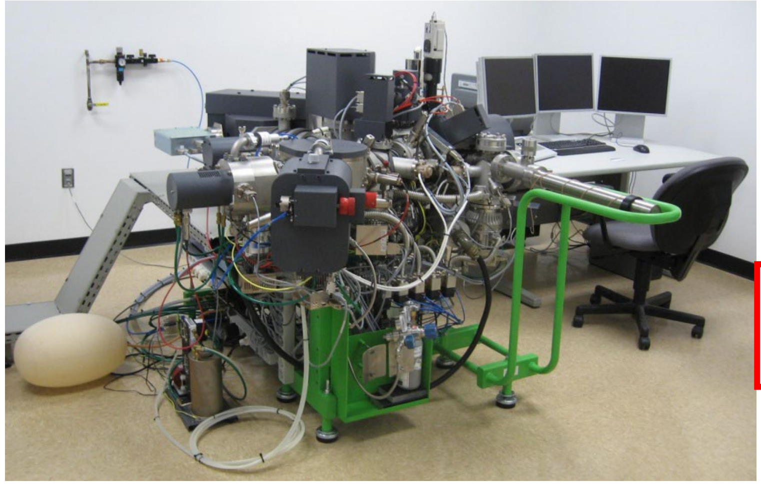
Field Emission Scanning Electron Microscope (SEM)



Scanning Transmission Electron Microscope

Auger Electron Spectroscopy

Dual-Beam Focused Ion Beam



Secondary Ion Mass Spectrometer

Outreach: VT C-Tech^2 Summer Camp *K*-12 Juniors and Seniors @ ADSEL

Removed Students' photos

Graduate student, Michael Clavel is explaining Ga-Al mixing effect

PI is explaining MBE system

PI's graduate student Michael is demonstrating how two metals, Ga and Al react each other

PI with C-Tech^2 summer camp *K*-12 juniors and seniors (women in engineering)

VT-C-Tech^2 summer camp *K*-12 juniors and seniors in PI's lab

Challenges & Summary: FETs and Laser

- Defect and interface control for large mismatch materials
- How to realize alternate channel Ge/InGaAs FINFETs and NSFET
- Tunable wavelength strained Ge and GeSn based QW Laser and photodetectors
- Bridging the lattice constant for lattice matching device structure with low defect on Si ??
- Heterogeneous Integration of III-V and Ge based Photonics and Electronics on Si