Electrical Safe Operating Area and Latent Damage of SiC Low-Voltage nMOS Under TLP and VF-TLP Stresses

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***Abstract*— In this article, transmission line pulse (TLP) and very fast TLP (VF-TP) systems were utilized to characterize the electrical safe operating areas (SOAs) and latent damage of silicon carbide (SiC) low-voltage nMOS devices to investigate their electrostatic discharge (ESD)-related reliability performance. The gate oxide breakdown voltages of SiC nMOS with varying gate oxide thickness were measured by dc, TLP, and VF-TLP. The TLP and VF-TLP waveforms at breakdown points were also presented and discussed. ESD capability of SiC nMOS devices with gate lengths varying from 1 to 6 μm was also characterized by TLP and VF-TLP. Their ESD behaviors and failure mechanisms were discussed. Scanning electron microscopy (SEM) and technology computer-aided design (TCAD) simulations were also carried out to understand the failure mechanism. At last, the ESD-induced latent damage on SiC nMOS was characterized. A decrease in threshold voltage and an increase in drain leakage current were observed with the increase in stress cycles. The latent damage is mainly due to the gate oxide injected carriers during the avalanche operation and can be recovered after 200 °C anneal.**

***Index Terms*— CMOS devices, electrostatic discharge (ESD), latent damage, low-voltage silicon carbide (SiC), safe operating area (SOA).**

I. Introduction

SILICON carbide (SiC) is a promising semiconductor material for high-voltage (HV) and high-temperature applications due to its wide bandgap, low intrinsic carrier concentration, and high thermal conductivity [1]. In order to further improve the high-temperature performance of electronic systems, a variety of integrated circuits (ICs) have been designed and manufactured in SiC-based bipolar and CMOS technologies [2], [3], [4], [5], [6]. Although these ICs are capable of operating up to 600 °C, their reliability is not sufficiently explored yet. Among reliability issues, electrostatic discharge (ESD) has been identified as one of the most significant concerns for modern ICs and electronic systems. As a result, a few SiC-based ESD protection devices have been proposed and investigated to improve the reliability of SiC ICs [7], [8], [9], [10], [11]. For example, Lai et al. [7] reported an HV silicon-controlled rectifier (HV-SCR) structure that was fabricated by a 4H-SiC bipolar-CMOS-DMOS (BCD) process. The HV-SCR shows a relatively higher failure current compared to SiC nMOS and LDMOS. Furthermore, Do et al. [8], [9], [10], [11] also proposed SiC-based gate-body-floating nMOS (GBFNMOS), high-holding floating gate nMOS (HHFGNMOS), low-voltage SCR, and lateral insulated-gate bipolar transistor-based SCR (LIGBT-SCR) for ESD protection. High failure current and reliable thermal performance were observed in these devices.

Besides the development of SiC-based ESD protection devices, the ESD-related reliability of the devices under protection (e.g., CMOS devices) needs to be studied. For conventional silicon (Si) based CMOS devices, their electrical safe operating area (SOA, e.g., gate oxide breakdown and drain–source failure current) and latent damage induced by ESD stresses are usually investigated to evaluate their reliability [12], [13], [14], [15], [16], [17], [18]. Weir et al. [12], Malobabic et al. [13], and Wu and Rosenbaum [14] investigated Si-based gate oxide reliability under ESD conditions. Transmission line pulse (TLP) and very fast TLP (VF-TP) were utilized to characterize the oxide breakdown voltage, and various models were proposed to analyze the failure mechanism. Amerasekera et al. [15] characterized and analyzed the parasitic n-p-n of Si-based nMOS in the 0.2 μm CMOS process. A methodology was proposed to improve the drain–source failure current (I_{t2}) of short-channel and thin-oxide nMOS devices. Cester et al. [16], Huh et al. [17], and Groeseneken [18] studied the latent damage of Si nMOS devices under ESD stresses. The transconductance, saturation current, and drain–source leakage current showed significant degradation after nondestructive ESD stresses. On the other hand, very few researches have been carried out on the ESD-related reliability of SiC-based devices. Phulpin et al. [19] investigate the ESD robustness of SiC-based MESFETs. A Zener diode and a Schottky diode were embedded in the SiC MESFETs to increase the drain–source I_{t2}. In previous

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work [20], we reported ESD characteristics of 15 V SiC nMOS in the Raytheon high-temperature SiC (HiTSiC) process to explore ESD robustness. The SOAs of low-voltage SiC nMOS devices with varying channel widths, gate lengths, and gate bias conditions were characterized by a TLP system. However, the gate oxide breakdown voltage, failure mechanisms, and latent damage of the SiC low-voltage nMOS have not been sufficiently analyzed.

In this article, a systematic study of ESD reliability was conducted on SiC-based low-voltage nMOS devices. TLP and VF-TLP were utilized to stress the devices. The research is divided into six sections. In Section II, the gate oxide breakdown of SiC nMOS with varying oxide thickness under dc, TLP, and VF-TLP stresses are reported. In Section III, the drain–source I_{t2} of SiC nMOS devices with varying gate lengths and gate bias conditions are presented. Scanning electron microscopy (SEM) and technology computer-aided design (TCAD) simulations were carried out to analyze the failure mechanism. The latent damage of SiC low-voltage nMOS devices is investigated in Section IV. Repetitive TLP and VF-TLP pulses were applied to the drain terminals of the nMOS devices. Drain–source current was characterized after the stresses to analyze the latent damage. Finally, the discussion and conclusion are provided in Sections V and VI.

II. Gate Oxide Breakdown Under ESD Stresses

Gate dielectric breakdown is one of the most important reliability concerns for MOS devices. Scores of researchers argued that the oxide reliability for SiC-based MOS devices was worse than that for Si counterparts due to the low conduction-band offset of the SiC-SiO_2 interface [21], [22]. However, some researchers claimed that the gate oxide breakdown voltage could be further improved [23]. Therefore, in order to demonstrate the SOAs of SiC CMOS devices under ESD conditions, gate oxide breakdown voltage needs to be investigated.

A. Experimental Setup

Gate oxide breakdown of SiC-based lateral nMOS devices was characterized by dc, TLP, and VF-TLP systems. For dc characterization, a Keithley 2450 source measure unit (SMU) was utilized as the voltage source and current meter. For TLP and VF-TLP measurements, an ES620 system by ESDEMC was implemented. The rise times of the TLP and VF-TLP pulses are 10 ns and 100 ps, and the pulse widths of the TLP and VF-TLP are 100 and 10 ns, respectively. The waveforms were captured by a Keysight MSO-6004A oscilloscope. The gate leakage current was measured at 2 V bias after each TLP and VF-TLP pulse to monitor the device failure point. The failure points (i.e., the breakdown points of the gate oxide in this section) of the devices are defined at which the dc gate leakage current increases by over 100%.

SiC nMOS devices with varying gate oxide thickness of 35, 50, and 80 nm were characterized. The nMOS devices with 35 nm gate oxide thickness were fabricated by Raytheon HiTSiC CMOS process, and their recommended supply voltage is 15 V [24]. The nMOS devices with gate oxide

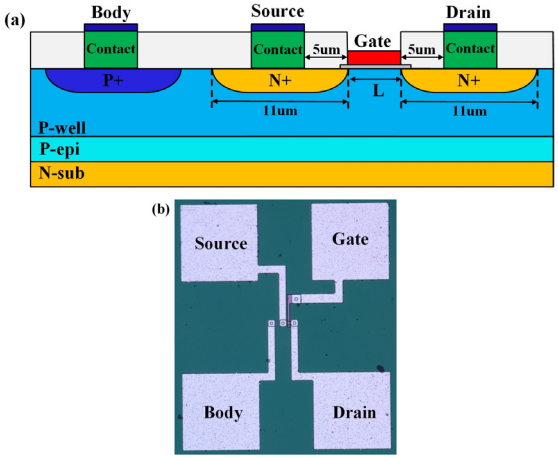

Fig. 1. (a) Cross-sectional view and (b) layout view of the measured SiC nMOS.

thicknesses of 50 and 80 nm were fabricated by the 4H-SiC BCD process of Fraunhofer Institut für Integrierte Systeme und Bauelementetechnologie (IISB) in Germany [25]. The recommended supply voltages for the nMOS with 50 and 80 nm gate oxide are 20 and 30 V, respectively. Fig. 1(a) and (b) shows the cross-sectional view and layout view of the nMOS. N-type polysilicon was deposited on the gate oxide as the gate terminal. Nickel/aluminum alloy is used as the contact silicide for N+ regions. The three processes provide nMOS devices with a minimum gate length (L) of 1 μm, and the channel width and L of the nMOS devices measured in this section are 3 and 1 μm. The stresses were applied to the gate terminals of the devices, and drain, source, and body terminals were grounded during the measurements.

B. Experimental Results

Fig. 2(a)–(c) shows the I–V curves of SiC nMOS gate oxide under dc, TLP, and VF-TLP stresses. The data with solid symbols correspond to the I_{DUT} and V_{DUT}, and the data with open symbols corresponds to the gate leakage current after each TLP (or VF-TLP) pulse. The oxide breakdown voltage decreases with the increase of the pulsewidth due to the cumulative damage of longer pulses. The breakdown voltages of 50 nm gate oxide under TLP and VF-TLP stresses are 75.5 and 95.4 V, respectively. Meanwhile, the breakdown voltage of the gate oxide increases with the oxide thickness. For example, the breakdown voltage under TLP stresses from 55 to 109.7 V with the oxide thickness varying from 35 to 80 nm. Anode-hole injection model is usually utilized to illustrate and analyze the oxide breakdown [12], [26]. During the pulse stresses, electrons and holes tunnel through the oxide region, and a portion of the tunneling holes generate defects in the oxide. When a critical number of defects is generated, the oxide is bridged by overlapping defects, which triggers the breakdown. This can be expressed as [12] and [26]

$$T_{\mathrm{BD}} = \left(\frac{N_{\mathrm{BD}}}{k}\right)^{1/n} \frac{1}{J_h} \tag{1}$$

where T_{BD} is the time to break down, N_{BD} is critical defect density, n is trap generation rate, J_h is hole current density, and

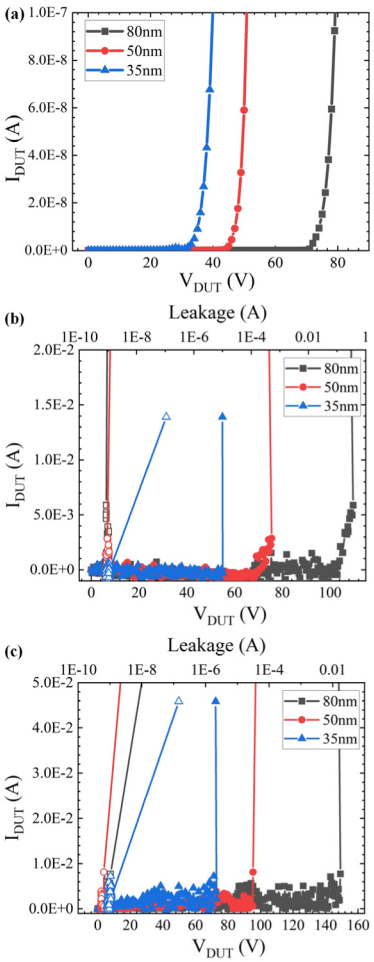

Fig. 2. SiC nMOS gate oxide *I–V* curves under (a) dc, (b) TLP, and (c) VF-TLP stresses.

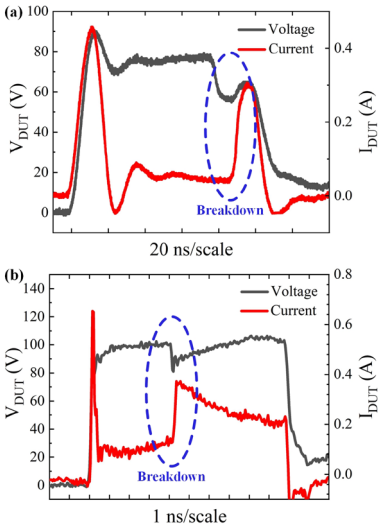

Fig. 3. Voltage and current waveforms of 50 nm gate oxide breakdown under (a) TLP and (b) VF-TLP stresses.

k is lattice-hole generation coefficient which increases with the increase of oxide electric field. The increase of the oxide thickness decreases the oxide electric field. Therefore, nMOS devices with thicker oxide show higher breakdown voltages.

Fig. 3 shows the voltage and current waveforms of 50 nm SiC nMOS gate oxide breakdown under TLP and VF-TLP stresses. As shown in Fig. 3(a), the oxide failure takes place at ~69 ns after the initial occurrence of the TLP pulse. The voltage drops from ~78 to ~55 V, and the current increases from ~0.05 to ~0.3 A. After the hard failure, the leakage current increases from ~900 to ~10 μA [Fig. 2(b)]. Similar behaviors were observed under VF-TLP conditions [Fig. 3(b)].

III. ESD Capability of SiC nMOS With Parasitic n-p-n

The ESD performance of nMOS devices is strongly related to their parasitic lateral n-p-n bipolar junction transistors (BJTs), especially when implemented as output buffers. ESD generates a high voltage that reaches the avalanche breakdown voltage of the drain-substrate junction of nMOS devices. The avalanche-generated current then forward-biases the base–emitter junction of the parasitic n-p-n (i.e., substrate-source junction of the nMOS) in the nMOS device, and the parasitic n-p-n is turned on. The nMOS may show a voltage drop due to the turn-on of the parasitic n-p-n, which is the so-called snapback. It has been demonstrated that the current gain of the parasitic n-p-n affects the operation of the nMOS under ESD conditions, such as the snapback holding voltage (V_h) as well as the trigger voltage (V_{t1}) and I_{t2} [27]. Therefore, SiC nMOS devices with associated lateral n-p-n were characterized by TLP and VF-TLP in this section to investigate their ESD-related SOAs.

A. Experimental Setup

SiC lateral nMOS devices that were fabricated by the 4H-SiC BCD process of Fraunhofer IISB were characterized by TLP and VF-TLP systems. The gate oxide thickness of the devices is 50 nm, and the L of the devices varies from 1 to 6 μm. All the devices are one-finger with a channel width of 100 μm. The TLP and VF-TLP pulses were applied to the drain terminals of the devices with the gate, source, and body grounded. The rise time and pulsewidth of the TLP and VF-TLP are the same as the setup in Section II. The leakage current was measured with a 10 V bias to monitor the failure of the devices. After the device failure, drain–source leakage current with gate and body floating and drain-gate leakage current with source and body floating were measured to investigate the failure mode. SEM was utilized to observe the failure points. The 2-D TCAD simulations were carried out by Synopsys Sentaurus to understand the failure mechanisms. SiC nMOS devices with varying gate bias voltages (V_G) were also characterized by TLP and VF-TLP.

B. SiC nMOS With Gate Grounded

Fig. 4 shows the TLP and VF-TLP characterizations of SiC nMOS with L varying from 1 to 6 μm. The devices did not show snapback behaviors as Si-based nMOS devices. The snapback of the nMOS is strongly related to the current gain (β) of the parasitic lateral n-p-n bipolar transistor. The requirement of the snapback is defined as [27]

$$\beta(M-1) > 1 \tag{2}$$

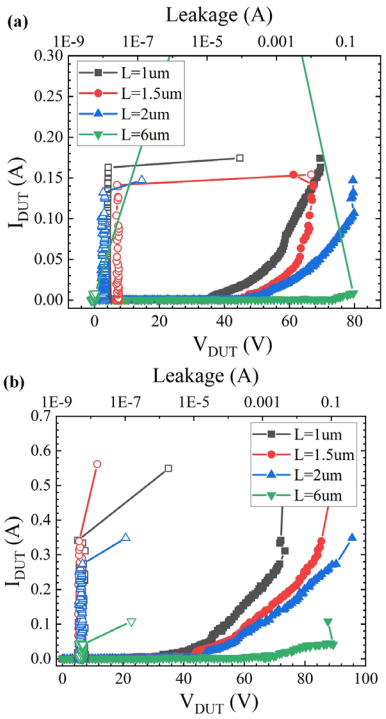

Fig. 4. (a) TLP and (b) VF-TLP characterization results of SiC nMOS with varying L.

where M is the multiplication factor of the avalanche. The current gain of an n-p-n is determined by intrinsic doping concentrations, minority diffusion constants, and widths of base and emitter regions [28]. Compared to commonly used Si-based nMOS, since SiC nMOS devices have a stronger bandgap narrowing effect [29], lower minority carrier mobility [30], and wider base regions (i.e., L), the current gain of the parasitic n-p-n is too low to show snapback behaviors. In addition, the I_{t2} of the nMOS with 1 μm L under TLP stress is ~162 mA, and it decreases to ~132 mA when the L increases to 2 μm. This is because the increase of L increases the ON-resistance and failure voltage (V_{t2}). The device failure is mainly caused by the thermal limit of the reversed p-n junction (i.e., drain to substrate junction). The increase of V_{t2} increases the junction power, which generates more heat in the junction region and decreases the I_{t2} [31]. Additionally, for VF-TLP measurements, the I_{t2} of the nMOS with 1 μm L is ~341 mA, and it decreases to ~243 mA when the L increases to 2 μm. Due to the decrease of the pulsewidth, less heat was generated in the device junction, which increases the I_{t2}.

It should be noted that the I_{t2} of the nMOS with L of 6 μm under both TLP and VF-TLP stresses is much lower than that of short-channel nMOS devices (i.e., $L < 2$ μm). In order to figure out the failure mode, the drain–source leakage current and drain–gate leakage current were measured after the device failure. Table I lists the leakage current of the failure devices at 10 V bias. The drain–gate leakage current of the nMOS with 6 μm L is higher than 10 nA. This indicates that the failure of the devices is due to gate oxide breakdown instead of junction thermal runaway. This may be an important difference between SiC and Si nMOS devices as the gate oxide breakdown under this condition occurs when the gate oxide is thinner than 3 nm for Si-based nMOS [15]. Since SiC nMOS devices do not show snapback behaviors, the failure threshold of long-channel devices is determined by the gate oxide breakdown.

TABLE I
SiC nMOS Leakage Current After TLP and VF-TLP Failure

Gate length	TLP		VF-TLP	
	Drain to source	Drain to gate	Drain to source	Drain to gate
1 µm	1.82E-6	1.5E-10	5.44E-3	1.66E-10
1.5 µm	4.01E-4	1.86E-10	7.91E-5	1.48E-10
2 µm	1E-4	1.6E-10	2.64E-5	1.5E-10
6 µm	1.1E-10	7.97E-8	1.72E-10	9.28E-4

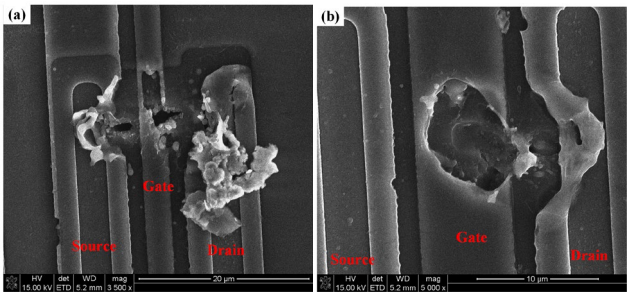

Fig. 5. SEM photographs of SiC nMOS with (a) 1 μm L and (b) 6 μm L after TLP failure.

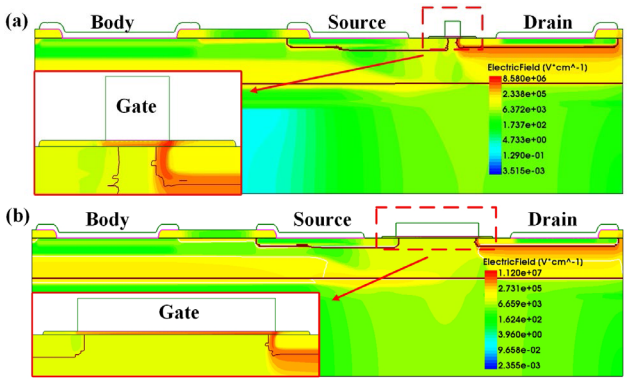

Fig. 6. Simulated electric field distribution of SiC nMOS with (a) 1 μm L and (b) 6 μm L at failure voltages.

SEM was utilized to observe the damages of the TLP on the SiC nMOS devices. The SEM photographs of SiC nMOS devices with 1 and 6 μm L are shown in Fig. 5. The thermal filament of 1 μm SiC nMOS spreads from the drain contact to the source contact while the filament defect is only observed on drain and gate terminals for 6 μm L SiC nMOS. This also verifies that the early failure of the long-channel nMOS (i.e., $L = 6$ μm) is due to the gate oxide breakdown.

TCAD simulations were carried out by Sentaurus to understand the failure mode of the nMOS devices. In order to increase the simulation precision Monte-Carlo-based ion implantation was performed to form the p-well, N+, and P+ regions. The ion implantation profiles were extracted from the real process. Transient-based ESD simulations were performed by Sentaurus Device to extract the electric field distribution of the SiC nMOS. Fig. 6 shows the simulated electric field

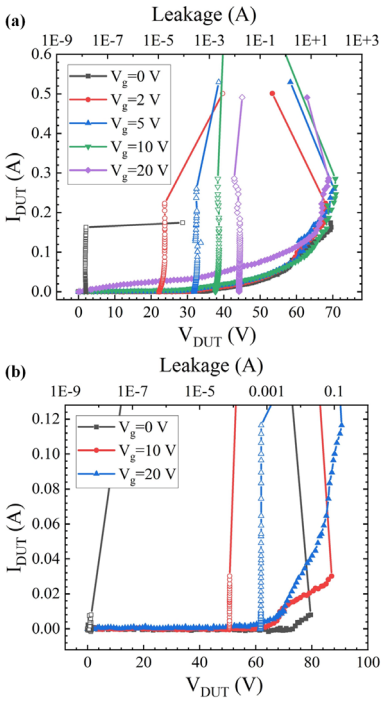

Fig. 7. TLP characterization results of SiC nMOS of (a) 1 μm L and (b) 6 μm L with varying V_G.

distribution of the SiC nMOS at the failure voltages (i.e., drain voltage of 70 and 80 V for L of 1 and 6 μm respectively). The electric field in the gate oxide of 1 μm L nMOS is ~8.5 MV/cm while it is ~11.2 MV/cm for the 6 μm L nMOS.

C. SiC nMOS With Gate Bias (V_G)

For gate-controlled devices (e.g., nMOS, LDMOS, and gate-controlled SCR), the ESD behaviors are related to the gate bias voltage. V_G provides seed current to the substrate, which helps trigger the parasitic n-p-n and reduces V_{t1} [27]. Besides, it turns on the inversion channel of nMOS, which helps discharge the ESD current and increases I_{t2} [32]. Therefore, the 1 and 6 μm L nMOS devices with gate bias were characterized by the TLP system. The TLP measurement results are shown in Fig. 7. For the nMOS with 1 μm L, I_{t2} increases from ~162 to ~285 mA when V_G increases to 10 V, and it shows little change when V_G increases to 20 V. This is similar to conventional Si-based nMOS [32]. For the nMOS with 6 μm L, I_{t2} increases from ~8 to ~116 mA when V_G increases to 20 V. The increase of V_G reduces the drain–gate voltage drop, which increases V_{t2} and I_{t2}.

IV. ESD-Induced Latent Damage on SiC nMOS

Besides the hard failure caused by ESD stresses, latent damage induced by nondestructive ESD stresses also needs to be studied since CMOS devices showed degradation after nondestructive ESD stresses [16], [17], [18]. Therefore, in this section, TLP and VF-TLP stresses were applied to SiC nMOS devices to investigate ESD-induced latent damage.

A. Experimental Setup

SiC lateral nMOS devices that were fabricated by the 4H-SiC BCD process of Fraunhofer IISB were characterized by TLP and VF-TLP systems. For each experiment, three identical devices were characterized. Since the results are very similar, only one of the devices is presented in this article. The gate oxide thickness, gate length, and width of the SiC nMOS devices are 50 nm, 1 μm, and 100 μm, respectively. The rise times and pulse widths of the TLP and VF-TLP were kept the same as the setup in Sections II and III, and the drain leakage current was monitored at 10 V. Repetitive TLP and VF-TLP pulses were stressed to the drain terminals of the devices with the device source and body grounded. The pulses were kept at voltage levels which generate 60% of the device I_{t2}. After the stress cycles of 10, 50, 100, 200, 500, and 1000 pulses, the devices were cooled down for 5 min to eliminate heat accumulation. Then TLP (or VF-TLP) I–V curves, drain current versus gate voltage (i.e., I_D–V_G) curves, and leakage current were measured. The I_D–V_G curves were characterized by a Keysight B1505 curve tracer, and the drain leakage current was extracted at 10 V by a Keithley 2450 SMU. Finally, the devices were annealed for 10 h at 200 °C in a high-temperature oven (i.e., Fisher Scientific 650–126). Then the TLP (or VF-TLP) I–V curves, I_D–V_G curves, and leakage current of the devices were measured after 10 h cooled down to observe whether the latent damage could be recovered. In addition, in order to compare the latent damage between the SiC and Si, a Si-based 5 V nMOS device that was fabricated on a 0.18 μm BCD process was also characterized. The gate oxide thickness, gate length, and width of the device are 14 nm, 1 μm, and 100 μm. For the convenience of the measurement, a silicide block layer was applied to the drain of the Si nMOS to increase I_{t2}. The experimental conditions for the Si nMOS were the same as the SiC nMOS except that the drain leakage current was monitored and measured at 5 V. Moreover, the drain-gate leakage current of the SiC and Si nMOS devices was also measured with varying drain voltage (V_D). The measurements were carried out by a Keysight B1505 curve tracer, and the voltage was applied to the drain terminals with gate, body, and source terminals grounded.

B. Repetitive TLP Stresses on SiC ggNMOS

The variation of the SiC gate-ground nMOS (ggNMOS) after TLP stresses is shown in Fig. 8. The trigger voltage, V_{t1}, of the device increases from 34.1 to 38.6 V after ten cycles of stresses. Then V_{t1} shows little change after 1000-cycle stresses. V_{t1} was recovered to 35.6 V after the anneal. Additionally, little degradation was observed on the ON-resistance of the device. The I_D–V_G curves are shown in Fig. 8(b) to compare the threshold voltage (V_{th}) at which the drain current reaches 0.1 μA/μm (i.e., 10 μA for nMOS with 100 μm width). The threshold voltage shows an evident shift (i.e., from 2.4 to 2 V) after ten-cycle stresses and a slight decrease from ten cycles to 1000 cycles. After 200 °C anneal, V_{th} recovers to 2.3 V. The drain leakage current, I_{lk}, shifts of the measured devices are shown in Fig. 8(c). The drain leakage current keeps increasing with the stressing cycles. After 1000 cycles of stresses, the leakage current increases by over 500% for Sample 1 and Sample 2.

During the avalanche operation, hot electrons and holes, especially in the gate–drain overlap region, can gain sufficient

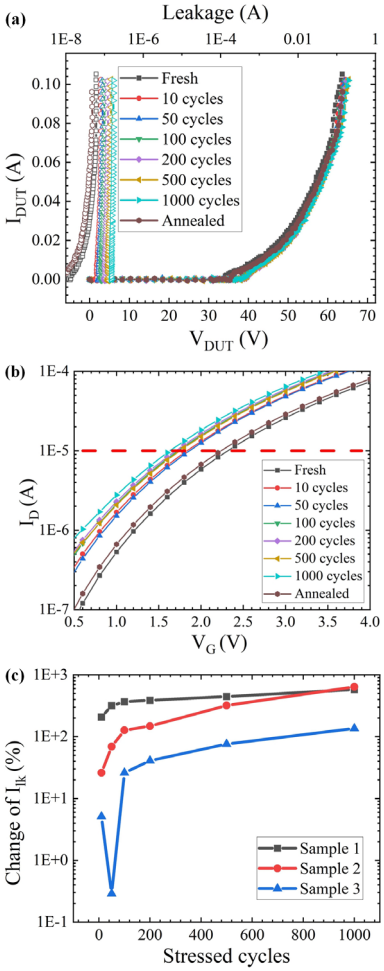

Fig. 8. Variation of SiC ggNMOS after TLP stresses (a) TLP curves, (b) I_D–V_G curves, and (c) drain leakage current.

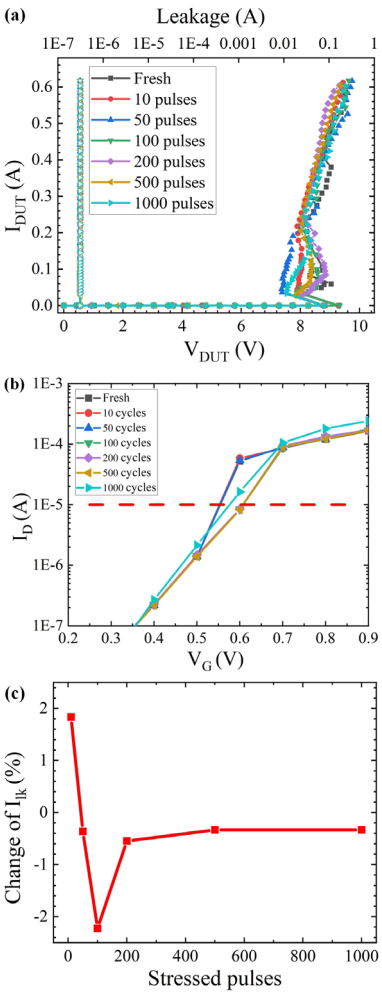

Fig. 9. Variation of Si ggNMOS after TLP stresses (a) TLP curves, (b) I_D–V_G curves, and (c) drain leakage current.

energy to surmount or tunnel through the gate oxide due to the strong vertical electric fields. This generates oxide traps, interface traps, and trapped charges, which reduces V_{th} and increases drain–source leakage current, I_{lk} [28]. After annealing, the trapped charges were recovered by thermal emission [28]. As a result, the V_{th} increases to 2.3 V. It should be noted that although the V_{t1} was also recovered by the annealing process, it may not be due to the trapped charges. This needs further investigation.

In order to compare the latent damage between SiC and Si devices, a Si-based nMOS was also characterized by the TLP system. Fig. 9 shows the variation of the Si ggNMOS after TLP stresses. The TLP I–V curves, I_D–V_G behaviors, and leakage current show little change after 1000 cycles of TLP stresses. This may be because the Si nMOS has lightly doped drain (LDD) implant regions and a low V_h (i.e., ~8 V), which leads to fewer carrier injection into the gate oxide region compared to the SiC nMOS.

The transient drain-gate leakage current is difficult to monitor under TLP stresses. Thus, drain–gate leakage currents with varying V_D of the SiC and Si nMOS devices were measured by a curve tracer (i.e., dc conditions). Since the devices are easy to be destroyed under dc conditions, the drain current was limited to 10 mA. Fig. 10 shows the drain-gate leakage

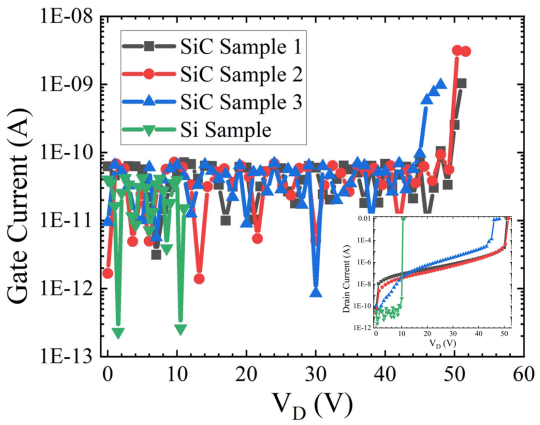

Fig. 10. Drain–gate leakage current with varying V_D.

current versus V_D, and the insert shows the total drain current versus V_D. It should be noted that the measured drain-gate leakage currents are negative while the absolute values were plotted. As shown in Fig. 10, the drain-gate leakage currents of SiC and Si devices are lower than 100 pA before the avalanche breakdown. When V_D reaches the avalanche breakdown voltage (i.e., ~50 V in the inserted figure), the drain-gate currents of the SiC nMOS devices show a significant increase,

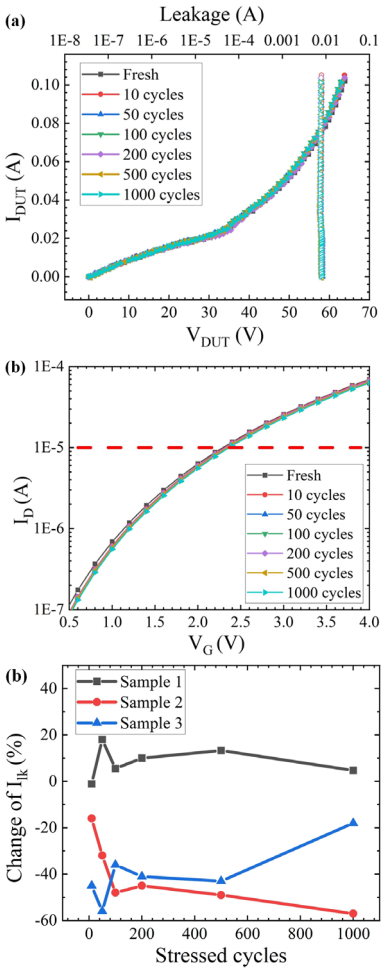

Fig. 11. Variation in 20 V gate-bias SiC nMOS (a) TLP curves, (b) I_D–V_G curves, and (c) drain leakage current after TLP stresses.

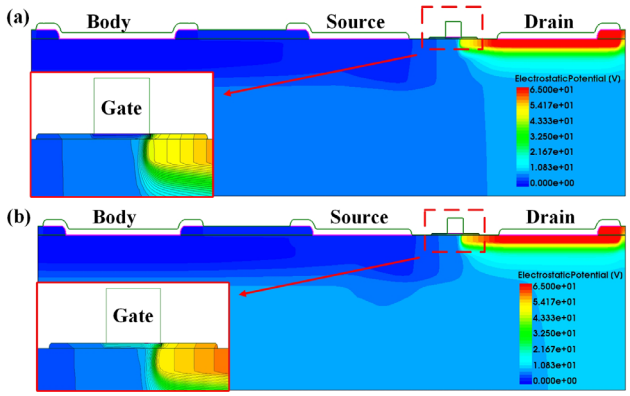

Fig. 12. Simulated electric potential distribution of 1 μm L SiC nMOS with (a) 0 V V_G and (b) 20 V V_G.

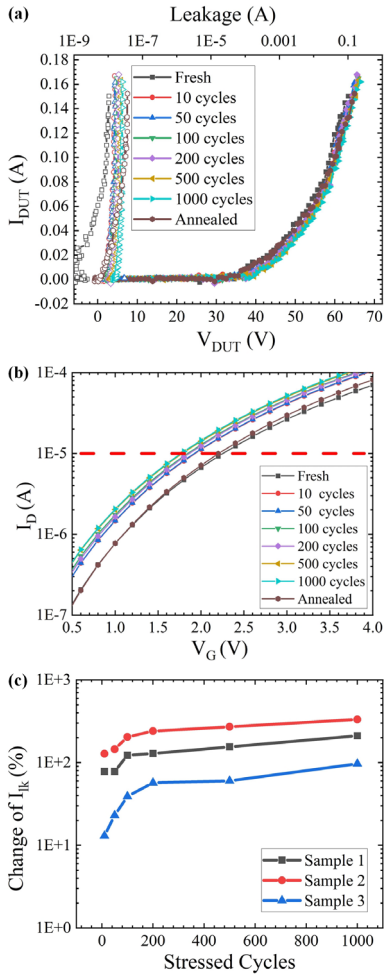

Fig. 13. Variation in SiC ggNMOS (a) VF-TLP curves, (b) I_D–V_G curves, and (c) drain leakage current after VF-TLP stresses with 0 V V_G.

which indicates strong carrier injection into the gate oxide. On the other hand, since the breakdown voltage (i.e., 10.5 V) and V_h [i.e., 8 V in Fig. 9(a)] of the Si nMOS are much lower than the SiC nMOS, the drain-gate leakage current shows little change after avalanche breakdown. Therefore, little latent damage was observed in the Si nMOS. Moreover, besides the lower breakdown voltage and V_h, the Si nMOS has LDD implant regions, which may also reduce the carrier injection [18].

C. Repetitive TLP Stresses on Gate-Bias SiC nMOS

Fig. 11 shows the variation in the TLP I–V curves, I_D–V_G, and leakage current of SiC nMOS with 20 V V_G after repetitive TLP stresses. The TLP I–V curves and V_{th} of the device show little change after 1000 cycles of stresses. The leakage current shifts less than 60%. TCAD simulations were carried out by Sentaurus. Fig. 12 shows transient ESD simulation results of the electric potential distribution in the SiC nMOS with 0 and 20 V V_G. The simulated V_D was 65 V. As shown in the figures, the electric potential in the channel region is ~10–20 V. Therefore, V_G decreases the drain–gate voltage drop and electric field in the gate oxide. This leads to less carrier injection.

D. Repetitive VF-TLP Stresses on SiC ggNMOS

The variation of the SiC ggNMOS after VF-TLP stresses is shown in Fig. 13. The results are similar to the gate-ground SiC nMOS after TLP stresses. The V_{t1} of the nMOS increases from 39 to 43 V after ten-cycle stresses and is recovered to 39.1 V by the annealing process. The shifts of the V_{th} and I_{lk} are mainly caused by the generation of the trapped charges

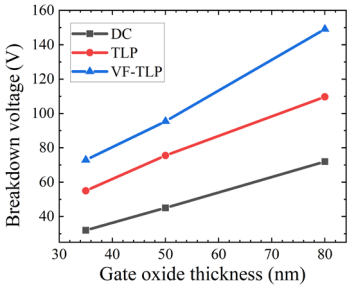

Fig. 14. Gate oxide breakdown voltage versus gate oxide thickness.

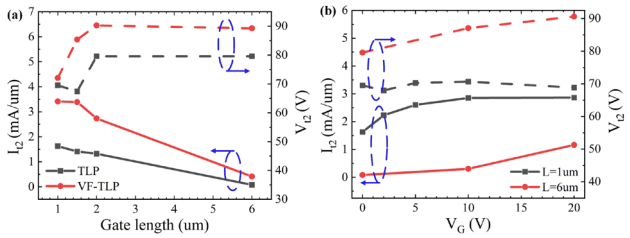

Fig. 15. SiC nMOS I_{t2} and V_{t2} versus (a) L and (b) V_G under TLP and VF-TLP stresses.

in the oxide traps and interface traps during the avalanche operation. The V_{th} decreases from 2.4 to 2 V after ten-cycle stresses and shows a slight decrease with the stressing cycles. The degradation was also recovered by annealing. Since the pulsewidth of the VF-TLP is shorter than that of the TLP, fewer carriers were injected into the gate oxide region. As a result, it shows less degradation of I_{lk} (i.e., from 100% to 300%) compared to the TLP measurements.

V. Discussion

A. Gate Oxide Breakdown

The gate dielectric breakdown voltage of nMOS devices is critical as it defines the up boundary of the SOA and ESD design window. Fig. 14 shows the gate breakdown voltage versus the gate oxide thickness of SiC nMOS devices. The results are average values extracted from three samples. The gate breakdown voltages under dc, 100 ns TLP and 10 ns VF-TLP conditions are ~0.9, ~1.48, and ~1.95 V/nm, respectively. It should be noted that the gate breakdown voltage under 100 ns TLP conditions of conventional Si-based nMOS devices is ~2.1 V/nm [12], [33], [34], which is 1.4 times of SiC nMOS. With the scale-down of SiC CMOS processes, the gate oxide reliability issues of thin-oxide SiC CMOS devices are expected to be more challenging than Si counterparts unless the quality of the gate oxide can be improved in the future.

B. Failure Current and Voltage

SOA of nMOS under ESD conditions is strongly related to I_{t2} and V_{t2} since the performance of the ESD protection devices is determined by the nMOS devices under protection. Fig. 15(a) shows the SiC nMOS I_{t2} per μm and V_{t2} versus L under TLP and VF-TLP stresses. These values can be utilized to design the output nMOS width for the robustness of ESD protection. Moreover, the I_{t2} of SiC nMOS is much lower than that of silicide-block nMOS based on Si (i.e., $I_{t2} > 5$ mA/μm) [27]. Therefore, it is worth studying the SOA of silicide-block nMOS devices on SiC in future work. On the other hand, the V_{t2} of SiC nMOS is much higher than Si nMOS. This may make the effective ESD protection of the SiC nMOS easier compared to Si as the requirement of the ESD protection devices is [27]

$$V_{t\max\_ESD} > V_{t2} + R_s I_{t2} \tag{3}$$

where $V_{t\max\_ESD}$ is the greater trigger voltage and failure voltage of the ESD protection device, R_s is the series resistor, and I_{t2} and V_{t2} are the failure current and voltage of the device under protection (i.e., the SiC nMOS in this case).

Fig. 15(b) shows the SiC nMOS I_{t2} per μm and V_{t2} versus V_G under TLP stresses. For nMOS with 1 μm L, I_{t2} increases from 1.6 to 2.9 mA/μm with V_G increasing from 0 to 10 V while V_{t2} shows little change. This indicates that SiC nMOS with gate coupling circuitry may be an option for the ESD protection of output nMOS devices in the future.

VI. Conclusion

The electrical SOA under ESD conditions of 4H-SiC low-voltage nMOS has been investigated. SiC nMOS device gate oxide breakdown voltages, failure current with parasitic n-p-n, and latent damage have been characterized by TLP and VF-TLP systems. TLP and VF-TLP waveforms at the oxide breakdown points are also presented and discussed.

In addition, the ESD capability of SiC nMOS devices with parasitic n-p-n BJTs has also been characterized by TLP and VF-TLP. The nMOS devices did not show snapback behaviors due to the low current gain of the parasitic n-p-n. The long-channel nMOS (i.e., $L > 2$ μm) showed early failure under both TLP and VF-TLP measurements. It has been demonstrated that the failure threshold of long-channel SiC nMOS devices is determined by the gate oxide breakdown since they do not show snapback behaviors. SEM and TCAD simulations were also utilized to illustrate this phenomenon.

At last, the ESD-induced latent damage on the SiC nMOS has been studied. Degradation was observed on SiC ggNMOS under repetitive TLP and VF-TLP stresses. This is because hot carriers were injected into the gate oxide during the avalanche operation, which generated trapped charges and affected the threshold voltage and leakage current. The latent damage was recovered by 200 °C anneal as trapped charges were reemitted in high-temperature conditions. Meanwhile, SiC nMOS devices with 20 V V_G showed little degradation under repetitive TLP stresses.

In general, a few ESD-related performances of SiC low-voltage nMOS devices may need attention, such as the nonsnapback behaviors, the failure threshold, and the latent damages, since they are different from the conventional Si-based nMOS.

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