A 200 °C SiC Phase-Leg Power Module With Integrated Gate Drivers: Development, Performance Assessment, and Path Forward

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***Abstract*— In order to reduce the size, weight, and cost of power electronic systems, a high-temperature silicon carbide (SiC)-based half-bridge power module is proposed in this article. Two gate drivers, which were fabricated on low-temperature co-fired ceramic (LTCC) substrates, are integrated into the power module to reduce the gate loop inductance and size of the power module. The design and fabrication process of the LTCC-based gate driver is presented. In addition, the layout design, simulations, and fabrication materials of the power module are also discussed. High-temperature components and materials were implemented to fabricate the power module, which allows it to operate up to 200 °C. Double pulse tests (DPTs) were carried out from 25 °C to 200 °C to investigate its switching performance. The turn-on and turn-off dv/dt of the power module is from 10 to 15 V/ns, and little degradation was observed at elevated temperatures. While the power module achieves functional integration and promising thermal performance, the operating temperature is limited by the gate driver integrated circuit (IC). A high-temperature gate driver IC will be designed and integrated into the power module in future work to improve thermal reliability. This work provides a critical foundation for the development of high-temperature and high density power modules.**

***Index Terms*— Gate driver, high-temperature applications, low-temperature co-fired ceramic (LTCC), power module packaging, silicon carbide (SiC).**

I. Introduction

SILICON carbide (SiC) is one of the most commonly used materials in power applications due to its wide energy bandgap, high electric field strength, and high thermal conductivity [1], [2]. This significantly increases the power rating, operating voltage, and power density of power modules [3]. It has been demonstrated that SiC-based power modules show higher switching frequencies and lower losses than their silicon (Si)-based counterparts [4], [5]. In order to further reduce the size, weight, and cost of power electronic systems, a variety of methods have been proposed to facilitate the performance of SiC power modules, such as the optimization of operating temperatures, the reduction of parasitic elements, and the integration of driving circuits [6].

Scores of researchers contributed to high-temperature power modules since the increase in the operating temperature of power modules allows for the elimination of bulky cooling systems, which significantly reduces the size and cost of the system and increases the power density. In 2010, Scofield et al. [7] investigated the reliability of the packaging materials, such as substrate [i.e., direct bond copper (DBC)] and encapsulation materials, for high-temperature power modules. Based on these results, Scofield et al. [8] developed two high-temperature power modules. Cree's SiC power MOSFETs were integrated into the power module, and the power modules were characterized up to 200 °C. Meanwhile, Chen et al. [9] proposed a 1.2-kV high-temperature power module. Both SiC power MOSFETs and the power module were characterized and fully analyzed at a temperature of 200 °C.

Besides the improvement of the operating temperatures, the integration of driving circuits into power modules has also been investigated to optimize SiC-based power modules. This not only reduces the size of the system but also decreases the gate loop parasitic inductance. In 2010, silicon-on-insulator (SOI) gate driver integrated circuits (ICs) were integrated into a power module [10]. The power module shows reliable switching behaviors and relatively low-power loss. Mantooth et al. [11] also proposed a solution for the integration of gate drivers into power modules. Besides, Infineon also announced intelligent power modules with integrated gate drivers for low-power motor drives [12], [13]. These works as well as some recently published and commercially available SiC power modules are organized in Table I. According to Table I, the operating temperatures of power modules with

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TABLE I
RECENTLY PUBLISHED AND COMMERCIALLY AVAILABLE POWER MODULES

Reference	Power loop inductance	Gate loop inductance	Maximum operating temperature	Footprint		Gate driver
				Length	Width	
[7], [8]	-	-	200 °C	-	-	Not integrated
[9]	10 nH	-	200 °C	48.4 mm	42.8 mm	Not integrated
[10]	-	-	150 °C	-	-	Integrated
[12], [13]	-	-	125 °C	34 mm	27 mm	Integrated
[14]	6.7 nH	-	175 °C	80 mm	53 mm	Not integrated
[15]	4.9 nH	-	175 °C	110 mm	62 mm	Not integrated
[16]	15 nH	74 nH	150 °C	106.4 mm	61.4 mm	Not integrated
[17]	8.4 nH	-	150 °C	-	-	Integrated
[18]	1.3 nH	20 nH	150 °C	-	-	Not integrated
[19]	4.3 nH	6 nH	-	-	-	Not integrated
[20]	3.8 nH	-	-	25.1 mm	18.8 mm	Not integrated
[21]	13.8 nH	-	150 °C	40 mm	40 mm	Not integrated

integrated gate drivers are limited at ∼150 °C, and isolators were normally not designed in these gate driver circuits to protect low-voltage logic controllers [10], [17]. Therefore, the development and investigation of high-temperature SiC-based power modules with integrated gate driver circuits are still highly desirable for high-density power electronic systems.

Optical isolators (e.g., optocouplers and optical fibers) and magnetic isolators (e.g., transformers) are often used as galvanic isolation devices in gate driver circuitry to protect low-voltage controlling devices from high voltage [22], [23]. Typically, transformers were implemented as isolators for high-temperature applications [24]. However, the transformers usually consume a large area of the gate driver circuits, and the modulation and demodulation circuits increase the complexity of the circuit design. Therefore, in previous work [25], [26], [27], [28], [29], [30], [31], high-temperature optocouplers as galvanic isolators for SiC power modules were proposed and developed. In order to develop high-temperature optocouplers, high-temperature light-emitting diodes (LEDs) and photodiodes were designed and characterized with a wide range of temperatures (i.e., from −200 °C to 500 °C) [25], [26], [27], [28], [29]. Both the LEDs and photodiodes showed good performance at high-temperature conditions. Then, the LEDs and photodiodes were used as emitters and detectors, respectively, and packaged with low-temperature co-fired ceramic (LTCC) materials to form high-temperature optocouplers [30], [31]. Fig. 1(a) and (b) shows the cross section and fabricated sample of the LTCC-based high-temperature optocouplers, respectively. The emitters and detectors are attached and wire-bonded to the LTCC-based chip carriers, and the LTCC-based chip carriers are connected to the LTCC substrate, allowing the devices to face each other through the cavity. Then, the optocouplers were integrated into LTCC substrates, and LTCC-based gate drivers were fabricated [31]. The LTCC-based gate drivers were characterized and analyzed from 25 °C to 250 °C. The results proved the LTCC-based gate driver showed reliable driving capability. After that, the LTCC-based gate drivers were integrated into the SiC power module [32], [33]. However, the maximum operating temperature of the power module is ∼100 °C due to the temperature tolerance of the packaging materials (i.e., encapsulant), and the power modules were not fully characterized at high temperatures.

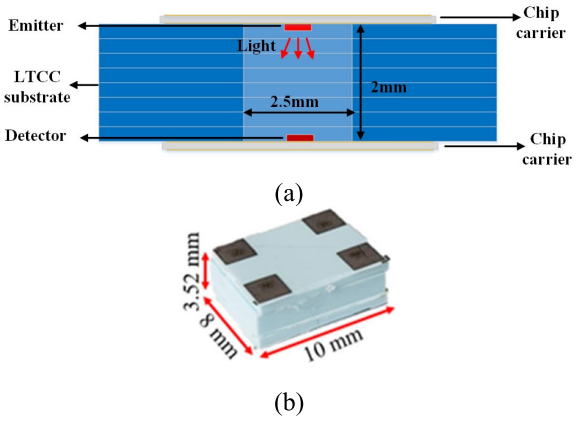


Fig. 1. (a) Cross section and (b) fabricated sample of the LTCC-based high-temperature optocoupler developed in previous works.

In this article, a high-temperature half-bridge power module with integrated gate drivers was proposed. High-temperature packaging materials were utilized, which allowed the SiC power module to operate at 200 °C. Two gate drivers, which were fabricated on LTCC substrates, were integrated into the power module to achieve a compact size for the system. This article is divided as follows. Section II presents the design and fabrication process as well as the characterization of the LTCC-based gate driver. In Section III, the design, fabrication, and characterization of the high-temperature power module are discussed. The 1.2-kV SiC MOSFETs were utilized as power switches, and high-temperature packaging materials were utilized for the encapsulation. Electrothermal simulations were carried out to analyze the performance of the power module. Double pulse tests (DPTs) were conducted from 25 °C to 200 °C to characterize the power module. The power module showed reliable switching behaviors at elevated temperatures (i.e., 200 °C). Finally, the conclusion is provided in Section IV.

II. LTCC-BASED GATE DRIVER

A. Design

SiC-based power modules require relatively low parasitic inductance due to their high switching speed. In order to

TABLE II
PROPERTIES OF LTCC AND FR4 PCB

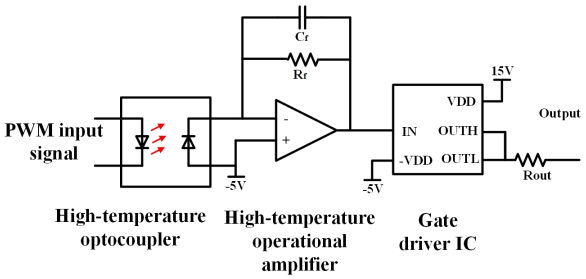
Material	LTCC	FR4 PCB
CTE (ppm/K)	4.4	15
Maximum operating temperature (°C)	450	150
Thermal conductivity (W/mK)	4.6	0.4

mitigate parasitics and reduce the passive components (e.g., decoupling capacitors and gate resistors), gate driver circuits are desired to be closely integrated with SiC power devices. Consequently, SiC power modules with embedded printed circuit boards (PCBs) have been proposed [34], [35]. The PCBs cannot only be substrates for passive and driving components but also provide extra flexibility to the layout. However, the temperature tolerance of PCB and its coefficient of thermal expansion (CTE) mismatch with SiC and the ceramic substrate (i.e., DBC) of power modules limit the operating temperature of SiC power modules. To solve this issue, in this article, LTCC is utilized as the substrate material of the gate driver circuit. LTCC technology utilizes a multilayer fabrication process, which allows for the creation of vias, interconnects, cavities, and embedded traces. This makes it well suited as a substrate for semiconductor devices and ICs. In addition, LTCC-based components have also been demonstrated to be easily integrated with power modules [36], [37]. Table II lists the properties of LTCC and FR4 PCBs. Compared to FR4 PCBs, LTCC has a closer CTE to SiC (i.e., 4.2 ppm/K) and the ceramic substrate (e.g., AlN DBC and Si_3N_4 DBC) of power modules. Moreover, its maximum operating temperature and thermal conductivity are much higher than those of a PCB. These make the LTCC substrates more promising to be integrated into power modules than PCB substrates.

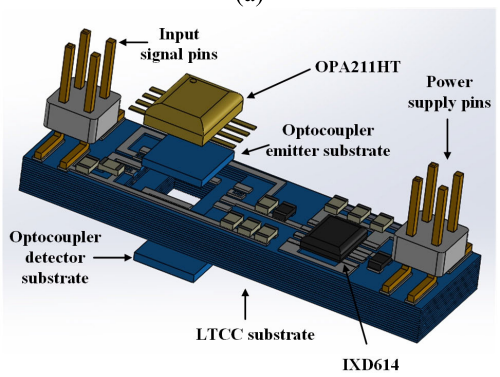
Fig. 2(a) and (b) shows the schematic and the 3-D model of the LTCC-based gate driver, respectively. A high-temperature optocoupler, which was developed in previous work [30], [31], was used as the galvanic isolation device. A transimpedance amplifier (TIA, i.e., OPA211HT by Texas Instruments (TI) with a maximum operating temperature of 210 °C) is used to convert the optocoupler output current to voltage, and a gate driver IC (i.e., IXD614) is utilized to drive the power devices. High-temperature resistors [38] and capacitors [39] (both by Vishay), which are capable of operating at 200 °C, are utilized. As shown in Fig. 2(b), two slots were designed on the top and bottom sides of the LTCC substrate for the integration of the high-temperature optocoupler. Passive components (e.g., resistors and capacitors) and ICs are attached to the top layer of the LTCC substrate. The output signal traces are located on the bottom side of the LTCC, which makes it easy to connect with the power module substrate and the power devices.

B. Simulation

The major challenge of the gate driver design is the tradeoff between the propagation delay and the stability of the circuit. Due to the low optocoupler output current at high temperatures, a high transimpedance gain of the TIA is required. This limits TIA's stability and rise/fall time, which affects the



(a)



(b)

Fig. 2. (a) Schematic and (b) 3-D model of the LTCC-based gate driver.

propagation delay of the gate driver circuit. Thus, in order to optimize the performance of the gate driver circuit, the TIA was simulated by LTSPICE. Fig. 3(a) shows the simulation schematic of the TIA. The model of the operational amplifier (i.e., OPA211) was provided by TI. The optocoupler is modeled as a current source with a 54-pF junction capacitance, C_{in}. The output current of the current source was 50 μA, which is its output current at 200 °C. The transimpedance gain is determined by the feedback resistor, R_f, which can be expressed as

$$V_{\text{out}} = R_f I_{ph} \tag{1}$$

where V_{out} is the TIA output and I_{ph} is the optocoupler output current. R_f was set as 62 kΩ, which makes V_{out} higher than the threshold voltage of the gate driver IC (i.e., 3 V). The TIA circuit is a two-pole system, and the poles can be expressed as [40]

$$s = -\omega_0\left(\frac{1}{2Q} \pm \frac{1}{2}\sqrt{\frac{1}{Q^2} - 4}\right) \tag{2}$$

$$\omega_0 = \sqrt{\frac{A_0 + 1}{R_f C_{\text{in}} T_A}} \tag{3}$$

$$Q = \frac{\sqrt{(A_0 + 1) R_f C_{\text{in}} T_A}}{R_f C_{\text{in}} + T_A} \tag{4}$$

where A_0 and T_A are the dc gain and the time constant of the pole for the operational amplifier, respectively. When Q is higher than 0.707, which normally results from a high $R_f C_{\text{in}}$ value, the values of s are complex conjugates, and the circuit is not stabilized [40]. In order to stabilize the circuit, a feedback capacitor, C_f, was added in parallel to the feedback resistor.

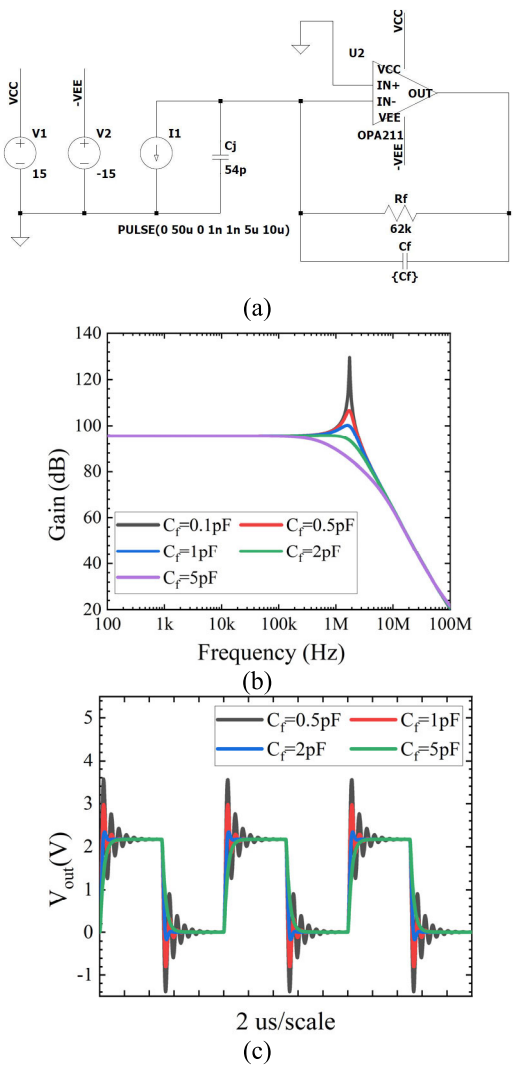


Fig. 3. Simulated (a) schematic, (b) ac response, and (c) output waveforms of the TIA.

The feedback capacitor introduces a zero, which compensates the poles. The zero can be expressed as [40]

$$z = \frac{1}{2\pi R_f C_f}. \tag{5}$$

The simulated ac responses and output voltage waveforms with varying C_f are shown in Fig. 3(b) and (c), respectively. When $C_f < 1$ pF, high amplitude peaking and strong rings are observed in the frequency domain and time domain, which indicates a not stabilized circuit. When $C_f \geq 2$ pF, smooth ac response and output waveforms can be observed. However, when C_f is 5 pF a high rise/fall time is also observed in the output waveform due to the low bandwidth of the ac response. Therefore, a 2-pF feedback capacitor was selected for the design of the TIA circuit.

C. Fabrication

The LTCC-based gate drive substrate is composed of 16 layers of individual LTCC. The layout of all the layers with vias, traces, and cavities is designed in AutoCAD. Then, the metal traces, pads, vias, and cavities were extracted to generate masks for the LTCC fabrication process. 4 shows the steps of the fabrication process. Dupont 9K7 LTCC sheets with a thickness of 10 mil are used. These LTCC sheets are compatible with silver (Ag) and gold (Au) paste and have a CTE of 4.4 ppm/K and a thermal conductivity of 4.6 W/mK, which makes them a highly suitable material for the manufacturing of integrated gate drives. As shown in Fig. 4, the fabrication process started with the cavity and via punching in LTCC sheets. The punched vias were filled with co-fired silver via fill paste (i.e., Dupont LL601), which has the ability to withstand 850 °C [41]. Then, the sheets were dried at 70 °C for 10 min. The dry sheets were screen-printed with silver paste Dupont LL612 Ag and Dupont LL617 AgPd for the internal (nonsolderable traces) and external (solderable) trace formation in the LTCC sheets, respectively (i.e., conductor printing) [41]. After the screen printing, they were heated at 70 °C for 15 min to cure. The cured sheets were then cut into sections, stacked one layer on top of the other, and laminated at a pressure of roughly 2500 lbf/in^2. The laminated LTCC substrates were sintered and cured at 850 °C for 27 h (i.e., cooking), and the cured substrates were then diced to form the individual LTCC substrates. Finally, components, such as optocouplers, resistors, capacitors, and ICs, were attached to the LTCC substrates. The fabricated LTCC-based gate driver is shown in Fig. 5.

D. Characterization

The LTCC-based gate driver was characterized from 25 °C to 200 °C to investigate its performance. The experimental setup is shown in Fig. 6. The LTCC-based gate driver was placed on a Corning PC-600D hot plate, and thermal grease was applied to achieve a uniform temperature distribution during the measurements. An input signal with 100-kHz frequency and 50% duty cycle was generated by the Rigol DG1022 function generator, and the output waveforms of the TIA and gate driver were captured by an oscilloscope (i.e., MOD4034 by Tektronix). The output waveforms are shown in Fig. 7(a)–(c). The output voltage (peak to peak) of the TIA decreases from 4.5 to 3 V when the temperature increases from 25 °C to 200 °C due to the degradation of the optocoupler. This resulted in the turn-on propagation delay increasing from ∼330 to ∼760 ns, and the turn-off propagation delay decreasing from ∼280 to ∼200 ns [Fig. 7(d)]. However, the output voltage of the gate driver shows little degradation at 200 °C. This proves that the gate driver is capable of driving power devices at elevated temperatures.

DPTs were carried out to characterize the switching performance of the LTCC-based gate driver circuit. The DPT setup is shown in Fig. 8. The LTCC-based gate driver was attached to a transfer board that is made by PCB. A commercial 1.2-kV SiC power module (i.e., CAS300M12BM2 by CREE) was used to investigate the driving capability of the gate driver. Besides, a PCB-based gate driver, which has the same schematic [i.e., Fig. 2(a)] as the LTCC-based gate driver, was also tested as a comparison. The DPT results were captured by a MOD4034 oscilloscope (by Tektronix).

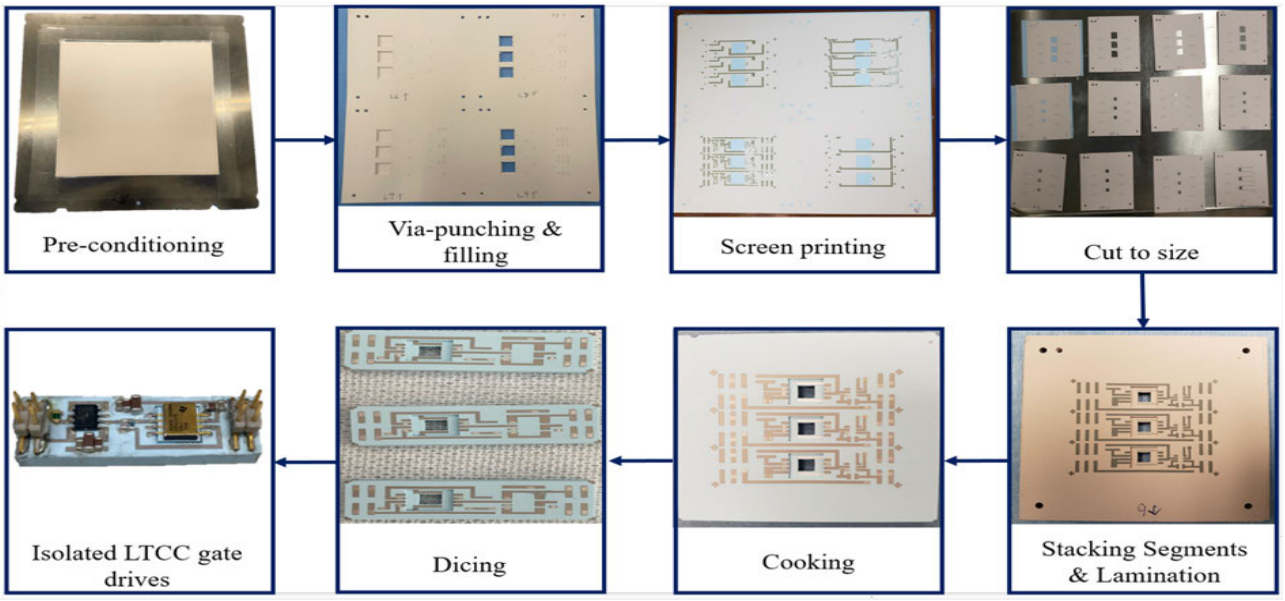


Fig. 4. Fabrication process of LTCC-based gate drivers.

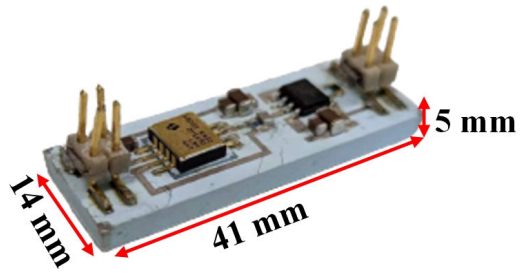


Fig. 5. Fabricated LTCC-based SiC MOSFET gate driver.

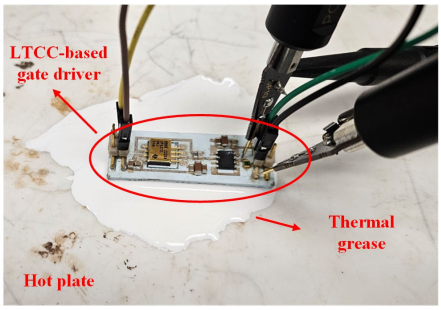


Fig. 6. Experimental setup for the LTCC-based gate driver with varying temperatures.

A voltage probe (Tektronix P6139A with 500-MHz bandwidth), a high-voltage differential probe (Tektronix P5200A with 50-MHz bandwidth), and a Rogowski coil (i.e., PEM CWT with 30-MHz bandwidth) were utilized to measure the gate–source voltage, drain–source voltage, and drain–source current, respectively. Fig. 9 shows the DPT results of the gate drivers. The drain–source voltage (V_{ds}) was set at 600 V, and the maximum drain–source current (I_{ds}) was 120 A. The LTCC-based gate driver shows good switching performance with a 10-Ω external gate resistor (R_g), which results in ∼5- and ∼6-V/ns dv/dt at turn-on and turn-off conditions. When R_g is 1 Ω, dv/dt of turn-on and turn-off increases to ∼12 V/ns. However, mistriggers were observed after the second pulse. The PCB-based gate driver with $R_g = 1\ \Omega$ shows good switching performance at this condition (i.e., $dv/dt =$ ∼12 V/ns). The switching of the power devices generates electromagnetic interference (EMI) noise, which affects the gate driver circuit. The common-mode EMI noise current that affects the gate driver, $I_{\text{noise\_}GD}$, can be expressed as [42] and [43]

$$I_{\text{noise\_}GD} = \frac{C_{CM} \cdot C_{GD\_\text{ground}}}{C_{CM} + C_{GND\_\text{ground}} + C_{GD\_\text{ground}}} \cdot \frac{dv_{ds}}{dt} \tag{6}$$

where C_{CM} is the parasitic capacitance between the floating potential of the half-bridge circuit and ground, C_{GND_ground} is the parasitic capacitance between the gate driver GND and ground, and C_{GD_ground} is the sum of the parasitic capacitance between the gate driver and ground (except for C_{GD_ground}). In terms of (6), low C_{GD_ground} and high C_{GND_ground} are normally desired to reduce the EMI noise. The relative permittivity of LTCC (i.e., ∼7.5) is slightly higher than that of PCB (i.e., 5.5) [44], which indicates a higher C_{GD_ground} of the LTCC-based gate driver. Besides, since the metal routing and layout of the LTCC substrate are limited by its process, it is difficult to create a shielding GND plane, which indicates a lower C_{GND_ground}. Therefore, the LTCC-based gate driver has less EMI noise immunity than the PCB-based gate driver and shows a relatively low switching speed when driving the power module.

The isolation voltage of the LTCC-based gate driver was also characterized. Fig. 10(a) shows the setup of the isolation voltage measurement. Since the isolation voltage is mainly determined by the optocoupler, only the emitter and detector of the optocoupler were attached to the LTCC substrate. A Valhalla 5880A dielectric analyzer was used to characterize the isolation voltage. The positive probe was placed on the

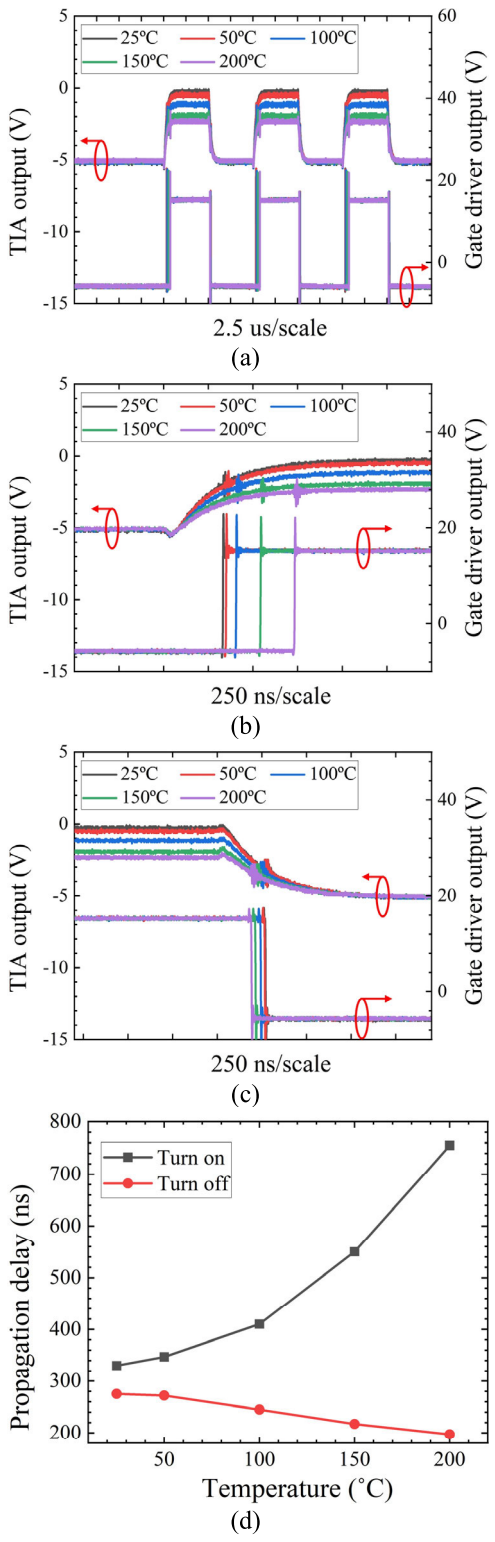


Fig. 7. LTCC-based gate driver measurement results (a) overview waveforms, (b) turn-on waveforms, (c) turn-off waveforms, and (d) propagation delay with varying temperatures.

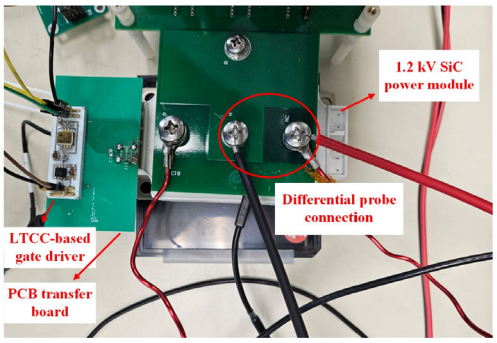


Fig. 8. DPTs setup of the LTCC-based gate driver.

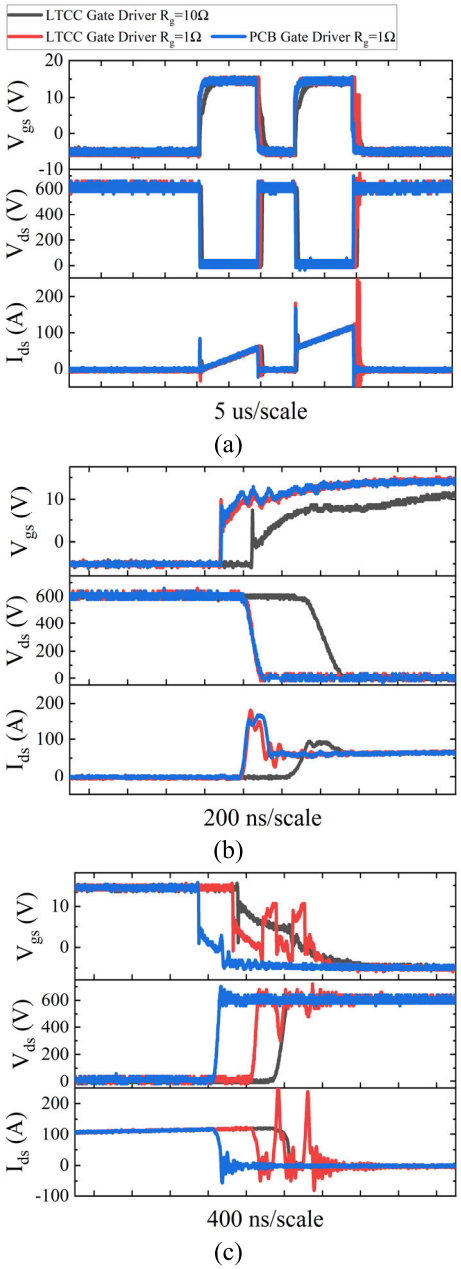


Fig. 9. DPT results of the gate drivers (a) overview waveforms, (b) turn-on waveforms, and (c) turn-off waveforms.

detector output, and the negative probe (i.e., ground) was placed on the emitter input. The maximum isolation voltage is registered when the leakage current crosses 100 nA. Fig. 10(b) shows the isolation voltage measurement result of the LTCC-based gate driver with varying temperatures. As shown in Fig. 10(b), the isolation voltage is 2900 V at 25 °C. The isolation voltage mainly depends on the air

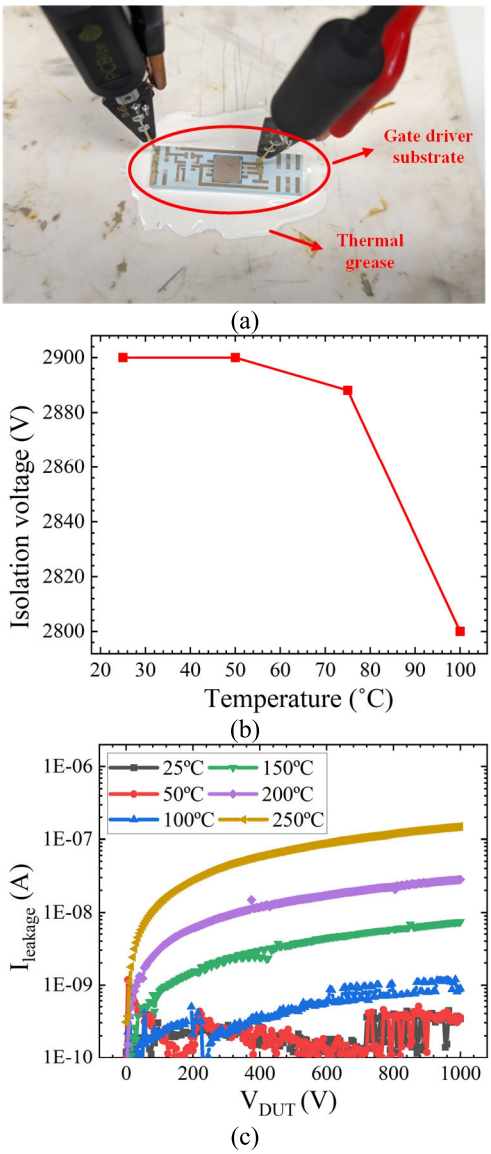


Fig. 10. (a) Isolation measurement setup, (b) isolation voltage, and (c) leakage current of the LTCC-based gate driver with varying temperatures.

breakdown between the optocoupler's emitter and detector. Since the distance between the emitter and detector is ∼1 mm, the air breakdown voltage is 30 kV/cm, and the isolation voltage of the LTCC-based gate driver is 2900 V. The isolation voltage decreases to 2800 V at 100 °C due to the decrease in air breakdown with the increase in temperature. Since the maximum temperature of the hot plate for the dielectric analyzer system is 100 °C, and the leakage current was not recorded by the dielectric analyzer, a Keithley 2470 source measure unit (SMU) was utilized to perform the measurement at higher temperatures. Fig. 10(c) shows the leakage current of the LTCC substrate with varying temperatures. The leakage current is lower than 1 nA at 1000 V when the temperature is lower than 100 °C. It increases to ∼28 nA at 200 °C. At 250 °C the isolation voltage drops to ∼680 V due to the decrease in the air breakdown voltage.

TABLE III
COMPONENTS FOR HIGH-TEMPERATURE POWER MODULE

Component	Material	Specification
Base plate	Cu	Au plated
DBC	Cu-AlN-Cu	Au plated 0.2 mm Cu 0.6 mm AlN
Switch	SiC MOSFETs	1.2 kV 149 A
Bond wire	Al	5 mil for gate loop 12 mil for power loop
Terminal	Cu	Au plated
Housing	Epoxy resin	300 ºC
Encapsulant	Silicone	Nusil R-2188 250 ºC

III. SiC-BASED HIGH-TEMPERATURE POWER MODULE

Although the fabricated LTCC-based gate driver shows limited switching speed, it provides an efficient way for system integration of high-temperature power modules. Consequently, a high-temperature SiC-based half-bridge power module with integrated LTCC-based gate drivers was designed and fabricated.

A. Design

Fig. 11(a) and (b) shows the layout and 3-D model of the proposed high-temperature SiC power module, respectively, and the components used for the power module are listed in Table III. Copper (Cu) was selected as the baseplate material due to its high thermal conductivity (i.e., 398 W/mK). AlN-based DBC was utilized as the substrate of the power module since AlN has a high thermal conductivity (i.e., 150 W/mK) and a close CTE (i.e., 4.6) to SiC. Gold (Au) was plated on both the baseplate and DBC substrate to prevent the oxidation of Cu. As shown in Fig. 11(a), 1.2-kV SiC power MOSFETs from CREE (i.e., CPM3-1200-0013A) are integrated into the power module. Each position has three devices in parallel. Two LTCC-based gate drivers are attached to the DBC and connected to the power devices with Cu traces (on the DBC) and bond wires. The integration of the gate drivers reduces not only the size of the power electronic system but also the gate loop parasitic inductance. Aluminum (Al) was selected as the material for bond wires (Table III) due to its reliable bonding quality. Since the gate pads of power devices are fragile, 5-mil Al wires were bonded for the gate loop. The 12-mil Al bond wires were used for the power loop connection to increase the current carrying capability. As shown in Fig. 11(b), the dc^+ and dc^- power terminals are placed facing each other to enhance the mutual inductance, which helps to decrease the power loop parasitic inductance. The power terminals are designed to be almost as wide as the DBC (i.e., ∼40 mm) to reduce the power loop parasitic inductance. Moreover, high-temperature peak carbon material was used to build the housing and lid structures to increase thermal reliability.

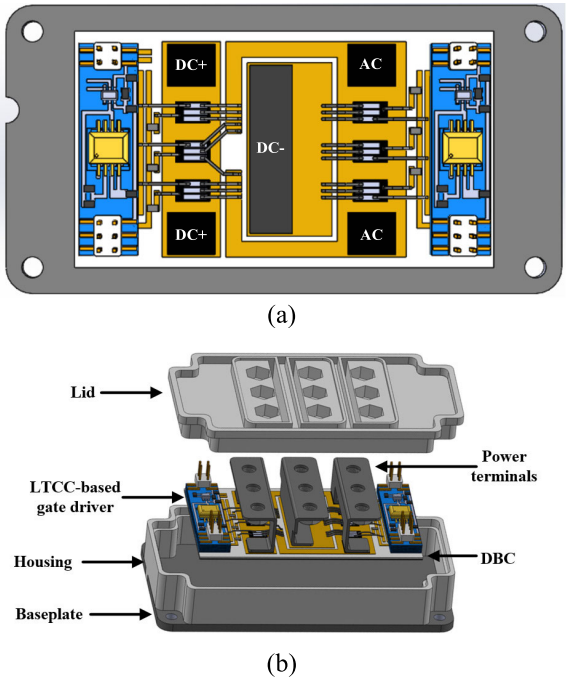


Fig. 11. (a) Layout and (b) 3-D model of the proposed high-temperature SiC-based half-bridge power module.

B. Simulations

The parasitic gate loop inductance, L_g, and power loop inductance, L_s, play a significant role during the operation of the power module. Therefore, the parasitic inductance of the power module was extracted by ANSYS Q3D. Fig. 12 shows the extracted gate loop and power loop inductance. For the power loop simulation, the source and sink were applied on the dc^+ and dc^- terminals, respectively. For the gate loop simulation, the output pad of the LTCC-based gate driver and the gate pads of the power devices were set as source and sink. It should be noted that the gate loop inductance shown in Fig. 12 is the average value of the three parallel power devices. As shown in Fig. 12, the power loop inductance is ~7.5 nH at 1 MHz, which is at the same level as commercial SiC power modules [14], [15]. The gate loop inductance, which is mainly created by Al bond wires, is ~9.5 nH at 1 MHz. Since the gate drivers are closely integrated with the SiC power devices, the gate loop inductance of the proposed power module is much lower than that of commercial SiC power modules (i.e., 50–70 nH), as reported in [16] and [45].

In order to estimate the maximum operating current of the proposed power module with varying temperatures, an electrothermal simulation was carried out by ANSYS Workbench. The maximum operating current is limited by the melting point of the solder paste for the terminal attachment (i.e., 218 °C). As a result, the maximum operating current was set when the terminal temperature reached 215 °C. Fig. 13(a) shows the thermal distribution of the proposed power module with 450 A (i.e., maximum drain–source current of the SiC power devices) at the ambient temperature of 25 °C. The maximum temperature, which is located on the power devices, is ~240 °C, and the temperatures at the terminals

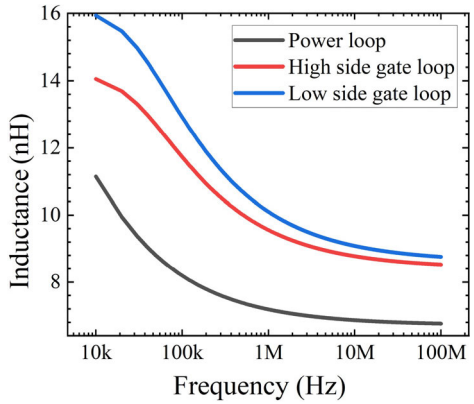


Fig. 12. Simulated parasitic inductance versus operating frequency.

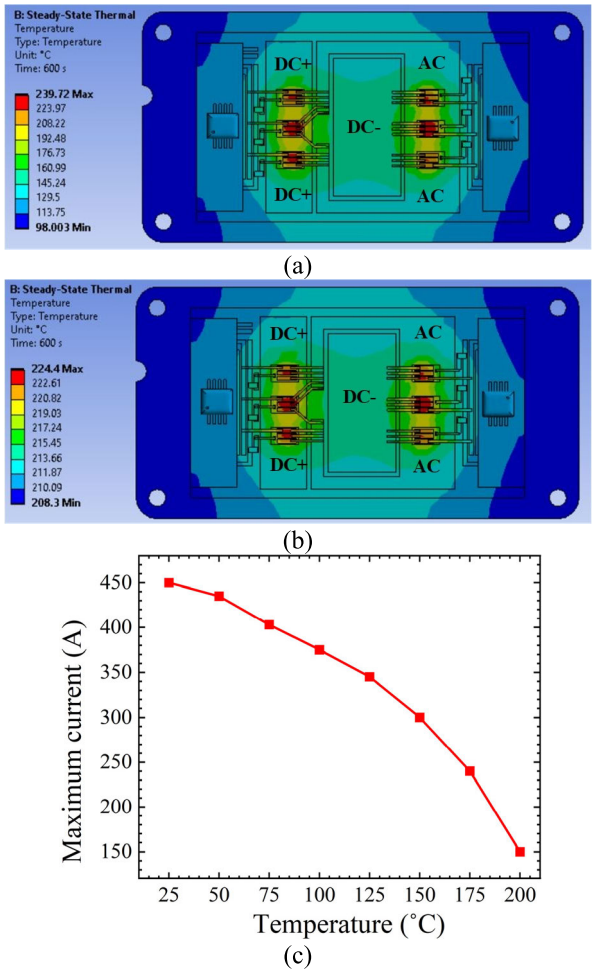


Fig. 13. Thermal simulation results (a) 25 °C ambient temperature and 450-A operating current, (b) 200 °C ambient temperature and 150-A operating current, and (c) maximum operating current with varying temperatures.

are ~175 °C. Fig. 13(b) shows the thermal distribution of the proposed power module with 150-A operating current at 200 °C. Although the maximum temperature in the device is ~224 °C, the temperatures at the terminals are ~215 °C. Thus, the maximum operating current is limited to 150 A at 200 °C. The maximum operating current of the power module with varying temperatures is extracted in Fig. 13(c).

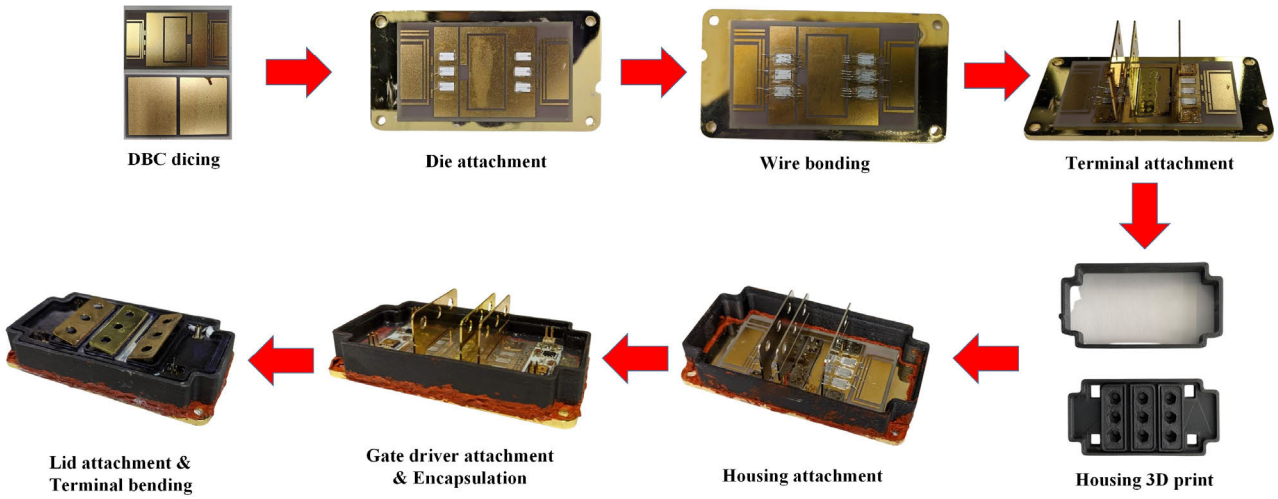


Fig. 14. Fabrication process of the high-temperature SiC-based half-bridge power module.

C. Fabrication

The fabrication process of the proposed high-temperature SiC half-bridge power module is shown in Fig. 14, and the solder and adhesive used for the fabrication are listed in Table IV. First, the DBC substrates were diced by a dicing saw to form the desired sizes. Then, a plasma clean process was performed on the DBC and baseplate to remove the organic contamination and ensure a high-quality die attachment process. The die attachment process was carried out by silver sintering. Silver (Ag) paste (i.e., H9890-6A from NAMICS) was utilized to adhere to the power devices, DBC substrate, and baseplate. The silver sintering process was conducted in a nitrogen oven at a maximum temperature of 200 °C. It should be noted that the bottom copper of the DBC was separated into two parts with a 1-mm gap, and the baseplate was prebended by ~100 μm to avoid the issues caused by the baseplate warpage during the high-temperature process. After the die attachment process, Al bond wires were bonded from the power devices to the DBC substrate to form the connection. Then, Cu terminals were attached to the DBC substrate by a Sikama Falcon 5C reflow oven. Subsequently, the housing wall was printed by a 3-D printer and attached to the baseplate with RTV106 high-temperature epoxy. Then, the LTCC-based gate drivers were attached to the DBC substrate by CW2400 conductive epoxy, and high-temperature silicone (i.e., Nusil R-2188, Table III) was used to coat the power devices, bond wires, and gate drivers (i.e., encapsulation process). The encapsulation process was carried out at room temperature for 24 h to remove the air bubbles trapped in the silicone and then performed at 150 °C for 1.5 h to cure the silicone. Finally, the lid was attached to the power module, and the terminals were bent. The length, width, and height of the fabricated power module are 105, 55, and 18 mm, which are similar to commercial half-bridge power modules [14], [15], [16] listed in Table I.

D. Characterization

DPTs were carried out on the high-temperature SiC power module from 25 °C to 200 °C to characterize its switching performance. Fig. 15(a) shows the experimental setup of the DPTs. A 90-μH inductance was used as the load, and a function generator (Rigol DG1022) was used to generate a double pulse signal with a 9-μs pulsewidth and a 15-μs period. The DPT results were captured by an oscilloscope (i.e., MOD4034 by Tektronix). A high-voltage differential probe (i.e., Tektronix P5200A) and a Rogowski coil (i.e., PEM CWT) were implemented to measure the drain–source voltage and drain current, respectively. In addition, the power module was heated by a Corning PC-600D hot plate, and thermal grease was applied between the hot plate and the power module to improve the thermal distribution. After the hot plate reached the testing temperature, the power module was heated for 10 min to achieve a uniform heat distribution. The temperature was monitored by a thermal camera. The thermal map of the DPT at 200 °C is shown in Fig. 15(b).

Both the high side and low side of the half-bridge power module were characterized. Since the results are very similar, only high-side device switching behaviors are presented in this article. In order to fully characterize the switching speed of the proposed power module, DPTs with varying gate resistors, R_g, were carried out at 25 °C. The results are shown in Fig. 16(a), and Fig. 16(b) and (c) shows turn-on and turn-off waveforms with a 600-V drain voltage and 120-A maximum

TABLE IV
SOLDER AND ADHESIVE FOR POWER MODULE FABRICATION

Parts	Materials	Maximum temperature	Fabrication process
H9890-6A	Ag	260 ºC	DBC & die attachment
SAC305	Sn/Ag/Cu	218 ºC	Terminal attachment
CW2400	Conductive epoxy	343 ºC	Gate driver attachment
RTV106	Epoxy	260 ºC	Housing attachment

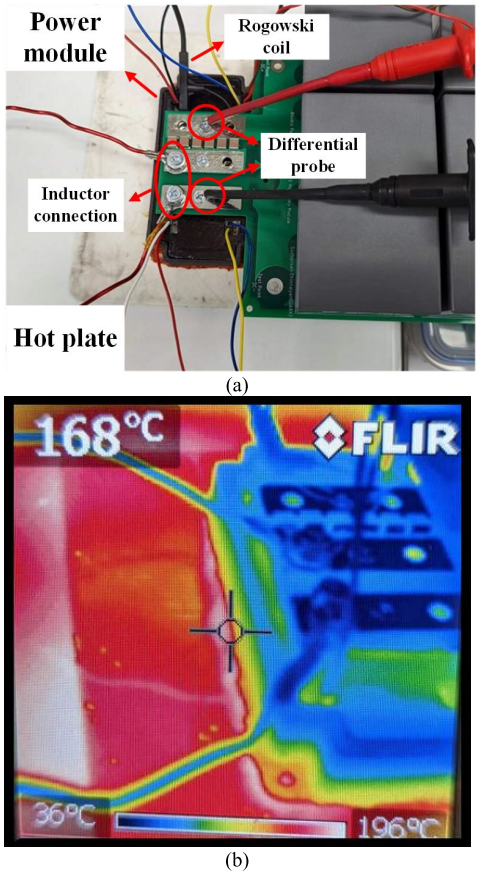


Fig. 15. (a) Experimental setup and (b) thermal map at 200 °C of the DPTs.

drain current, respectively. The proposed power module shows good switching performance when R_g is higher than 5 Ω. Very little voltage and current oscillations were observed during the device switching. The overshoot voltage, ΔV_{DS}, during turn off, is ∼102 V, and the voltage turn-on and turn-off time are 60.48 and 36.08 ns with $R_g = 5$ Ω, respectively. It should be noted that the power module shows a false trigger when R_g is 3 Ω. dv/dt of the proposed power module is limited at ∼16 V/ns due to the low EMI noise immunity of the LTCC-based gate driver.

DPTs were also conducted from 25 °C to 200 °C to characterize the high-temperature performance of the proposed power module. An 8-Ω gate resistor was utilized, and the results are shown in Fig. 17(a)–(c). The power module shows reliable switching performance from 25 °C to 200 °C. The turn-on pulsewidth decreases from 9 to ∼8.7 μs at 200 °C due to the degradation of the high-temperature optocoupler output current at elevated temperatures. dv/dt of the power module is extracted in Fig. 18. The turn-on and turn-off dv/dt of the proposed power module is from 10 to 15 V/ns and shows little degradation with the temperature varying from 25 °C to 200 °C. During the turn-on and turn-off periods, very few voltage oscillations were observed from 25 °C to 200 °C due to the low-power loop inductance of the proposed power module.

The current overshoot at the device turn-on period increases from ∼26 to ∼34 A with the temperature varying from 25 °C to 200 °C. This is mainly contributed by the charging and

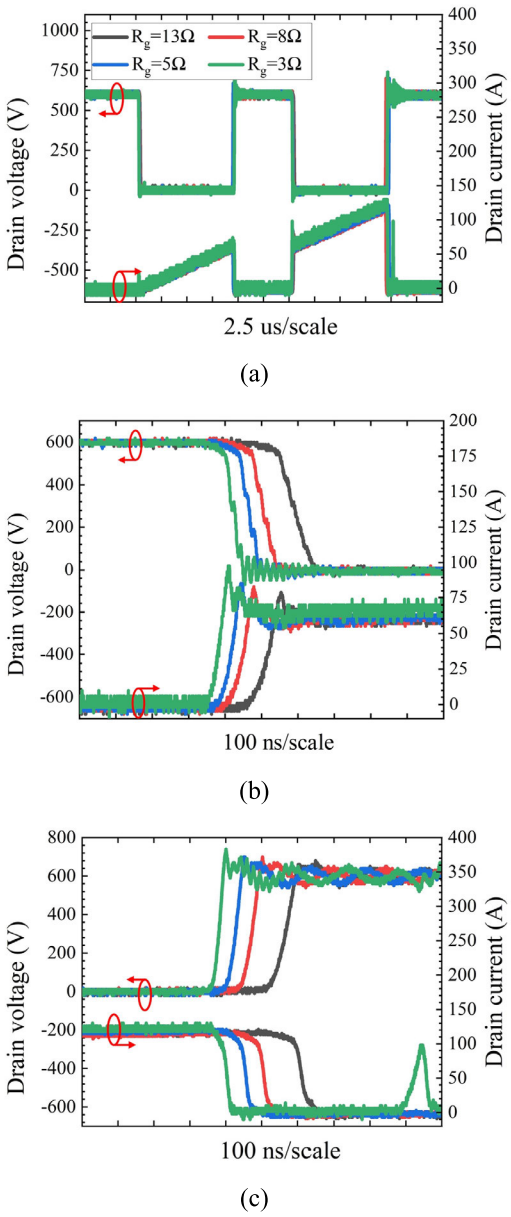


Fig. 16. DPT results of the high-temperature SiC half-bridge power module with varying gate resistors (a) overview waveforms, (b) turn-on waveforms, and (c) turn-off waveforms.

reverse recovery current of the power MOSFETs' body diodes. When the high-side power MOSFETs turn on, they operate as a current source and charge the power loop parasitic inductance and the body diodes of the low-side power MOSFETs. This generates a current overshooting, ΔI_{DS}, that is given by [46]

$$\Delta I_{DS} = \frac{di_{DS}}{dt}\sqrt{2C_D L_{\text{loop}}} \tag{7}$$

where C_D is the junction capacitance of the body diodes. During the turn-on period

$$\frac{di_{ds}}{dt} = \frac{g_{fs}(V_{GH} - V_{TH})}{(R_g + R_{g,\text{int}})C_g + g_{fs}L_s} \tag{8}$$

where g_{fs}, V_{TH}, C_g, and L_s are the transconductance, threshold voltage, gate parasitic capacitance, and source parasitic

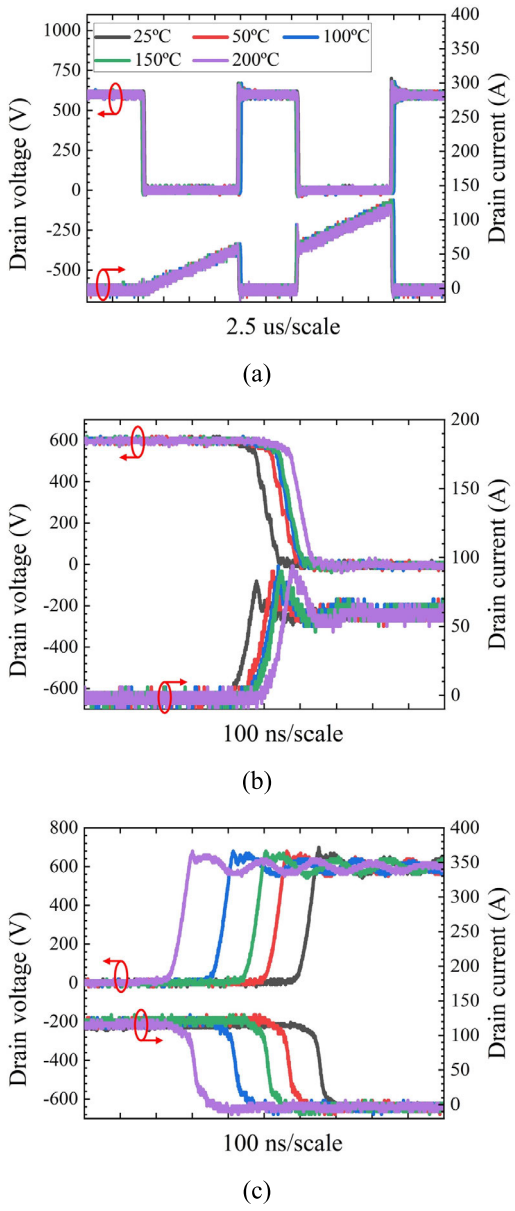


Fig. 17. DPT results of the high-temperature SiC half-bridge power module from 25 °C to 200 °C (a) overview waveforms, (b) turn-on waveforms, and (c) turn-off waveforms.

inductance of the power MOSFETs, respectively; V_{GH} is the maximum gate voltage (i.e., 15 V); and $R_{g,\text{int}}$ is the internal gate resistance [47], [48]. According to the datasheet of the power MOSFETs [49], V_{TH} decreases with the increase in the temperature, and g_{fs} shows little change with the temperature. Therefore, di_{ds}/dt increases due to the decrease in V_{TH}, which increases the current overshoot.

Moreover, the reverse recovery current of the low-side body diodes may also contribute to the overshoot current. During a body diode turn-on period, minority carriers are stored at the depletion region. When the body diode switches off, a reverse recovery current is generated by the stored minority carriers. The reverse recovery current, I_R, can be expressed as [50]

$$I_R(t) = \frac{dQ_r(t)}{dt} + \frac{Q_r(t)}{\tau} \tag{9}$$

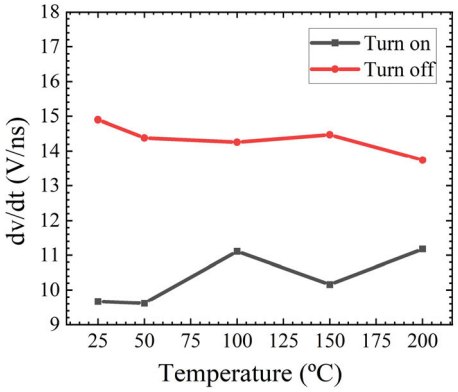


Fig. 18. Switching speed of the proposed power module with temperatures.

where Q_r is the minority carrier charge and τ is the minority carrier lifetime. When $t = 0$

$$Q_r(0) = \tau \cdot \frac{I_F}{A} \tag{10}$$

where I_F is the forward current and A is the junction area. Since the minority carrier lifetime increases with the increase in the temperature, the minority carrier charge increases when the temperature increases. This may lead to an increase in the reverse recovery current and current overshooting.

IV. Conclusion

This article proposes a high-temperature SiC-based half-bridge power module with built-in gate drivers, which makes SiC power modules compact and increases the density of power electronic systems. The integrated gate drivers were fabricated on LTCC substrates to achieve better thermal reliability, such as CTE fit, operating temperature, and thermal conductivity, than PCB substrates. High-temperature optocouplers, which were developed in previous work, were utilized as the galvanic isolators to compact the LTCC-based gate drivers. The design considerations and fabrication process of the LTCC-based gate driver are discussed. LTSPICE simulations were carried out to optimize the circuit performance. In addition, DPTs were carried out on the LTCC-based gate driver with a commercial power module to characterize the driving capability. The output waveforms and isolation voltage of the gate driver with varying temperatures were also characterized. After the fabrication and characterization of the LTCC-based gate driver, the design, simulation, and fabrication of the high-temperature SiC power module with integrated gate drivers are discussed. The extracted gate loop and power loop inductance values are ~9.5 and ~7.5 nH according to ANSYS Q3D simulations, and the maximum operating current with varying temperatures was simulated by ANSYS Workbench. DPT was carried out to characterize the power module. The turn-on and turn-off times of the power module showed little degradation from 25 °C to 200 °C, and little voltage overshoot was observed. The turn-on current overshoot increases from 26 to 34 A with the temperature varying from 25 °C to 200 °C. This is mainly due to the charging and reverse recovery current of the power MOSFETs' body diodes.

In general, although the proposed high-temperature power module with integrated gate drivers shows a relatively low switching speed, it achieves low loop inductance, a high operating temperature, and a compact size. In future work, the layout, metal routing, and the utilized components of the LTCC-based gate driver will be improved to enhance the switching speed of the power module. Since the gate driver IC (i.e., IXD614) was not designed for high-temperature applications, a high-temperature gate driver IC will be designed and integrated into the power module in future work to improve thermal reliability. Besides, the terminal attachment process will be improved by replacing the solder (i.e., SAC305) to further increase the operating temperature.

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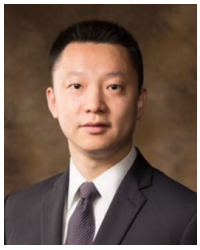

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