

On-wafer S-parameter Characterization of a D-band SIW Power Divider using Two-Port VNA

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Abstract — In this work, on-wafer S-parameter characterization of a three-port substrate-integrated-waveguide (SIW)-based D-band power divider is reported, using a two-port VNA. In this configuration, the third port is terminated with a selection of known impedances to enable full extraction of the 3-port S-parameter matrix. A novel methodology for selecting the third-port impedance is proposed for S-parameter reconstruction. To assess the power splitter performance, the reconstructed three-port S-parameters were de-embedded using a thru-reflect-line algorithm, followed by time-domain-gating, and achieved an excess loss of 0.7 ± 0.1 dB and an input return loss of 25 ± 7 dB over the D band (110–170 GHz).

Index Terms — Multiport network, scattering matrix measurement, on-wafer measurement, D-band, time domain gating, calibration, power divider, SIW.

I. INTRODUCTION

Three-port networks, such as power dividers and baluns, are important building blocks in many wireless communication frontends. As operating frequencies push beyond 100 GHz and into the sub-THz regime for applications such as NextG wireless, accurate on-wafer characterization of these devices becomes critical. The classic Tippet method [1] reconstructs three-port S parameters from sequential two-port network measurements with the third port terminated, but requires the ability to directly access each port and measure several port pairings (i.e. port switching). However, this is challenging for sub-THz on-wafer probe systems, for which the port orientations are fixed and with large, inflexible frequency extenders and probes. These mechanical limitations make it difficult to connect multi-port devices directly to the vector network analyzer (VNA). To avoid port switching, Davidovitz proposed reconstructing the three-port matrix using measurements at only two ports, provided three known terminations are applied to the remaining port [2]; later work extended the concept to reciprocal N-ports [3]. However, the optimal selection of the termination impedances remains underexplored.

In this work, a D-band on-wafer SiC substrate integrated waveguide (SIW)-based power divider is characterized by using a two-port VNA, following the outline suggested by the Davidovitz technique. A novel quantitative termination-evaluation strategy is proposed for the three-port S-parameter reconstruction. Since the terminations are applied at the end of a wafer probe that is electrically large, time-domain gating (TDG) is applied to the reconstructed S parameters, yielding reliable three-port characteristics and demonstrating practicality for sub-THz on-wafer measurements.

II. TERMINATION TRIPLET CRITERION

Consider a reciprocal three-port network with scattering matrix S . Port 3 is not directly measured; instead, it is terminated by known loads with reflection coefficients Γ_i , for $i = 1, \dots, M$, where $M \geq 3$.

For an unordered termination triplet $\{a, b, c\}$ and chain $\ell \in \{11, 12, 22\}$, a candidate $S_{33}^{\{a,b,c\},\ell}$ is first computed [2]. Given this candidate set of terminations at frequency k , we define

$$\xi_i^{\{a,b,c\},\ell}(k) = \frac{\Gamma_i(k)}{1 - S_{33}^{\{a,b,c\},\ell}(k)\Gamma_i(k)}. \quad (1)$$

For each chain ℓ , the measurement model is, in the error-free case, the complex-affine relation

$$y_{\ell,i}(k) = S_{\ell}(k) + T_{\ell}(k)\xi_i^{\{a,b,c\},\ell}(k), \quad (2)$$

where $y_{\ell,i}$ is the measured two-port S parameters with load i ; under reciprocity becomes (frequency dependence suppressed for clarity):

$$T_{11} = S_{13}^2, T_{12} = S_{13}S_{23}, T_{22} = S_{23}^2.$$

We can then stack the data as

$$\mathbf{y}_{\ell} = [y_{\ell,1}(k), \dots, y_{\ell,M}(k)]^T, \\ \boldsymbol{\xi}^{\{a,b,c\},\ell} = [\xi_1^{\{a,b,c\},\ell}(k), \dots, \xi_M^{\{a,b,c\},\ell}(k)]^T,$$

and form a design matrix \mathbf{X} used for the least-square regression as

$$\mathbf{X} = [\mathbf{1}_M, \boldsymbol{\xi}^{\{a,b,c\},\ell}],$$

where $\mathbf{1}_M$ is the $M \times 1$ all-ones vector. Then the complex least-square estimate of the S-parameter matrix is

$$\boldsymbol{\theta}^{\{a,b,c\},\ell} = \begin{bmatrix} \hat{S}^{\{a,b,c\},\ell} \\ \hat{T}^{\{a,b,c\},\ell} \end{bmatrix} = (\mathbf{X}^H \mathbf{X})^{-1} \mathbf{X}^H \mathbf{y}_{\ell}, \quad (3)$$

where the hat notation (e.g., \hat{S} and \hat{T}) denotes the least-square estimates of the corresponding parameters (e.g., S and T), and $(\mathbf{X})^H$ denotes the conjugate transpose of \mathbf{X} . We can then define the per-frequency root-mean-square (RMS) residual as

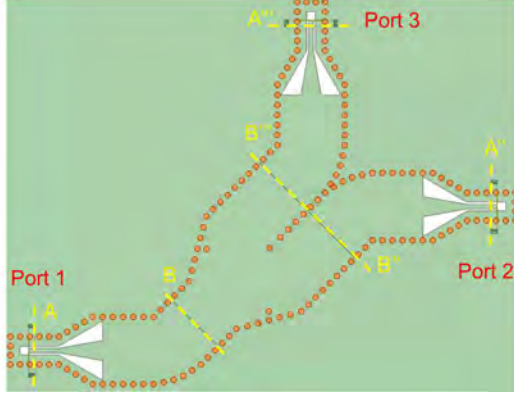


Fig. 1. Top view of the D-band SIW power divider layout.

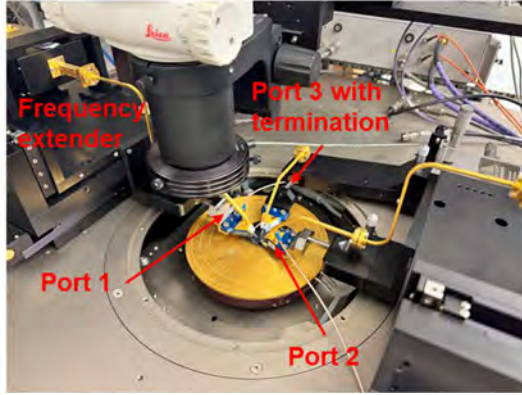


Fig. 2. Photograph of the experimental setup for on-wafer S-parameter measurement.

$$RMS^{\{a,b,c\},\ell}(k) = \sqrt{\frac{1}{M} \sum_{i=1}^M |e_i^{\{a,b,c\},\ell}(k)|^2}, \quad (4)$$

where

$$e_{\ell,i}(k) = y_{\ell,i}(k) - \left(\hat{S}^{\{a,b,c\},\ell}(k) + \hat{T}^{\{a,b,c\},\ell} \xi_i^{\{a,b,c\},\ell}(k) \right).$$

This can then be generalized to define the average score across the band as:

$$RMSE^{\{a,b,c\},\ell} = \sqrt{\frac{1}{N} \sum_{k=1}^N (RMS^{\{a,b,c\},\ell}(k))^2}, \quad (5)$$

where N is the number of frequency points. Among all unordered triplets and the three chains, the combination minimizing $RMSE^{\{a,b,c\},\ell}$ is selected for reconstruction.

III. EXPERIMENT

To validate the proposed quantitative termination evaluation strategy, the power divider (Fig. 1) was characterized using the experimental setup shown in Fig. 2, which consists of a

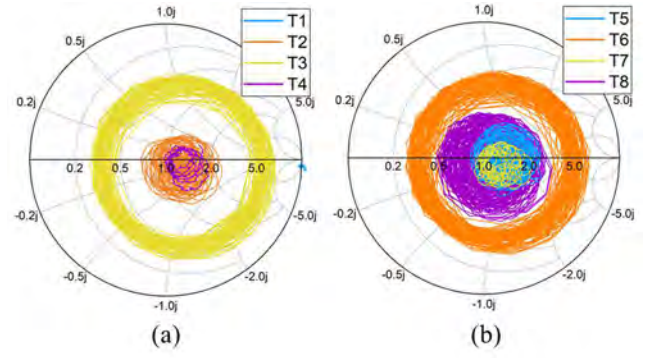


Fig. 3. Reflection coefficients 110-170 GHz of port-3 terminations referenced to the probe-tip plane: (a) T1-T4; (b) T5-T8.

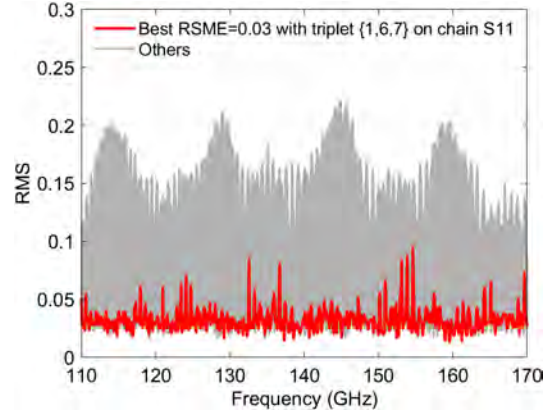


Fig. 4. Per-frequency RMS residual vs. frequency for all 168 unordered triplet-chain candidates. The red curve marks the best candidate of triplet {1,6,7} on chain S_{11} with the minimum average RMSE of 0.03, and the gray curves denote other candidates.

Keysight E8361C VNA equipped with two Virginia Diodes D-band WR6.5-VNAX frequency extenders and a pair of Form Factor i170-T-GSG-50 μ m probes. Eight sets of two-port S parameters of the divider are measured at ports 1 and 2, while port 3 is terminated with eight different loads. While only three distinct terminations are required for three-port S parameter reconstruction, eight were used in this study to compare different termination triplets and chains under the proposed evaluation method. The termination set included an unprobed (open) condition and configurations formed by mating an i170-T-GSG-50 μ m probe to a WR-6.5 waveguide section and a calibration standard, used either individually or in combination:

- 1) unprobed (T1),
- 2) probe + open (T2),
- 3) probe + short (T3),
- 4) probe + match (T4),
- 5) probe + 2-inch section + open (T5),
- 6) probe + 2-inch section + short (T6),
- 7) probe + 2-inch section + match (T7),
- 8) probe + 2-inch section + 3dB-attenuator + short (T8).

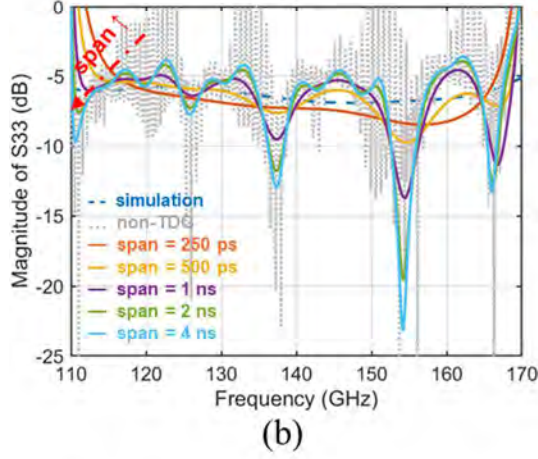
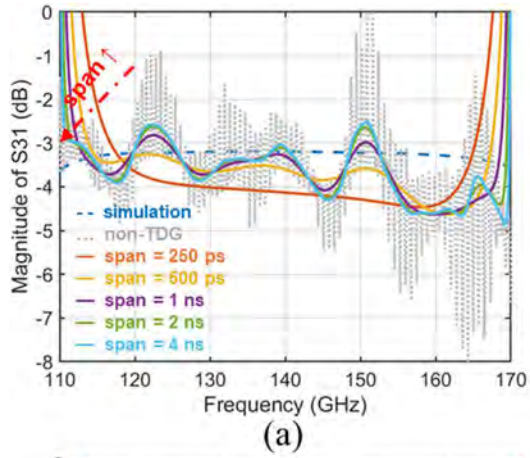


Fig. 5. Comparison of the simulated, non-TDG processed, and TDG-processed (a) S_{31} , and (b) S_{33} of the D-band SIW power divider. TDG spans are 250 ps, 500 ps, 1 ns, 2 ns, and 4 ns.

The reflection coefficient (Fig. 3) presented by each port-3 termination was characterized by measuring the reflection of the probe/termination combination through an on-wafer thru, and subsequently de-embedded to the probe tip reference plane.

Following the proposed methodology, the $RMSE^{\{a,b,c\},\ell}$ was evaluated for all termination triplets and chains (Fig. 4). The optimal candidate is triplet $\{1,6,7\}$ on chain S_{11} , yielding a minimum across-frequency $RMSE$ of 0.03 for three-port S-parameter matrix reconstruction. After the reconstruction, the grounded coplanar waveguide (GCPW) to SIW launches of the divider are de-embedded with thru-reflect-line (TRL) calibration [4], which moves the reference plane from A to B as shown in Fig. 1. The on-wafer TRL calibration standards include a thru, a short, and a 160- μm line. Furthermore, the TDG technique [5] was applied with different gate spans to suppress unwanted reflections arising from the electrically large terminations.

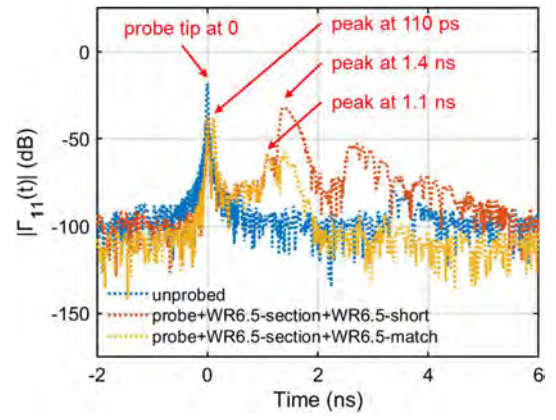


Fig. 6. Time-domain magnitude of the reflection coefficient for the selected termination triplet: T1, T6 and T7.

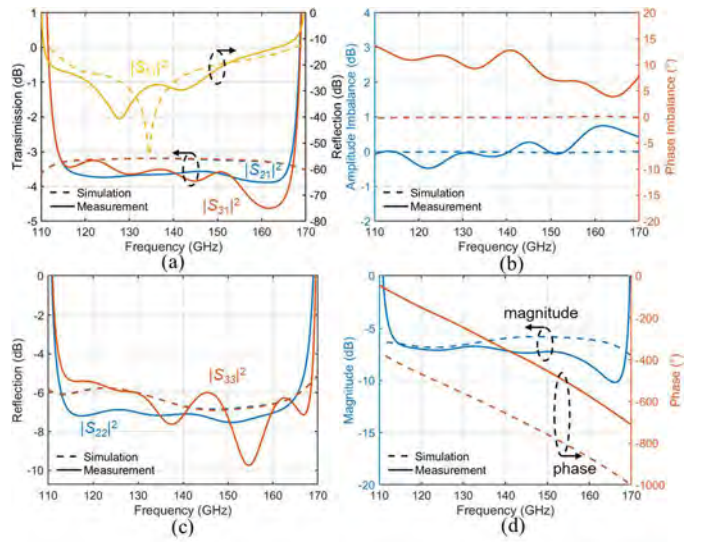


Fig. 7. Comparison of the simulated and TDG-processed (a) S_{21} , S_{31} , and S_{11} , (b) amplitude and phase imbalance, (c) S_{22} and S_{33} , and (d) S_{32} of the D-band SIW power divider. The TDG span is 500 ps.

IV. RESULTS AND DISCUSSION

Fig. 5 compares the simulated, reconstructed, and TDG-processed reconstructed S_{31} and S_{33} of the divider. Without TDG, the reconstructed S parameters exhibit pronounced frequency-domain ripples that are consistent with reflections external to the device under test (DUT) — arising from discontinuities (e.g., at the probe-WR-6.5 and WR-6.5-WR-6.5 interfaces) within the electrically large terminations. TDG suppresses these unwanted reflections in the time domain and markedly smooths the S parameters. A sweep of the TDG span shows the expected trade-off: narrower spans more aggressively reject distant echoes and thus better suppress ripples, but they also truncate time-domain energy and

introduce band-edge distortions after inverse transformation—an unavoidable manifestation of spectral leakage [6]. As shown in the time-domain reflection responses of the selected terminations (Fig. 6), the dominant reflections introduced by the probe and waveguide interfaces appear only after ~ 500 ps. Balancing ripple suppression against distortion, we adopt a 500-ps gate and restrict quantitative evaluation to 115–165 GHz to avoid over-interpreting edge effects.

Fig. 7 compares the TDG-processed (span = 500 ps) three-port S parameters with full-wave HFSS simulation, showing overall good agreement 115–165 GHz. As shown in Fig. 7(a), the measured insertion loss averages 3.7 ± 0.1 dB from port 1 to port 2, for an excess loss of 0.7 dB. Comparing this with 3.24 ± 0.04 dB in simulation, the ~ 0.46 -dB additional loss can be attributed to higher SIW losses from imperfect metallization, especially in the vias. The measured input return loss averages 25 ± 7 dB. Furthermore, Fig. 7(b) demonstrates a balanced power split has been achieved in experiment, with amplitude imbalance 0.05 ± 0.34 dB and phase imbalance $9 \pm 3^\circ$. In Fig. 7(c), the output return loss is 7.1 ± 0.2 dB at port 2 and 7 ± 1 dB at port 3. The isolation is 7.4 ± 0.7 dB, as shown in Fig. 7(d); due to the lack of on-chip resistor, this design is not expected to provide high isolation.

V. CONCLUSION

This work demonstrated on-wafer three-port S-parameter characterization of a D-band SiC SIW power divider using a two-port VNA, with the third port sequentially terminated by three known standards. The three-port S matrix is constructed under the proposed quantitative termination evaluation strategy, followed with TRL de-embedding and TDG processing. The resulting three-port S parameters exhibit reasonable agreement with full-wave simulation, achieving low excess loss of 0.7 ± 0.1 dB and an input return loss of 25 ± 7 dB across the D band.

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