High-Current Tunneling FETs with (1$\bar{1}$ 0) Orientation and a Channel Heterojunction

Pengyu Long, Jun Z. Huang, Michael Povolotskyi,
Gerhard Klimeck, *Fellow, IEEE*, and Mark. J.W. Rodwell, *Fellow, IEEE*[1]

***Abstract*— We propose InAs/GaSb ultra-thin-body (UTB) tunneling field-effect transistors (TFETs) using confinement in the (1$\bar{1}$ 0) plane and transport in the [110] direction to increase the tunneling probability by reducing the tunnel barrier energy and hole effective mass. To reduce the OFF-state leakage current we add an InAs/$In_{1-n}Al_{xn}As_{1-n}Sb_n$ heterojunction to the channel which increases the valence band barrier. The heterojunction also increases the tunneling probability and ON-current by reducing the tunneling distance through the PN junction and introducing a resonant state. A fully atomistic Non-Equilibrium Green Function quantum transport approach in NEMO5 is used to explore the design space. While choosing 10^{-3} A/m OFF current (I_{OFF}) and a 0.3V power supply, we simulate 270A/m ON-current (I_{ON}) for a 30nm gate length and 170A/m for a 15nm gate length (L_g), while a conventional 15nm L_g GaSb/InAs TFET under (001) confinement shows only 24A/m I_{ON}.**

***Index Terms*—Tunnel FETs, Crystal orientation, Band structure engineering, Resonant tunneling.**

I. Introduction

Future VLSI performance is constrained by power dissipation [1]. Low switching power calls for a low supply voltage, yet decreased standby power calls for either increased voltages or reduced transistor subthreshold swing (*S.S.*). In conventional MOSFETs, the *S.S.* is limited to 60mV/dec by thermal injection [1]. Though tunnel FETs (TFETs) [2,3,4] can obtain smaller *S.S.,* their ON current (I_{ON}) is limited by the PN junction tunneling probability [3], which is determined by the carrier effective mass and tunneling distance. In nanoscale TFETs confinement quantizes subbands and therefore increases the barrier energy and non-parabolic dispersions increase the carrier effective masses; both effects result in a decreased tunneling probability and reduced I_{ON}. The use of InAs/GaSb PN tunnel barriers reduces the tunneling barrier energy and tunneling distance, however at the desired layer thicknesses of a few nm, strong confinement and non-parabolic effects still reduce I_{ON} significantly. Alternative methods are needed to further increase I_{ON}.

Here we propose the concept to *increase* the confinement effective mass (to lower the confinement energy) and to *decrease* the transport effective mass (to increase the tunneling current). This can be achieved in the InAs material system by choosing the (1$\bar{1}$ 0) plane for confinement and the [110] direction for transport. We also introduce an InAs/$In_{1-n}Al_nAs_{1-n}Sb_n$ heterojunction into the channel, and therefore resonantly enhance the tunneling probability in the ON-state and reduce the OFF-state source-drain tunneling leakage current.

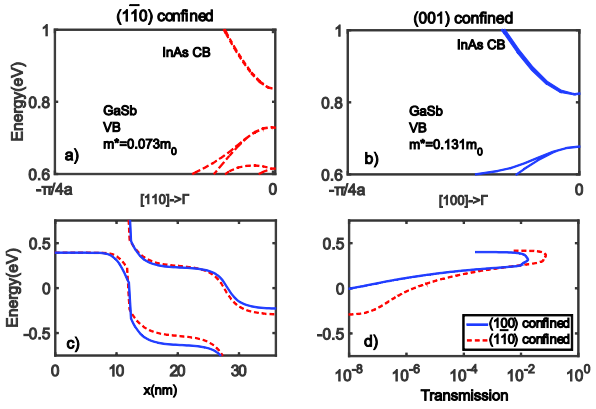

Figure 1: Conduction band structure of InAs and valence band structure of GaSb for a) (1$\bar{1}$ 0) confined, and b) (001) confined UTBs. c) Band diagram under ON-state bias and d) transmission probability of (1$\bar{1}$ 0) confined and (001) confined UTB GaSb/InAs TFETs. The channels are 2nm thick, and L_g=15 nm

TABLE I

PARAMETERS FOR GASB/INAS TUNNELING FETS

t_{ox}	2.56 nm	N_S	$5\cdot10^{19}$ cm^{-3}
t_{ch}	2 nm	N_D	$2\cdot10^{19}$ cm^{-3}
L_g	30 nm, 15 nm	$\varepsilon_{r,ox}$	9

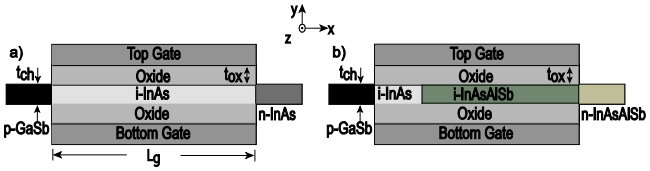

Figure 2: Cross-section of a) a conventional GaSb/InAs TFET. b) Newly design heterostructure GaSb/InAs TFET with an InAs/ $In_{1-n}Al_nAs_{1-n}Sb_n$ heterojunction in the channel.

II. Confinement and Transport Directions

III-V materials have strongly anisotropic heavy-hole bands [5,6], hence 2-D hole subband structure is a strong function [5,6,7] of the confinement plane. (1$\bar{1}$ 0) confinement provides subbands with low effective mass [8], particularly given [110]

P. Long, J. Z. Huang, M. Povolotskyi, and G. Klimeck are with the Network for Computational Nanotechnology and Birck Nanotechnology Center, Purdue University, West Lafayette, IN 47907 USA (e-mail: davidlong180@gmail.com).

M. J. W. Rodwell is with the Department of Electrical and Computer Engineering, University of California, Santa Barbara, CA 93106-9560 USA.

transport [9,10]. For a t_{ch}=2nm thick channel, the hole effective mass reduces from 0.132m_0 given (001) confinement and [100] transport, or 0.19m_0 given [110] transport, to 0.073m_0 given (1$\bar{1}$ 0) confinement and [110] transport. Further, because the heavy hole mass is larger in <110> than in <100>, the heavy hole subband energy shifts more slowly under (1 $\bar{1}$ 0) confinement than under (100). Compared to (100) confinement, at 2nm t_{ch}, (1$\bar{1}$ 0)-confined TFETs have lower hole effective mass and a smaller tunnel barrier energy (0.11eV vs. 0.15eV) between the GaSb source valence band and the InAs channel conduction band (Fig. 1a,b). The tunnel barrier is consequently thinner (Fig. 1c) and the tunneling probability higher (Fig. 1d).

The designs are based on a p-GaSb/n-InAs double-gate TFET (Fig. 2a). The gate oxide thickness is labeled t_{ox} and dielectric constant ε_r. The gate length is L_g, and source and drain doping densities are labeled N_S and N_D. The channel width extends in the z direction (perpendicular to the page). Table 1 lists the various design parameters. For (001)-confined TFETs, the transport direction is [100], and the GaSb/InAs heterointerface is InSb-like. For (1$\bar{1}$ 0)-confined TFETs, the transport direction is [110]. The channel is 2nm thick; at 15nm L_g, thicker channels suffer large source-drain tunneling leakage current. III-V MOSFETs with T_{ch}=2.5nm have been reported [11, 12].

Devices are simulated using the atomistic nanoelectronic modeling tool NEMO5 [13], which solves self-consistently the Poisson equation and the open boundary Schrödinger equation (quantum transmitting boundary method [14,15]), using the 300K tight binding parameters of [16,17]; these give, in bulk, a 0.197 eV offset between the GaSb valence band and the InAs conduction band [18]. The InAlAsSb parameters are linearly interpolated using the virtual crystal approximation and are benchmarked against [19]. We integrate over the 1D Brillouin zone using a high order Gauss quadrature with 20 points. The simulations do not model carrier scattering. In [20,21,22], it is shown that phonon scattering slightly reduces TFET I_{on}, but does not significantly increase I_{off} . In the on-state, if carrier scattering is strong, the degree of resonant enhancement of the transmission will be decreased, and will degrade I_{on}. Trap-assisted tunneling and Shockley-Read-Hall thermal generation may also increase I_{off} [23,24,25,26]. Increasing the alloy fraction n within the $In_{1-n}Al_nAs_{1-n}Sb_n$ channel will increase the channel bandgap and hence reduce thermal generation leakage currents.

Figure 1d demonstrates that in the energy range between the GaSb valence band and InAs conduction band, the TFET has a higher transmission probability with (1$\bar{1}$ 0) compared to (001) confinement. At 30nm L_g, I_{ON} increases from 30A/m to 80A/m (V_{DD}=0.3V, I_{OFF}=10^{-3}A/m) comparing to a (001) confined TFET. However, undesired source-drain transmission at energies below the InAs conduction band edge is *increased* in the (1$\bar{1}$ 0)-confined case (Fig. 1d) because InAs then has a smaller quantized bandgap (Fig. 1c) and smaller hole effective mass. The two-band S/D tunneling probability increases, and, at 15nm L_g, the *S.S.* is degraded and, at fixed I_{OFF}, I_{ON} reduced.

III. Channel Heterojunction

The introduction of an $InAs/In_{1-x}Al_xAs_{1-x}Sb_x$ channel heterojunction (Fig. 2b) can improve both ON- and OFF-state performance, as reported in [27] and [28].. In the OFF-state, the heterojunction increases the valence-band barrier at the channel-source interface. This reduces the (two-band) S/D tunneling probability (Fig. 3a) in part because, under off-state bias (Fig. 3b), the energy separation between the InAs valence band and S/D tunneling evanescent states is increased, and in part because $In_{1-n}Al_nAs_{1-n}Sb_n$ has slightly larger electron effective mass (0.067m_0) than InAs (0.052m_0). The width of the InAs well is adjusted so that the single resonant state is aligned with InAlAsSb conduction band; in the InAs layer, there are no states at energies below the InAlAsSb conduction band. The lower edge of the transmission characteristics (Fig. 3a) becomes sharper, resulting in a steeper *S.S.*, as will be seen subsequently. InAs is retained at the PN junction to maintain a small tunnel barrier energy for high I_{ON}.

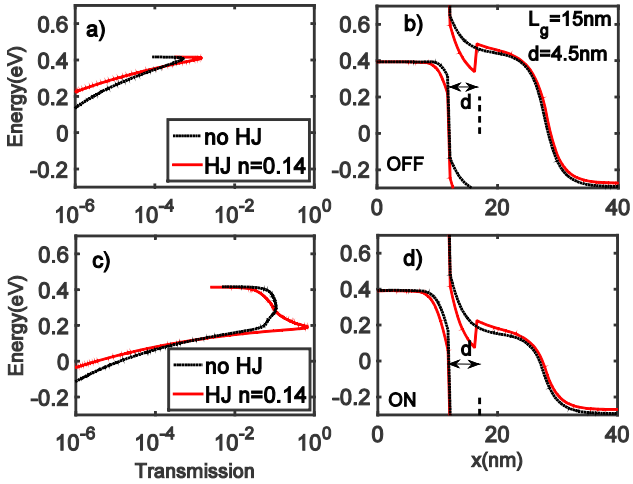

Figure 3: Off-state transmission probability a) and band diagram b) of (1$\bar{1}$ 0)-confined GaSb/InAs TFETs with and without an $InAs/In_{1-n}Al_nAs_{1-n}Sb_n$ channel heterojunction. The transmission probability c) and band diagram d) are also shown in the ON state. x is the alloy fraction.

Under ON-state bias (Fig. 3d), i.e. with the channel conduction band ~0.2eV below the source valence band, inserting the channel heterojunction increases the field in the PN tunnel barrier, reducing the PN junction tunneling distance hence increasing the tunneling probability (Fig. 3c). Inserting the channel heterojunction also introduces a resonant state in the InAs layer between the PN junction and the channel heterojunction (Fig. 4b). The tunneling probability is further increased by adjusting the $In_{1-n}Al_nAs_{1-n}Sb_n$ alloy fraction to align the resonant state energy to the channel conduction-band energy (Fig. 3c). This further improves I_{ON}.

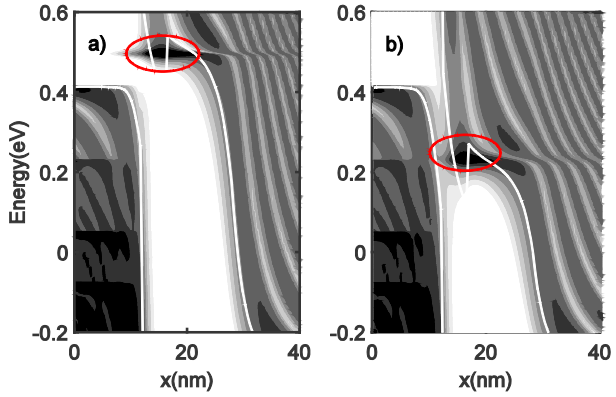

Figure 4: Local density of states in the a) OFF state and b) ON state of a GaSb/InAs TFET with an InAs/$In_{1-n}Al_nAs_{1-n}Sb_n$ (n=0.14) channel heterojunction. The circled area indicates the resonant state.

To investigate the effect of the channel heterojunction on I_{ON}, independent of its effect on S/D tunneling, we first consider the case of 30nm L_g. We simulate (Fig. 5b) a series of designs with varying InAs channel length d, while varying the $In_{1-n}Al_nAs_{1-n}Sb_n$ alloy fraction x such that the lowest resonant state in the InAs layer always lies immediately above the $In_{1-n}Al_nAs_{1-n}Sb_n$ conduction band.

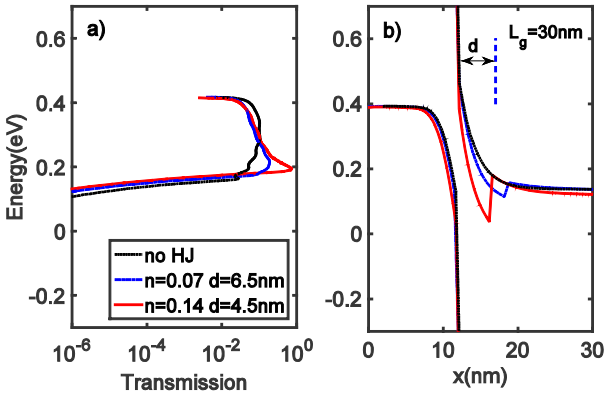

Figure 5. a) Transmission probability and b) band diagram of the GaSb/InAs tunneling junction for different InAs/$In_{1-n}Al_nAs_{1-n}Sb_n$ heterojunctions. In all designs, the resonant state energy lies immediately above the $In_{1-n}Al_nAs_{1-n}Sb_n$ conduction band. The TFETs have (1$\bar{1}$ 0) confinement.

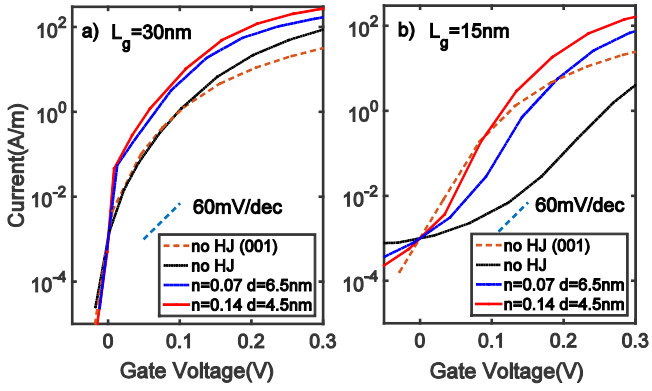

Figure 6: Transfer characteristics of a) 30nm L_g and b) 15nm L_g (1$\bar{1}$ 0)-confined TFETs for different $In_{1-n}Al_nAs_{1-n}Sb_n$ heterojunction band profiles. Results are compared to (1$\bar{1}$ 0)- and (001)-confined TFETs with no channel heterojunction.

As the InAs layer is progressively thinned and the alloy fraction n simultaneously increased, the InAs/$In_{1-n}Al_nAs_{1-n}Sb_n$ conduction band offset increases, and the energy separation between the InAs resonant state (aligned with the $In_{1-n}Al_nAs_{1-n}Sb_n$ conduction band) and the InAs conduction band increases (Fig. 5(b)). The PN junction tunneling distance therefore progressively decreases (Fig. 5b), progressively increasing I_{ON} (Fig. 6a). With V_{DD}=0.3V and I_{OFF}=10^{-3}A/m, and with (1$\bar{1}$ 0) confinement, I_{ON} increases from 80A/m (n=0) to 270A/m (n=0.14, d=4.5nm).

At 15nm L_g, S/D tunneling is larger, and the InAs/$In_{1-n}Al_nAs_{1-n}Sb_n$ heterojunction provides a greater improvement in the ON/OFF current ratio. With V_{DD}=0.3V and I_{OFF} =10^{-3}A/m, and with (1$\bar{1}$ 0) confinement, as the AlSb mole fraction n increases, I_{ON} increases from 5A/m (n=0) to 170A/m (n=0.14, d=4.5nm). The (001)-confined TFET shows 24A/m I_{ON}

A similar P-channel TFET design would use an N-InAs source, a channel containing a GaSb/AlGaSb heterojunction, a P+ AlGaSb drain, (1$\bar{1}$ 0) confinement, and [110] transport

IV. Summary

It is found that using the (1$\bar{1}$ 0) confinement plane and the [110] transport direction improves I_{ON} compared to (001)-confined TFETs. Introducing an InAs/$In_{1-n}Al_nAs_{1-n}Sb_n$ channel heterojunction reduces the S/D tunneling and improves the *S.S.* Further, the channel heterojunction greatly increases I_{ON}, both by decreasing the tunneling distance and by introducing a resonant state. Within this design space a 15nm gate length TFET with 170A/m ON current can be obtained.

V. Acknowledgment

The use of nanoHUB.org computational resources operated by the Network for Computational Nanotechnology funded by the US National Science Foundation under Grant Nos. EEC-0228390, EEC-1227110, EEC-0634750, OCI-0438246, OCI-0832623 and OCI-0721680 is gratefully acknowledged. This material is based upon work supported by the National Science Foundation under Grant Number (1125017). NEMO5 developments were critically supported by an NSF Peta-Apps award OCI-0749140 and by Intel Corp.

REFERENCES

[1] T. N. Theis and P. M. Solomon, "In quest of the "Next Switch": Prospects for greatly reduced power dissipation in a successor to the silicon field-effect transistor," Proceedings of the IEEE, vol.98, no.12, pp.2005-2014, Dec. 2010. DOI: 10.1109/JPROC.2010.2066531

[2] Q. Zhang, W. Zhao, and A. Seabaugh, "Low-subthreshold-swing tunnel transistors," IEEE Electron Device Lett., vol.27, no.4, pp.297-300, April 2006. DOI: 10.1109/LED.2006.871855

[3] S. O. Koswatta, M. S. Lundstrom, and D. E. Nikonov, "Performance comparison between pin tunneling transistors and conventional MOSFETs." IEEE Trans. Electron Devices, vol.56, no.3, pp.456-465, March 2009. DOI: 10.1109/TED.2008.2011934

[4] G. Dewey, B. Chu-Kung, J. Boardman, J.M. Fastenau, J. Kavalieros, R. Kotlyar, W.K. Liu, D. Lubyshev, M. Metz, N. Mukherjee, P. Oakey, R. Pillarisetty, M. Radosavljevic, H.W. Then, and R. Chau, "Fabrication, characterization, and physics of III–V heterojunction tunneling field

effect transistors (H-TFET) for steep sub-threshold swing," Proc. IEEE Int. Electron Devices Meeting, Dec. 2011, pp. 33.6.1-33.6.4, 5-7. DOI: 10.1109/IEDM.2011.6131666

[5] G. Klimeck, R.C. Bowen, T.B. Boykin, "Strong wavevector dependence of hole transport in heterostructures", Superlattices And Microstructures, Vol. 29 No. 3 pp. 187-216, March 2001. DOI: 10.1006/spmi.2000.0973

[6] N. Neophyto, A. Paul, G. Klimeck, "Bandstructure Effects in Silicon Nanowire Hole Transport", IEEE Trans. Nanotechnology, Vol. 7, No. 6,pp. 710-719, Nov 2008. DOI: 10.1109/TNANO.2008.2006272

[7] J. Z. Huang, L. Zhang, P. Long, M. Povolotskyi, and G. Klimeck, "Quantum transport simulation of III-V TFETs with reduced-order k.p method," arXiv preprint arXiv:1511.02516, 2015.

[8] N. Neophytou and G. Klimeck, "Design space for low sensitivity to size variations in [110] PMOS nanowire devices: The implications of anisotropy in the quantization mass," Nano Lett., vol. 9, no. 2, pp. 623-630, 2009. DOI: 10.1021/nl802893m

[9] J. Wang, P. M. Solomon, and M. Lundstrom. "A general approach for the performance assessment of nanoscale silicon FETs,", *IEEE Transactions on Electron Devices*, 51.9 (2004): 1366-1370. DOI: 10.1109/TED.2004.833962

[10] N. Neophytou, G. Klimeck, and H. Kosina, "Subband engineering for p-type silicon ultra-thin layers for increased carrier velocities: An atomistic analysis," *Journal of Applied Physics* 109.5 (2011): 053721. DOI: 10.1063/1.3556435

[11] S. Lee, V. Chobpattana , C.-Y. Huang , B. J. Thibeault, W. Mitchell, S. Stemmer, A. C. Gossard, and M. J. W. Rodwell, "Record I_{on} (0.50 mA/μm at V_{DD}= 0.5 V and I_{off}= 100 nA/μm) 25 nm-gate-length ZrO_2/InAs/InAlAs MOSFETs." Digest of Technical Papers, 2014 Symposium on. VLSI Technology, IEEE, DOI: 10.1109/VLSIT.2014.6894363

[12] C.-Y. Huang, P. Choudhary, S. Lee, S. Kraemer, V. Chobpattana, B. Thibeault, W. Mitchell, S. Stemmer, A. Gossard, M. Rodwell, "12 nm-gate-length ultrathin-body InGaAs/InAs MOSFETs with $8.3 \cdot 10^5$ I_{ON}/I_{OFF}.", 73rd Annual. IEEE Device Research Conference (DRC), 2015. DOI: 10.1109/DRC.2015.7175669

[13] J.E. Fonseca,. T. Kubis, M. Povolotskyi, B. Novakovic, A. Ajoy, G. Hegde, H. Ilatikhameneh, Z. Jiang, P. Sengupta, Y. Tan, and G. Klimeck "Efficient and realistic device modeling from atomic detail to the nanoscale," J. Comput. Electron, vol.12, no.4, pp. 592-600, 2013. DOI: 10.1007/s10825-013-0509-0

[14] C. S. Lent and D. J. Kirkner, "The quantum transmitting boundary method," J. Appl. Phys., vol. 67., no.10, pp.6353-6359, 1990 . DOI: 10.1063/1.345156

[15] M. Luisier, A. Schenk, W. Fichtner, and G. Klimeck, "Atomistic simulation of nanowires in the sp3d5s* tight-binding formalism: From boundary conditions to strain calculations," Phys. Rev. B, vol. 74, no. 20, p. 205323. Nov 2006. DOI: 10.1103/PhysRevB.74.205323

[16] Y. P. Tan, M. Povolotskyi, T. Kubis, T.B. Boykin, and G. Klimeck, "Tight-binding analysis of Si and GaAs ultrathin bodies with subatomic wave-function resolution". *Physical Review B* 92.8 (2015): 085301. DOI: 10.1103/PhysRevB.92.085301

[17] Y. P. Tan, M. Povolotskyi, T. Kubis, Y. He, Z. Jiang, T.B. Boykin, and G. Klimeck, "Tight Binding Parameters by DFT mapping," https://nanohub.org/resources/15173.

[18] I. Vurgaftman, J. R. Meyer, and L. R. Ram-Mohan. "Band parameters for III–V compound semiconductors and their alloys." *Journal of applied physics* 89.11 (2001): 5815-5875. DOI: 10.1063/1.1368156

[19] T. H, Glisson, J. R. Hauser, M. A. Littlejohn, C. K. Williams. "Energy bandgap and lattice constant contours of III–V quaternary alloys." *Journal of Electronic Materials* 7.1 (1978): 1-16. DOI: 10.1007/BF02656016

[20] M. Luisier, and G. Klimeck, "Simulation of nanowire tunneling transistors: From the WentzelKramersBrillouin approximation to full-band phonon-assisted tunneling," J. Appl. Phys, vol. 107, no. 8, p. 084507, 2010. DOI: 10.1063/1.3386521

[21] S. O. Koswatta, S. J. Koester, and W. Haensch, "On the possibility of obtaining MOSFET-like performance and sub-60-mV/dec swing in 1-D broken-gap tunnel transistors," IEEE Trans. Electron Devices, vol. 57, no. 12, pp. 3222–3230, 2010. DOI: 10.1109/TED.2010.2079250

[22] U.E. Avci, D.H. Morrie, S. Hasan, R. Kotlyar, Raseong Kim; R. Rios, D.E. Nikonov, I. A. Young, "Energy efficiency comparison of nanowire heterojunction TFET and Si MOSFET at Lg= 13nm, including P-TFET and variation considerations." 2013 IEEE International Electron Devices Meeting, 9-11 Dec. 2013. DOI: 10.1109/IEDM.2013.6724744

[23] U. E. Avci, B. Chu-Kung, A. Agrawal, G. Dewey, V. Le, R. Rios, D. H. Morris, S. Hasan, R. Kotlyar, J. Kavalieros, I. A. Young, "Study of TFET Non-ideality Effects for Determination of Geometry and Defect Density Requirements for Sub-60mV/dec Ge TFET." 2015 IEEE International.Electron Devices Meeting (IEDM), DOI not yet available

[24] M.G. Pala, D. Esseni, "Interface Traps in InAs Nanowire Tunnel-FETs and MOSFETs—Part I: Model Description and Single Trap Analysis in Tunnel-FETs," IEEE Transactions on Electron Devices, vol.60, no.9, pp.2795-2801, Sept. 2013. DOI: 10.1109/TED.2013.2274196

[25] M.G. Pala, D. Esseni,"Interface Traps in InAs Nanowire Tunnel FETs and MOSFETs—Part II: Comparative Analysis and Trap-Induced Variability," IEEE Transactions on Electron Devices, vol.60, no.9, pp.2802-2807, Sept. 2013. DOI: 10.1109/TED.2013.2274197

[26] S. Mookerjea, D. Mohata , T. Mayer , V. Narayanan , S. Datta, "Temperature-Dependent I–V Characteristics of a Vertical $In_{0.53}Ga_{0.47}As$ Tunnel FET", IEEE Electron Device Letters, vol.31, no.6, pp.564-566. DOI: 10.1109/LED.2010.2045631

[27] K. Ganapathi and S. Salahuddin. "Heterojunction vertical band-to-band tunneling transistors for steep subthreshold swing and high on current." *Electron Device Letters, IEEE* 32.5 (2011): 689-691. DOI: 10.1109/LED.2011.2112753

[28] M.G. Pala, S. Brocard, "Exploiting Hetero-Junctions to Improve the Performance of III–V Nanowire Tunnel-FETs," IEEE Journal of the Electron Devices Society, vol.3, no.3, pp.115-121, May 2015, DOI: 10.1109/JEDS.2015.2395719