A Multiphase Switched Capacitor Power Amplifier in 130nm CMOS

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***Abstract*—This paper presents a multiphase switched-capacitor power amplifier (MP-SCPA). Cartesian combining architectures suffer reduced output power and efficiency owing to combination of out-of-phase signals. The multiphase architecture reduces the phase difference between the basis vectors that are combined, increasing the output power and efficiency compared to the Cartesian combiners. 16 equally spaced phases are produced by a phase generator with each phase's relative amplitude weighted on the bottom plate of a capacitor array and combined on a common top plate, resulting in linear amplification. The MP-SCPA delivers a peak output power and PAE of 26 dBm and 24.9%, respectively. When amplifying an LTE signal the average output power and PAE are 20.9 dBm and 15.2%, respectively while achieving <-30 dBc ACLR and 3.5 %-rms EVM.**

***Index Terms*—Class-D PA, Digital PA, EER, Multiphase PA, Polar PA, Switched-Capacitor PA, SCPA.**

I. Introduction

RF power amplifiers are the dominant energy consumer in wireless transceivers for portable electronics; hence improving their energy efficiency is critical to improving battery life in these devices. Performance in CMOS is poor due to low operating voltages of fine line devices. The relatively low operating voltage exacerbates losses in on-chip matching networks. Furthermore, CMOS transistors continue to be poor transconductors; however, scaling has improved the devices performance as a low-loss switch. It is thus desirable to utilize the transistor in this mode as part of a switching amplifier.

Switching amplifiers must be linearized in order to amplify non-constant envelope (non-CE) modulation, owing to their insensitivity to input amplitude variation. Recently digital power amplifiers (DPAs) have shown promise in amplifying non-CE signals with high linearity and efficiency. DPAs have been implemented into Doherty amplifiers [1], polar transmitters [2], [3] and most recently Cartesian/quadrature transmitters [4]–[6]. The Cartesian variants of the DPA, including the quadrature SCPA (Q-SCPA), are complete front-end transmitters, acting as a digital-to-analog converter, a frequency upconverter and amplifier all-in-one [2]–[4], [6].

The polar techniques translate a signal from the Cartesian coordinate system (e.g., $I(t)$, $Q(t)$) to a polar coordinate system (e.g., $A(t)$, $\phi(t)$) using non-linear coordinate transformations.

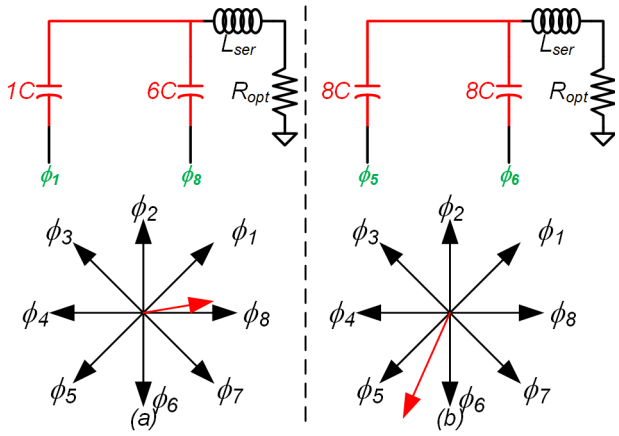


Fig. 1. Example operation of a MP-SCPA with 8 phases SCPA.

Due to the nonlinearity, the transformed polar vectors require larger bandwidth for linear recombination. Furthermore, $A(t)$ and $\phi(t)$ propagate at different frequencies and hence experience different group delays, requiring synchronization to ensure linearity. The quadrature DPA variants do not suffer such bandwidth expansion or requirements for stringent synchronization; however these transmitters suffer from a -3-dB loss upon recombination; thus, the drain efficiencies of the quadrature architectures are significantly lower than those of the polar variants. It is noted that the global efficiency may still be better for the quadrature DPAs when compared to polar DPAs, as they do not require high power phase modulators and synchronization circuitry.

Shown in Fig. 1 is an alternative to the quadrature DPA that expands the number of basis phase vectors that are available for recombination. In the quadrature architecture, there are only 4 basis vectors (e.g., $\pm I$ and $\pm Q$), all separated from one another by 90°. The large phase difference between the signals is the cause of the -3-dB loss. By adding additional phases the separation between the basis vectors is reduced, resulting in increased constructive summation between the vectors and hence reduced loss.

In this paper we present a capacitor-combined multiphase SCPA (MP-SCPA) for non-constant envelope amplification that implements the system depicted in Fig. 1. Similar to the Q-SCPA, the basis phase vectors (e.g., ϕ_1-ϕ_8,

Fig. 1) propagate with the same frequency and bandwidth; hence, timing alignment is not as critical as in a polar/EER based DPA. Therefore, no synchronization between signal paths is necessary, nor is a wideband phase modulator.

This paper is organized as follows. In section II, theory of operation of the MP-SCPA is presented, followed by design details in Section III. Measurement results are presented in Section IV. Finally, conclusions and future work are presented in Section V.

II. Theory of Operation for a Capacitively Combined Multiphase SCPA

Switched-capacitor circuits can be used to control output voltage using a charge division by precisely controlling the ratio of capacitors on an integrated circuit. The SCPA is a class-D PA with a controllable output charge division; hence a controllable output voltage amplitude. A detailed description of the theory of operation of an SCPA can be found in Yoo, et. al. [7].

In the MP-SCPA (Fig. 2) a capacitor is divided into an array of capacitor cells, where the bottom plates of all of the capacitors are shared and the top plates are driven by a single pole switch that can be toggled between V_{DD} and V_{GND}, or held at V_{GND}. The switch is a cascoded inverter that allows for operation from a larger voltage supply to reduce losses in the output matching network. In each cell there is a logic gate to enable/disable switching, a level shifter and separate buffer chains to drive the high-side and low-side of the switch. Care is taken to match the delays of these paths so that conduction losses are minimized.

To allow operation around the complex plane, an RF clock signal is subdivided into N equally spaced output phases (ϕ_1-ϕ_N), using either a DLL or a polyphase filter. Each phase is input to a MUX tree that is controlled by clock selection logic. The clock selection logic selects the two adjacent phases (ϕ_A or ϕ_B) to the desired output phase and routes these two phases to each cell of the MP-SCPA. The multi-phase logic decoder can route either adjacent phase to each individual cell, and control whether that cell is switched on ϕ_A or ϕ_B at the RF clock rate, or held at V_{GND}, using bits b_0-b_M. This allows the amplitude and phase at the output of the MP-SCPA to be precisely controlled. By allowing the MP-SCPA cells to be fully clocked by either ϕ_A or ϕ_B, the output is higher when the output is steered towards either basis phase; leading to more efficient uses of the cells and hence higher energy efficiency.

In a multiphase architecture there is an efficiency penalty that is related to the non-overlapping regions of the clocks. The phase separation of the signals is critical, to allow for the output of arbitrary phases, but it comes at the expense of reduced output power and efficiency. It can be shown that when multiphase signals are combined the output power of the combined signal relative to the power of the input vectors, P_{rel}, is given by the following:

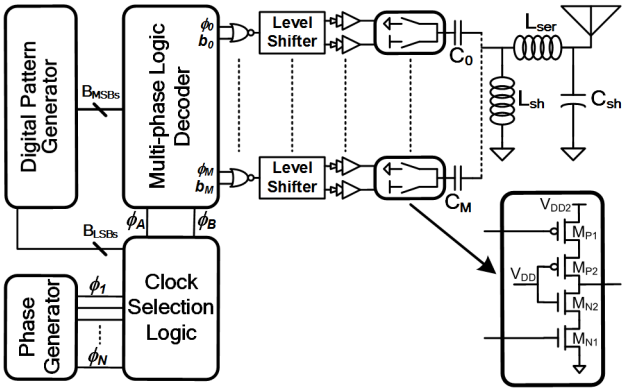


Fig. 2. Block Diagram of the proposed MP-SCPA. Note that the actual implementation is differential.

$$P_{rel} = 10\log(cos^2\frac{180}{N}). \quad (1)$$

N represents the number of phases that are available. Increasing N reduces the non-overlapping period of the clocks. For a quadrature architecture, N=4, leading to P_{rel}=-3 dB. Increasing N to eight reduces P_{rel} to -0.7 dB. N can be increased arbitrarily to reduce this power loss, at the expense of wider bandwidth; in the limit where N tends to infinity, the system would be the same as a polar implementation.

In multiphase DPA architectures, care must be taken to ensure symmetric loading in the ϕ_A and ϕ_B paths to maintain similar signal delay. This matching is less critical than that of a polar DPA, because the multiphase signals propagate at the same frequency, whereas envelope and phase signals in polar PAs propagate at significantly different frequencies; hence they experience different group delays.

III. Design of the Unit Cell of the MP-SCPA

A block diagram of the unit cascoded SCPA is shown in Fig. 2; a single-ended version is shown although the fabricated circuit is fully differential. In the proposed architecture, an off-chip phase generator creates 16 evenly distributed phase vectors (ϕ_0-ϕ_{15}) that are input to a clock selection MUX. Four LSB bits from the digital pattern generator are used to select the two adjacent phases (ϕ_A-ϕ_B) to the phase of the desired output signal. The phases, ϕ_A-ϕ_B, are distributed to every cell of a 7b capacitor array, where a 14b multiphase logic decoder can select whether to switch each capacitor cell on ϕ_A, on ϕ_B, or to ground the cell to V_{GND}. As was previously mentioned, the array can be steered entirely to either phase ϕ_A, or ϕ_B, allowing for larger output amplitude and efficiency.

The capacitor array is comprised entirely of a unary array to maximize the linearity of the MP-SCPA. The logic decoder operates in two steps. First it determines how many of the cells will be switched on ϕ_A, using a binary-to-thermometer decoder. Next it determines how many cells will be switched on ϕ_B also using a binary-to-thermometer

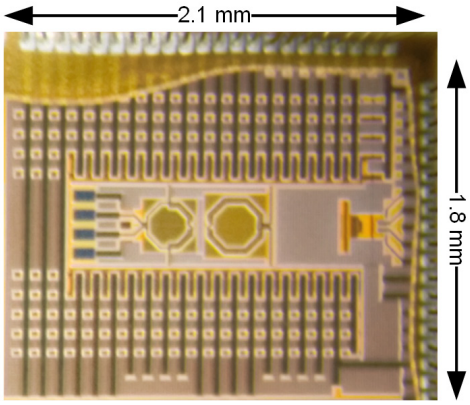


Fig. 3. Chip microphotograph of the 130 nm experimental prototype multiphase SCPA.

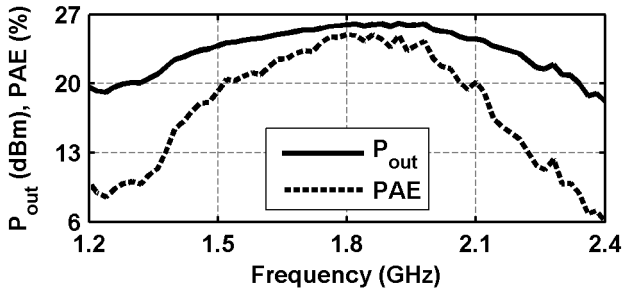
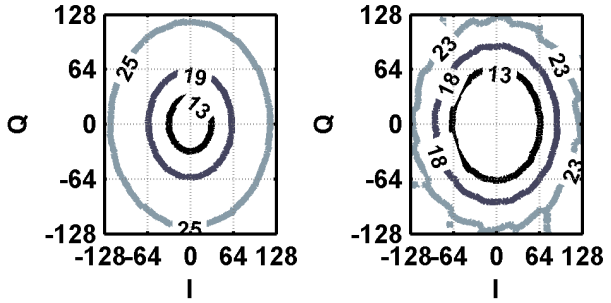


Fig. 4. Measured output power and PAE vs. frequency.

decoder. All remaining cells are connected to V_{GND}. As with other SCPA architectures, class-G can be added to enhance the efficiency for large output power backoff, though this was not implemented in this design [2].

In order to minimize losses resulting from large impedance transformation ratios, it is desirable to operate from larger voltage supplies. This is accommodated by cascoding the CMOS inverter that acts as the switch between the high supply voltage and ground. Using this arrangement and setting the gate voltage on the cascode transistors (M_{N2} and M_{P2}) to V_{DD} allows the supply voltage to be raised to twice V_{DD}, which is labelled V_{DD2}. This ensures that no terminal-terminal voltage ever exceeds V_{DD}.

The capacitor array is realized using MiM capacitors where all of the bottom-plates are shared, while the top plates are connected to the switches and subsequently the control logic. The top plates are connected in series with series resonant output matching network (L_{sh}, L_{ser} and C_{sh}) with excess reactive impedance that resonates with the sum of the unit capacitors, forming a bandpass series-resonant circuit at the design frequency. Because the total capacitance remains unchanged from the perspective of the inductor, the inductance is sized to be series resonant with the total array capacitance, regardless of the input code. The bandpass characteristic of the resonant matching circuit filters undesired harmonic content due to switching.



(a) (b)

Fig. 5. (a) Measured output power (dBm) contour and (b) Measured PAE contour.

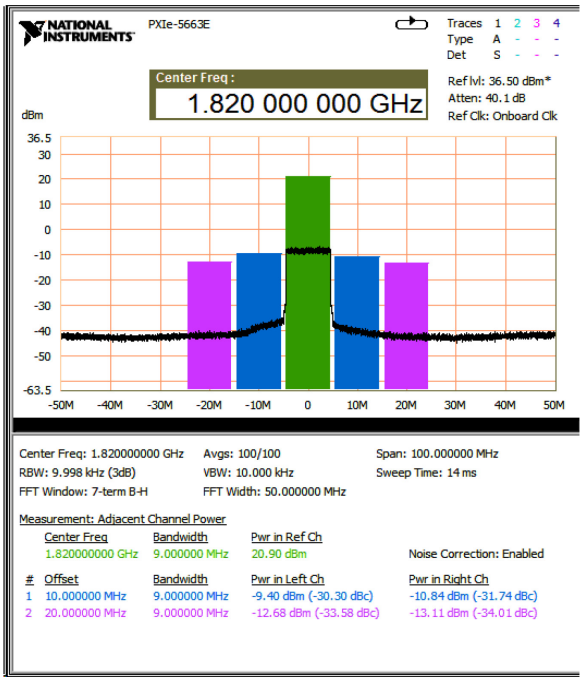


Fig. 6. Measured ACLR for a 10 MHz, 64 QAM LTE signal.

IV. Measurement Results

An experimental prototype of the capacitively combined MP-SCPA is fabricated in a 130 nm RF CMOS process with an ultra-thick top metal for high quality passive elements. A chip microphotograph of the MP-SCPA is shown in Fig. 3. The PA operates at a center frequency of 1.82 GHz with a peak output power and efficiency of 26 dBm and 24.9%, respectively, as shown in Fig. 4. Efficiency can be increased by increasing the optimum termination impedance of the amplifier, resulting in lower losses in the matching network and reduced voltage division; this also reduces output power. The -3 dB bandwidth of the PA is ≈750 MHz as determined by the loaded quality factor of the band-pass matching network. To verify the function over the code range the output power

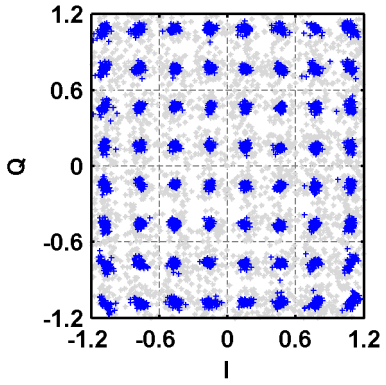


Fig. 7. Measured LTE signal constellation for a 10MHz, 64-QAM LTE signal. The blue (grey) dots are measured with (without) LUT-DPD. The measured EVM is 3.5 %-rms

TABLE I. COMPARISON TO PRIOR ART

	This Work	[4]	[3]	[6]	[5]
Process (nm)	130	28	40	65	65
Supply (V)	3	1.1	1.8	1.3	1.2/2.4
Resolution (b)	7-MP	6-IQ	13-IQ	13-IQ	7-IQ
Frequency (GHz)	1.8	0.8	2.4	2.4	2.0
Modulation	LTE	LTE	WiFi	Single Carrier	LTE
Average P_{out} (dBm)	20.9	7.0	18.8	16.9*	14.5
Average PAE (%)	15.2	29.1	17#	NA	12.2
ACLR (dBc)	-30.3	-32.4	NA	<-43	-30.7
EVM (%-rms)	3.5	NA	5.6	4.0	3.6

#Drain efficiency, *Assuming 6dB PAPR

and PAE are plotted on the complex plane for every output amplitude and phase in Fig. 5. A 2D lookup table (LUT) based digital pre-distortion (DPD) is applied. After DPD the output amplitude shows a linear response across all possible codewords and phases. The PAE has a peak value of 24 %, peaking for maxima along the basis phase vectors.

The MP-SCPAs ability to amplify signals with large PAPR is verified with a 10 MHz, 64 QAM LTE signal. The measured ACLR, is plotted in Fig. 6 and shows less than -30 dBc when outputting 20.9 dBm at 15.2% average efficiency. After the aforementioned 2D LUT (DPD) the measured EVM at this ACLR is 3.5%-rms. The signal constellation is plotted in Fig. 7. The functionality of the MP-SCPA is validated through both the static and modulated measurements.

DPD is required primarily due to excess bondwire inductance that can be replicated in simulation. Bondwires cause supply and ground bounce; packages with reduced inductance (e.g., flip-chip) do not require DPD owing to the low-loss switches and superior capacitor matching accuracy in CMOS processes.

V. CONCLUSIONS AND FUTURE WORK

An MP-SCPA that can output any phase and amplitude on the complex plane based on digitally coded multiphase inputs is demonstrated in 130nm CMOS. This PA leverages the advantages of digital PAs while not requiring the wideband modulator of polar DPAs, or having the high combining loss of a quadrature DPA. The performance of the PA is validated using static measurements and is also measured with a 10 MHz, 64-QAM LTE signal. After a 2D DPD, the ACLR is below the required -30 dBc limit and the measured EVM is 3.5 %-rms. A comparison to prior art is provided in TABLE I. Though this circuit was implemented in 130nm technology, it achieves 2 dB higher output power than its nearest competitor with similar efficiency. Output power can be traded off for efficiency by reducing output voltage division and matching network losses. It is also noted that SCPAs benefit significantly from process scaling.

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