A Switched-Capacitor Controlled Digital-Current Modulated Class-E EER Transmitter

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***Abstract*—An envelope elimination and restoration (EER) transmitter that comprises a class-E power amplifier and a digitally controlled current DAC modulator is presented. A switched capacitor DAC is designed to control an open-loop transconductor that operates as a current modulator, modulating the amplitude of the current supplied to a class-E PA. Such a topology allows for increased filtering of the quantization noise that is problematic in most digital PAs (DPA). The system measurements yield a peak output power and power added efficiency (PAE) of 22.5 dBm and 23.6%, respectively. When applying a WCDMA signal, the measured EVM is 1.32% and the adjacent channel power ratio (ACPR) is -37.9 dBc, while outputting 19.9 dBm at 14.3% PAE. For an LTE signal, the measured EVM is 3.72% and the ACLR is -30.2 dBc, while outputting 18.1 dBm at 10.6% PAE.**

Keywords—envelope elimination and restoration (EER); switched capacitor circuits; class-E power amplifier

I. INTRODUCTION

The pursuit of increased spectral efficiency in wireless communications has led to the emergence of non-constant envelope modulation techniques with high peak-to-average power ratios (e.g., orthogonal frequency-division multiplexing (OFDM), QAM, etc). In traditional transmitter architectures, a linear amplifier is needed to amplify these non-constant envelope (non-CE) modulated signals. Linear amplifiers in CMOS are inefficient when amplifying non-CE modulation because their efficiency is inversely proportional to their output power. While CMOS power amplifiers have great potential for their applications in wireless communication systems-on-chip (SoCs), it is essential that they achieve both high efficiency and linearity to justify replacing amplifiers comprised of compound semiconductor materials. Numerous techniques to improve the linearity and efficiency have been explored extensively, such as Chireix/LINC/Outphasing [1], Doherty [2], and Envelope Elimination and Restoration (EER) [3]. Among these techniques, Doherty and Chireix require large passive output matching/combining networks while achieving high efficiency. Contrarily EER combined with digital modulation does not require such networks; hence it offers reduced power loss and smaller size in integration [4].

Typically a linear supply-modulator for EER transmitters is implemented using a low-dropout regulator (LDO). This component is large and does not easily facilitate digital inputs. In this paper, we introduce a 10-bit pipelined switched-capacitor (SC) digital-to-analog converter (DAC) in combination with an open loop transconductance amplifier as the current modulator to a class-E PA, as shown in Fig. 1. Class-E operation dictates a constant voltage across the transistor when it is conducting; This condition is met because the envelope varies slowly relative to the switching frequency.

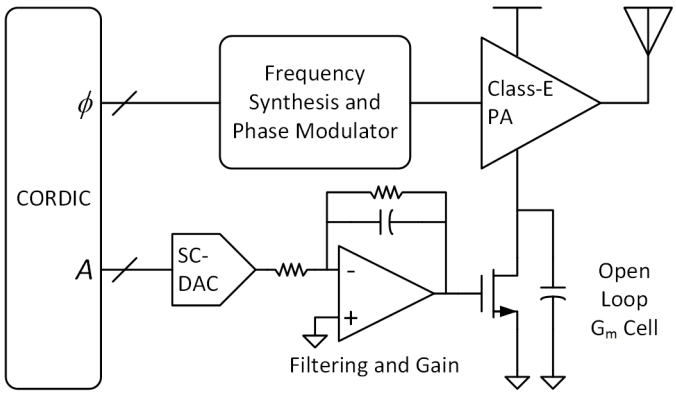

Fig. 1. Block diagram of the switched capacitor DAC modulated EER transmitter.

When compared to a current-mode DPA or an SCPA, this architecture is beneficial because the quantization noise can be suppressed by filtering at the DAC and the output matching/filtering of the PA [5], [6]; in a traditional DPA/SCPA the only filtering provided is the matching network of the PA, acting as a bandpass reconstruction filter. Size and loss in the RF matching components restrict the number of components and hence the order of the filter. By separating the RF amplifier and the DAC controlled transconductor, the quantized envelope signal can be filtered at low frequency by the reconstruction filter and at high frequency by the output matching network. Additionally, high peak efficiency is possible because the pipelined SC DAC and the open loop transconductor consume less power than an LDO, which often requires large capacitance due to necessity for compensation. An open loop transconductance amplifier controlled by an SC DAC can be easily implemented to achieve a large output current dynamic range. Hence, an SC-DAC modulated EER transmitter is a promising alternative for both the supply-modulator of an EER transmitter and for conventional current-mode DPAs.

The paper is organized as follows. In section II we introduce the circuit design details of the proposed system, including the RF PA and SC-DAC and open-loop current modulator. In section III, we present measurement results for both static and

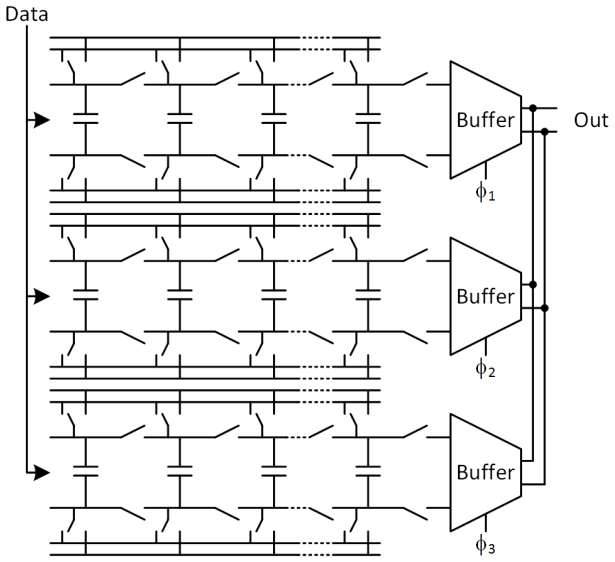

Fig. 2. Interleaved Switched Capacitor DAC

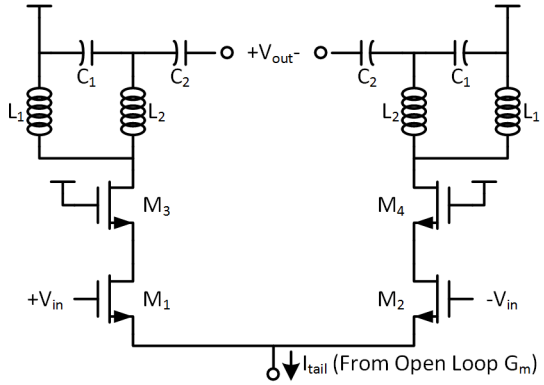

Fig. 3. Cascoded differential class-E amplifier.

dynamic characterization including digital predistortion (DPD). Finally, conclusions are presented in section IV.

II. Circuit Details

A. Pipelined Switched Capacitor DAC

In order to provide a direct interface with digital signal processing front-ends, it is convenient to fold DAC operation into the RF PA/Transmitter. Such an interface makes ease of SoC implementation possible. Traditionally high-speed DACs have been comprised of scaled current steering elements that can be controlled via digital switching. Such architectures are undesirable in this application due to the large peak current that is necessary when the PA is outputting full power. At low power this current would be steered into a dummy load and would consume significant quiescent current, lowering the overall system energy efficiency. Furthermore, dynamic non-linearity makes it difficult to correct for distortion in the output signal. To this end, a pipelined switched capacitor DAC is chosen as the digital interface. The DAC (Fig. 2) is similar to the design found in [7]. This DAC controls an open-loop transconductance cell that drives current into the common source node of a differential class-E PA. The current is proportional to the desired output amplitude and hence controls the output power of the PA. Because the transconductor operates in open-loop, the output amplitude is nonlinear with respect to the input code. Unlike closed-loop systems or current-steering DACs, this non-linearity is relatively easy to correct using DPD running in the DSP and is relatively constant with respect to output frequency [8]. Although the pipelined SC DAC is a binary-weighted DAC, it utilizes identical capacitors to minimize the cell mismatch. Compared with the more traditional current steering DAC, the pipelined SC DAC consumes less power and is glitch free [8]. A 10-bit pipelined SC DAC is implemented to provide sufficient margin for predistortion which will be discussed in section III. The EER power amplifier is designed to achieve an output power of 24 dBm into a 50 Ω load; hence, the open loop transconductance amplifier is designed with a peak output current of 250 mA. The clock frequency of the DAC is chosen by the bandwidth of the amplitude signal being processed. To achieve a wide modulation bandwidth at the output of the PA/DAC circuitry, the clock frequency of the SC DAC is derived from a divide-by-4 circuit whose input is the RF PA switching signal. The output of the transconductor supplies the current for the differential class-E PA that will now be discussed.

B. Open-loop Transconductance

To modulate the output of the PA the SC-DAC drives an op-amp that implements the reconstruction filter of the SC-DAC, as shown in Fig. 1. The reconstruction filter consists of an op-amp that is configured as an integrator with finite DC gain. This filter drives a transistor configured as an open drain buffer. The transistor is sized to minimize the drop-out voltage placed across it at the maximum output current.

C. Differential Class-E Power Amplifier

A differential class-E PA (Fig. 3) is designed similar to the PA presented in [9]. The differential topology serves two purposes; first, even order distortion terms are minimized at the output of the PA. Second, the virtual ground at the common-source node of the switching transistors allows the voltage across the transistors to remain relatively constant, which is required for class-E operation. Impedance matching is

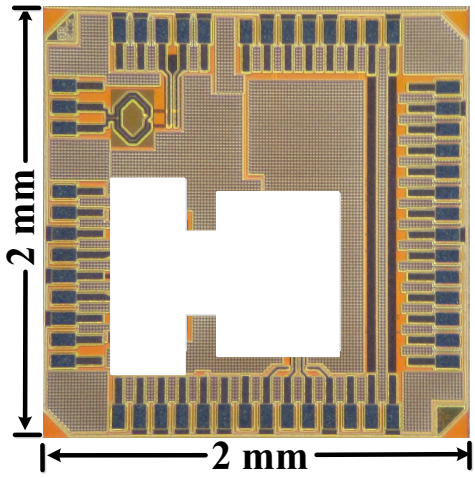

Fig. 3 Microphotograph of SC-DAC modulated EER transmitter in 130 nm CMOS

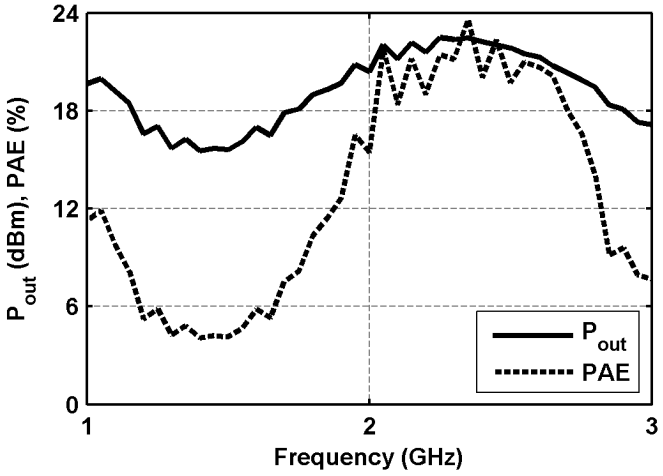

Fig. 4 Measured output power and PAE versus frequency.

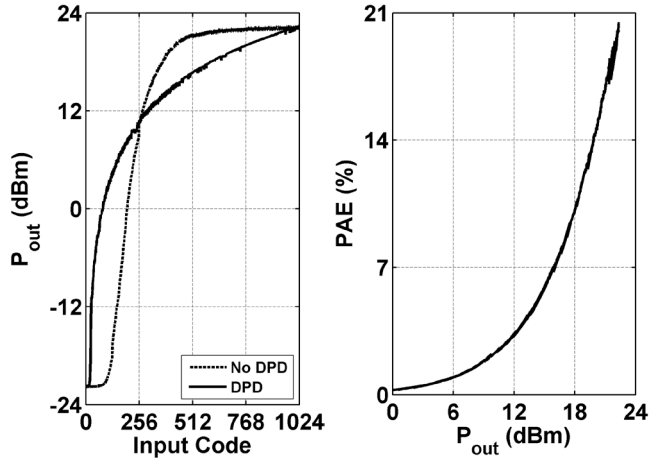

Fig. 5 (a) Measured output power vs. input code and (b) Measured PAE versus output power.

performed via a tapped inductor/tapped-capacitor (L_1, L_2, C_1, C_2) that presents the PA with the optimum resistance, susceptance and reactance required for class-E operation

Since class-E amplifiers offer high efficiency at the expense of device stress, a cascode implementation is applied to distribute voltage stress and improve device reliability [10]. With use of thick gate transistors, M_3 and M_4, the supply voltage V_{DD} can be safely increased to 2.5 V. The amplifiers amplitude is modulated with the I_{tail} port. The open loop transconductor (Fig. 1) controls the current flow to the amplifier and its output is proportional to the voltage provided by the SC-DAC, which is controlled by the envelope of the modulated signal. The measurement results for the SC-DAC modulated PA will now be presented.

III. Measurement Results

The SC-DAC modulated, class-E RF PA Is fabricated in a 130-nm RF CMOS process with 8 metal layers, including one ultra-thick metal. It occupies 2×2 mm including all pads, as shown in Fig. 3.

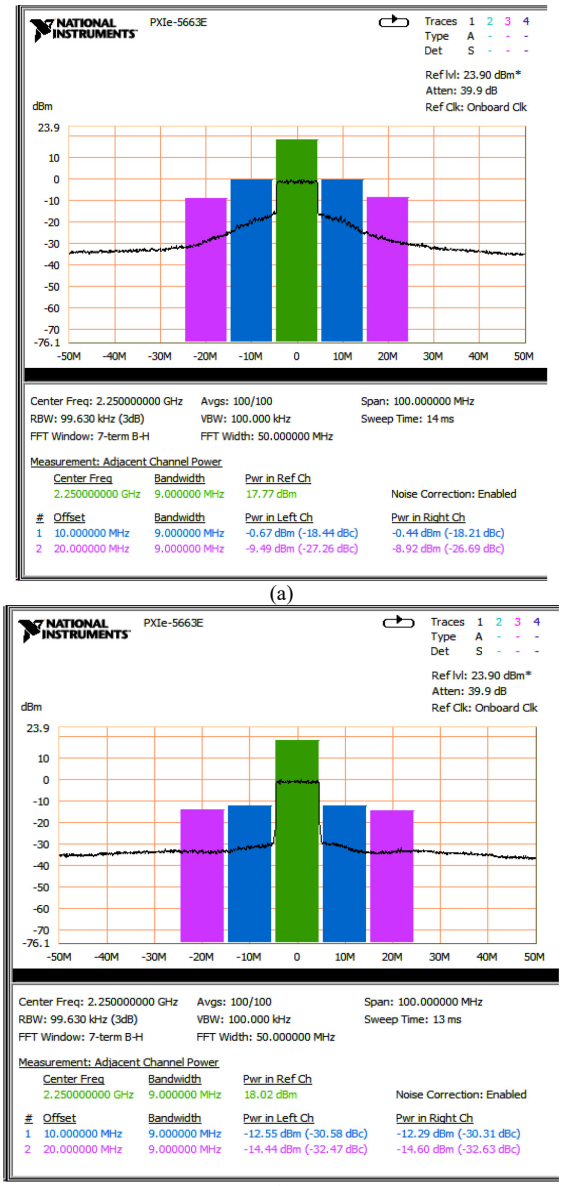

Fig. 6 Measured ACLR of the transmitter (a) without DPD (b) with DPD.

A. Static Measurement

The PAs static performance was characterized using a high-speed digital IO pattern generator, an RF vector signal generator and a vector signal analyzer. The Measured peak power and peak efficiency versus frequency is plotted in Fig. 4. At the designed center frequency of 2.4 GHz, the SC-DAC modulated EER transmitter achieves a peak power of 22.5 dBm with a corresponding power added efficiency (PAE) of 23.6%.

The output power is plotted vs the input code at 2.25GHz in Fig. 5a, for the DPD and non-DPD corrected signal. The PAE is plotted as a function of output power in Fig. 5b.

B. Dynamic Measurement

Due to the nonlinear behavior of the open-loop driver, digital predistortion (DPD) is applied [11] to improve the linearity of the EER transmitter. The PA output signals are detected and

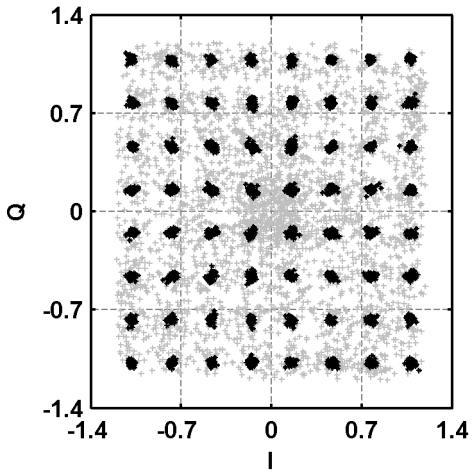

Fig. 7 Measured 10MHz 64 QAM LTE constellation demonstrating EVM=3.2%-rms after DPD. The constellation before DPD is in gray.

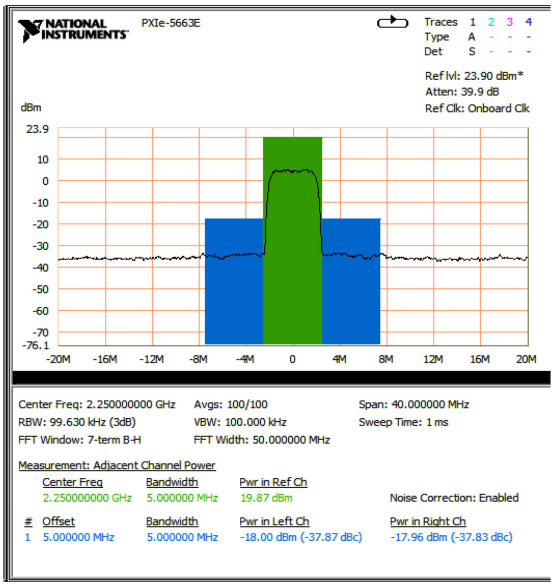

Fig. 8 ACPR measurement for a WCDMA signal.

lookup tables for the amplitude, A, and phase ϕ are constructed, respectively. Based on the lookup tables, A and ϕ are mapped to predistorted signals A' and ϕ', providing linearized signals at the PA output.

To evaluate the linearity of the EER transmitter with DPD, a 10MHz, 64QAM LTE signal is applied. The measured adjacent channel leakage ratio (ACLR) for adjacent and alternate channels is plotted in Figs. 6a with no DPD and 6b with DPD. The DPD improves the ACLR from -18.4dBc to -30.3 dBc, while the transmitter outputs an average power of 18 dBm.

The DPD drastically improves the PAs ACLR measurement and allows the transmitter to operate closer to saturation, improving efficiency. The measured average efficiency for this signal is 10.6%.

The demodulated LTE constellation diagram is shown in Fig. 7. The constellation is plotted before DPD in gray and after DPD in black. The EVM is improved from >19%-rms before DPD to 3.2%-rms after DPD.

To show the versatility of the PA, a WCDMA measurement is also performed. The ACPR measurement for this signal is plotted in Fig. 8. The average power is 19.9 dBm with an average efficiency of 14.3%. With DPD the ACPR is reduced to -37.8 dBc, from -24 dBc with no DPD. The constellation (not shown) has a measured EVM of 1.3 %-rms. To improve efficiency in future systems, such a modulator could be paired with a more efficient GaAs or GaN power amplifier, owing to the current driving capability of the presented supply modulator.

IV. Conclusions

A pipelined SC-DAC modulated EER transmitter is presented. It allows for reduced output quantization noise, and versatility due to the digital input and good system efficiency. This alleviates a prime issue in DPAs where the quantization is directly in the RF signal path. To compensate the nonlinearity of the open-loop transconductance amplifer, DPD is applied to improve the linearity of the EER transmitter. The circuit is fabricated in a 130 nm RF CMOS technology. At 2.25 GHz, the peak P_{out} and PAE are 22.5 dBm and 23.6%, respectively. By applying a test LTE signal, the transmitter linearity is validated. The output signal achieves an EVM of 3.6%-rms with an ACLR of -30 dBc at an average P_{out} of 18dBm. A WCDMA signal is applied to highlight the versatility of the transmitter.

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