Single-electron transistors featuring silicon nitride tunnel barriers prepared by atomic layer deposition

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***Abstract*—Single electron transistors (SET) featuring metal (Ni) electrodes and silicon nitride dielectric barriers prepared by atomic layer deposition are fabricated and tested. Electrical characterization of the devices reveals electrostatic energy parameters consistent with the parameters of the designed tunnel junctions. In addition, an analysis of temperature dependence of conductance confirms the formation of metal-insulator-metal (MIM) junctions with negligible in-series contribution of any surface native metal oxide. However, the fabricated devices exhibit a very high level of electrical noise, far exceeding the commonly observed shot noise. Experimental investigation reveals the random telegraph signal (RTS) nature of the observed excess noise. The RTS noise in electronic devices is commonly associated with charging of external traps that are electrostatically coupled to the SET island. In the devices under study, however, the defects that result in the observed RTS noise are demonstrated to reside *within* the tunnel junctions. Our results also indicate the critical importance of interface states and surface preparation for achieving good performance of the SETs fabricated using ALD to form the tunnel barrier.**

Keywords—single electron transistor, atomic layer deposition, silicon nitride, random telegraph signal, single charged defects.

I. Introduction

The downscaling of electronic device dimensions enables the use of ultrathin layers down to a few atomic layers which requires a good understanding of underlying physical and chemical processes that govern each nanofabrication step. In single electron transistors (SETs) [1] charge transfer through the device is guided by the Coulomb charging energy $E_C=e^2/2C$ where e is an elementary charge and C is the total capacitance of the island. The performance of an SET critically depends on the quality of a few-atomic-layer thick barrier in the source and drain tunnel junctions. For instance, the presence of defects in the dielectric will affect the noise exhibited by the SETs, and non-uniformities in the dielectric lead to strong variations in the SET characteristics. The unique sensitivity of SETs to single charge defects in the tunnel dielectric makes them ideal sensors for evaluating the quality of ultrathin dielectrics with "princess and the pea" sensitivity. Here, we use the electrical characterization of SETs to identify the origin of charged defects in the devices and to evaluate the strength of the observed noise. Additionally, several techniques are explored to passivate the defects in the fabricated devices.

II. Fabrication and Experiment

A. Device fabrication

The metal-insulator-metal (MIM) SETs are fabricated using a combination of high-resolution electron beam lithography (EBL), nanodamascene planarization, and Si_3N_4 tunnel barrier dielectric formation using plasma-enhanced atomic layer deposition (PEALD) [2, 3]. Figure 1 shows a micrograph of a fabricated device. First, using a Vistec EBPG 5200 100-keV EBL system, the pattern of the island is defined in polymethylglutarimide (PMGI) spun on the thermal SiO_2 substrate [4]. PMGI is used as a mask for SiO_2 etch due to its higher etch resistance than polymethylmethacrylate (PMMA). The pattern of the island is then transferred into the oxide using Ar, C_4F_8, CHF_3, and CF_4 chemistry in an inductively coupled plasma (ICP) etcher. Next, Ni is deposited by e-beam evaporation at the base pressure of $<8\times10^{-7}$ Torr to fill the trench in SiO_2, while the field is still covered by the remaining PMGI mask. The evaporated metal on the field along with the underlying PMGI is then lifted off by MR-Rem 400 stripper from Micro Resist Technology, heated to 70°C. Chemical mechanical polishing (CMP) is then used to remove any residual Ni on the oxide field, while leaving the island trench filled with Ni. Next, 21 cycles of PEALD of Si_3N_4 is performed in an Oxford FlexAL system, with Bisdiethylaminosilane ($C_8H_{22}N_2Si$) and H_2+N_2 plasma to form the Si_3N_4 dielectric barrier covering the island. Finally, Ni source and drain are defined by a second EBL and liftoff. Two post-fabrication treatments were also investigated: H_2 plasma treatment to ensure reduction of NiO potentially formed during exposure of the junctions to the ambient, and N_2 plasma treatment with the goal of passivating the nitrogen vacancies that are possibly formed in the barrier.

B. Experiment

Next, devices are bonded to a chip carrier and electrically tested in the range of temperatures from 300K down to 0.4K in a closed-cycle ^{3}He refrigerator. For electrical characterization we use standard lock-in technique with AC and DC voltage sources connected to the drain, and source connected to the input of transimpedance amplifier. Differential conductance $G=dI_{ds}/dV_{ds}$ is measured at 8-30 Hz with excitation level of 1 mV in the temperature range of 300 K-10 K and 100 μV for lower temperatures down to 0.4 K. The conductance of fabricated devices measured at room temperature exhibits wide spread of values, from 10 nS up to 1 μS for nominally identical devices. This is likely to originate from non-uniformities in the Si_3N_4 that is formed during the PEALD.

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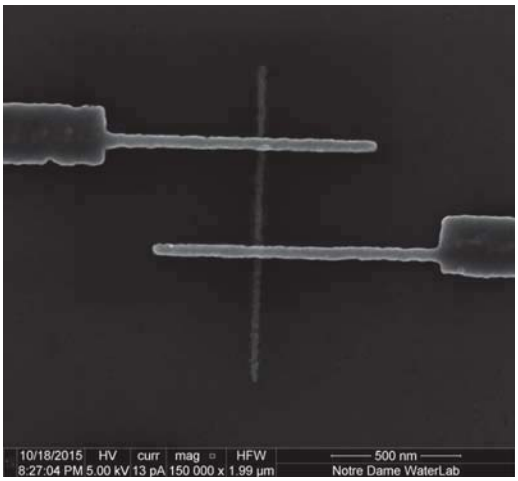

Fig. 1. Scanning electron micrograph (SEM) of the fabricated device

Two dimensional maps $G(V_g, V_{ds})$, a standard test for SET characterization, are acquired for more than 10 devices, and all of them show "Coulomb diamonds" with the shape typical for SETs with MIM junctions and characteristic energy gap, $4\times E_C$ in the range 1.5 to 2 meV. An experimentally obtained diamond plot for a typical device is shown in Fig. 2a. To evaluate parameters of the junctions, we perform simulations based on orthodox model [5], where the capacitance matrix is defined using parameters obtained from the shape of Coulomb diamonds [1], and the values of the junction conductances are obtained by fitting the shapes of experimental $G(V_{ds})$ measurements to the model. Fig. 2b shows the results of simulations with the following parameters: C_s=45 aF, C_d=52 aF, C_g=27.6 aF, G_s=0.55 µS, and G_d=0.2 µS. Neglecting fringing field, a parallel plate estimate for junction capacitance of 30 × 20 nm^2 overlap and using SiN with dielectric constant of ε=7 and thickness of 1 nm, gives the value of the expected junction capacitance ~35 aF, in reasonable agreement with the experiment.

Dissimilar (by a factor of >2) conductance of the junctions can be attributed to non-uniformities in the ALD dielectric layer where a thinner "weak spot" in the dielectric may drastically change device conductance while not significantly affect its capacitance. An important known issue for MIM SET devices with ALD dielectric is the formation of interfacial metal oxide during the ALD process [2, 3, 6], resulting in a strong temperature dependence of conductance in the peaks of Coulomb blockade oscillations (CBOs). To investigate the potential presence of NiO in Ni-Si_3N_4-Ni junctions, we measure temperature dependence of the SET zero-bias conductance for a slowly increasing temperature. During the experiment, the V_g bias is continuously swept over five periods of CBOs while temperature slowly increases, so the temperature dependence of conductance can be accurately evaluated at both peaks and valleys of CBOs. The result of the experiment is presented in Fig. 3, where ln $G(V_{ds}=0)$ is plotted as a function of inverse temperature 1/T. According to the orthodox theory of Coulomb blockade for MIM SETs [7], as the temperature is reduced to T≈ $4Ec/k_B$, the conductance

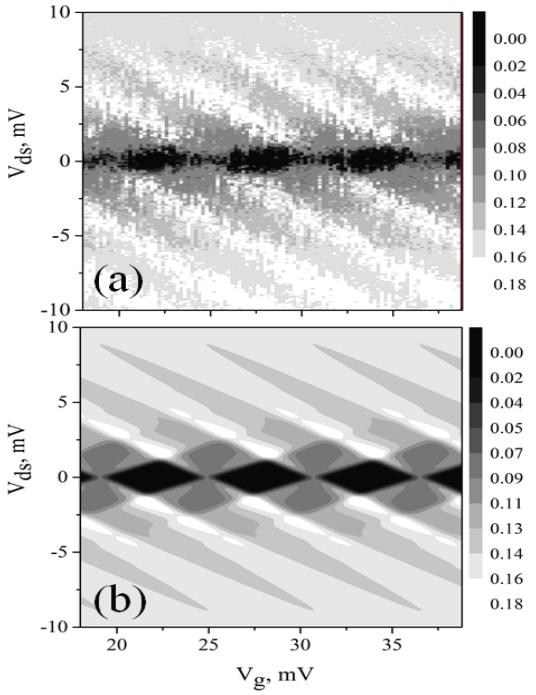

Fig. 2. Typical Coulomb diamond plot for SET with 21 layer of SiN (sample NT-G1): (a) experiment (b) simulations using orthodox model. Gray scale in µS.

through the device decreases due to Coulomb blockade in the island. As the temperature is lowered, the differential conductance in the peaks of the CBO stays at a level $G_{max}=G_0/2$ (blue dashed line in Fig.3) where G_0 is conductance at high temperature ($T>>E_C/k_B$), while with lowering T the conductance in the valleys is exponentially suppressed with an activation energy of E_C: $G(T)=G_0 \exp(-E_C/k_BT)$. The experiment shows exactly this: for $1/T<0.2$ the data are merged into a line, while for $1/T>0.2$ the line diverges into an

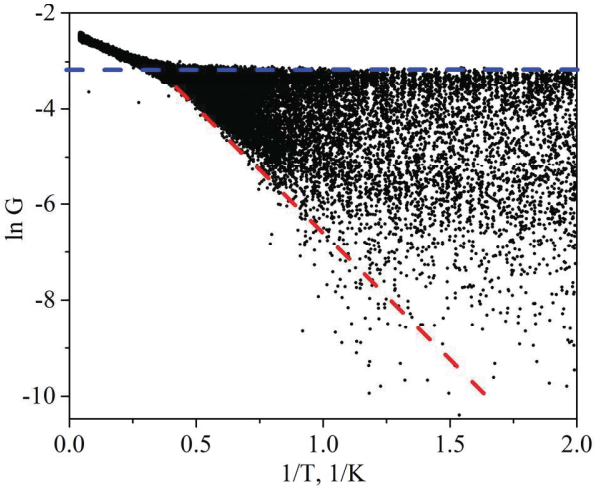

Fig. 3. Temperature dependence of conductance at V_{ds}=0. Data are acquired for V_g bias swinging in the range over five periods of Coulomb blockade oscillations for slowly changing temperature. Variation in the density of points is the result of non-linear axis transformation.

area with minimal values approaching the red dashed line corresponding to the thermal activation over the barrier. A very close proximity of the expected CBO maxima to the blue dashed line ($G_0/2$) indicate an insignificant contribution of in-series thermally activated NiO surface oxide in the junctions to the total conductance [2, 3] and the activation energy $E_A \approx 0.5$ meV extracted from this measurement closely matches the charging energy value obtained from Coulomb diamond plot.

The observed Coulomb diamond plot also reveals a very large level of excess "switching noise." An example of such noise is shown in Fig. 4, where two traces of $G(V_{ds})$ were measured for the same V_g, showing multiple jumps between several states. This is a signature of RTS, a random phenomenon stemming from capture and release of charge carriers in single traps near the conducting channel of an electronic device [8]. In the case of SETs, the RTS can be treated as an additional offset charge that modulates conductance through the SET, a process that was investigated in detail in [9]. If several of such modulators are active simultaneously the resulting pattern is identified as "multi-level RTS" [10]. To understand the origin of this noise we experimentally acquire a large number of $G(V_{ds})$ traces, in addition to those shown in Fig 4, for a fixed value of V_g and then calculated the "time averaged" curve (red line in Fig 5a). We also averaged $G(V_{ds})$ traces over the full span of 3 experimentally obtained Coulomb diamonds (magenta line in Fig. 5a). As expected, "diamond average", i.e. conductance averaged over full Coulomb diamond has no oscillatory features. In contrast, noticeable oscillatory features are observed for time averaged trace at fixed V_g in Fig 5a. To replicate the experimentally observed features with simulations we performed iterative averaging over a variable span of V_g, centered on the gate bias used in experiment (red line in Fig. 5b). For simplicity, a uniform distribution was assumed for curves weights in the averaging V_g interval. Additionally, a diamond average over three full diamonds was calculated (magenta line in Fig 5b). Finally, we subtracted respective diamond averages from time average (experiment) or narrow V_g span average (calculations). The results shown in Fig. 5c are in reasonable agreement with each other, indicating the validity of the proposed charge offset evaluation technique.

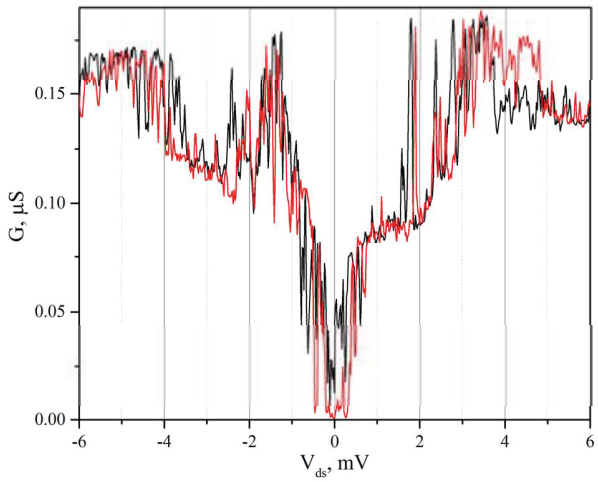

Fig. 4. Two consecutive sweeps of V_{ds} taken at V_g=27 mV (sample NT-G1). Very strong "switching noise" is clearly visible.

C. Discussion

We believe that the observed results shed light on the equivalent magnitude of charge offset noise. Experiment reveals that the observed time averaged $G(V_{ds})$ trace can be replicated by averaging of multiple traces uniformly distributed in the offset charge span of $\delta Q_g = e\,(\delta V_g/\Delta V_{CBO}) \approx 0.3\ e$. This is a "full swing" of charge fluctuation, meaning that deviation from average is up to 0.15 e in a bandwidth of 0.78 Hz, or 0.17 e/√Hz. This is a very large noise level, exceeding by many orders of magnitude both the shot noise caused by charge discreteness and 1/f noise that limits the sensitivity of SETs at levels $\approx 10^{-4}/\sqrt{\text{Hz}}$ at low frequencies. Can a single trap in a junction lead to this level of charge fluctuations? The impact of charging of a single electron trap depends on coupling of that trap to the island. The case of charged traps coupled to gate, island and source (or drain) of the SET was studied in [11], where it was observed that a single trap can cause an abrupt shift in CBO pattern (e.g. from peak to a valley). Note that in such a case the appearance of a specific trap is gate voltage dependent (i.e. it changes the conductance over specific range of gate bias and stays "mute" elsewhere [9, 11]). Here the situation is qualitatively different: the switching events are "gate independent" i.e. occurring with equal probability at any gate voltage. That implies that the source of switching is not electrostatically coupled to the gate. Therefore it is reasonable to assume that the source of this noise is located *within* the tunnel junctions - either in the ALD dielectric or in the interfacial layers adjacent to the dielectric where it is shielded from electric field emanating from the gate. The trap charging/discharging process in the junction decoupled from the gate nonetheless leads to offsets of Coulomb diamond patterns along V_g axis because the action of that trap is equivalent to an extra gate potential acting on the island. The strength of coupling from such trap to the island determines the strength of the observed shift. If a trap located in the source

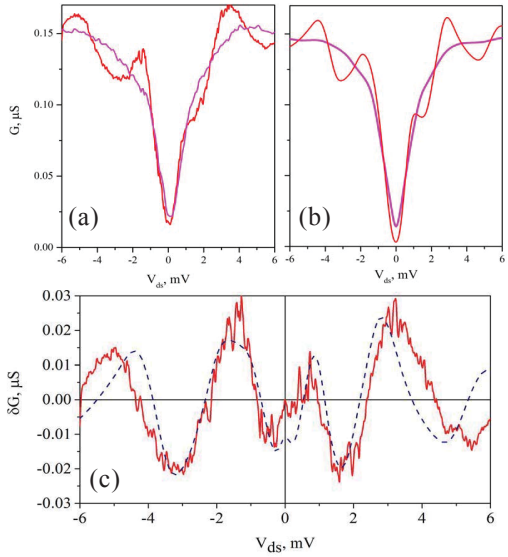

Fig. 5. Results of $G(V_{ds})$ "span average" vs time average at V_g=const: (a) – experiment. Red: average of 57 traces at V_g=27 mV. Magenta: "diamond average," i.e. traces averaged over V_g span of three full Coulomb diamonds in Fig. 2 a. (b) – simulations. Red: ensemble average over 25.5 mV< V_g<27.2 mV span. Magenta: diamond average over V_g span of three full Coulomb diamonds in Fig 2 b.(c) Comparison of the experiment and the simulations after "diamond average" subtraction. Red–experiment; dashed blue line- simulations

(drain) junction is equally coupled to the source (drain) and the island, the change in its population by one electron will exert a 0.5 *e* charge and shift the diamonds by a half of a CBO period. The experimentally observed averaged diamond shift of 0.2-0.3 *e* can be explained by action of the traps located closer to the junction's interfaces (i.e. asymmetrically coupled, leading to smaller charge offsets) or may results from oversimplified model used in simulations. Nonetheless, this value is consistent with the model of traps acting inside the junctions. Since the observed switching noise has no identifiable voltage threshold in V_{ds} it is reasonable to assume that several different traps located inside the tunnel junction are participating in the process: as V_{ds} changes, certain traps become active within certain range of V_{ds} resulting in a "multiple RTS" signature. The exact number of traps participating in the process is not precisely known and remains to be investigated.

We have previously demonstrated that by using a combination of anneal and reducing plasma treatments it is possible to nearly completely suppress this type of noise in Ni-SiO_2-Ni junctions [12]. In other words, those charge defects could be potentially healed with proper treatments.

So far, N_2 plasma on the finished devices to fill the nitrogen vacancies in the nitride or H_2 plasma to chemically reduce the parasitically formed NiO does not seem to be effective in decreasing the observed noise. One potential drawback of such treatments after device fabrication is the top Ni source-drain electrodes that impede delivery of the chemical elements (H_2 and N_2) to the underlying barrier and island. The abundant traps in SiN film are generally obtained by N atoms substituted by Si atoms, producing silicon dangling bonds, referred to as *K*-center defects [13]. Other defects can be associated with the presence of hydrogen typically present in the Si-N structure [14]. It was shown that the number of defects can be reduced by high temperature (~1000°C) heat treatment of the layer or producing Si-rich compositions [13]. Another source of defects which need to be addressed is inadequate surface preparation.

III. Conclusions

In conclusion, the MIM SETs featuring ALD Si_3N_4 as barrier dielectric are fabricated for the first time, to the best of our knowledge. Analysis of temperature dependence of conductance confirm the formation of MIM junctions with negligible in-series contribution of native surface oxide, in contrast with the NiO that is observed to parasitically form in MIM Ni-SiO_2-Ni junctions, [2, 3]. However, very large magnitude of observed RTS noise indicates a large density of traps inside the tunnel junctions. We are currently investigating high temperature and plasma treatments of the Si_3N_4 ALD layers and improved surface preparation to reduce the number of defects inside the junctions. Noise analysis technique proposed here can be also extended for characterization of various single-electron devices and identification of charged defects in these structures.

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