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Fabrication of nanodamascene metallic single electron transistors with atomic layer deposition of tunnel barrier

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The fabrication is reported of nanodamascene metallic single electron transistors that take advantage of unique properties of chemical mechanical polishing and atomic layer deposition. Chemical mechanical polishing provides a path for tuning the dimensions of tunnel junctions by adjusting the polish time, surpassing the limits imposed by electron beam lithography and lift-off, while atomic layer deposition provides precise control over the thickness of the tunnel barrier and significantly increases the choices for barrier materials. Single-electron transistor operation of a prototype device was successfully demonstrated at $T < 1$ K. © *2015 American Vacuum Society*.
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I. INTRODUCTION

As the most sensitive electrometers to date, single electron transistors (SETs) are capable of detecting a fraction of elementary electron charge, as small as 10^{-6} e/$\sqrt{\text{Hz}}$ (Ref. 1) and are naturally suitable for detecting nanometer scale displacement,[2] gas sensing down to single molecules,[3] and readout sensors in atomic level computing architectures such as quantum cellular automata.[4–6] Additionally, single electron transistors provide a means to characterize ultrathin tunnel barriers and the interface between the deposited dielectric and the substrate, which is important in the characterization of CMOS relevant dielectrics, such as MOSFET gate stack materials.[7]

SETs are composed of a nanometer-scale island that is separated from source and drain leads by ultrathin (~1 nm) tunnel barriers. The island is capacitively coupled to a third electrode, referred to as the gate that can adjust the island potential and thus control the electron transport through the island. An important figure of merit for an SET is the charging energy, E_C, defined as $E_C = e^2/2C_\Sigma$, where C_Σ is the total capacitance of the island. The charging energy of an SET sets an upper limit on its operating temperature, as the thermal energy of electrons must be much smaller than the charging energy, i.e., $E_C \gg k_BT$ (in practice, $Ec \geq 3\,k_BT$ is sufficient for device operation), where k_B is the Boltzmann constant and T is the absolute temperature.[5] A low-k dielectric barrier and small size tunnel junctions can considerably lower the junction capacitance and consequently increase the operating temperature of SETs.

In this paper, we present a fabrication method for metal–insulator–metal (MIM) SETs with planar nanometer-scale tunnel junctions using chemical mechanical polishing (CMP) and atomic layer deposition (ALD). In this scheme, CMP provides a path for scaling down the dimensions of the tunnel junctions beyond the dimensions imposed by electron beam lithography (EBL) and lift-off, since by careful adjustment of the polish step, the depth (height) of the junctions can be further reduced, and planar tunnel junctions with less than 10 nm in thickness are achievable.[8] The cyclic deposition of ALD, with one monolayer of the desired material deposited in each cycle, makes it a more controllable and precise method to form ultrathin tunnel barriers compared to the formation of the barrier from the native oxide of metal substrates. Recently, a Pt-based SET with thermal ALD Al_2O_3 tunnel barrier has been reported.[9] This is of great importance since previously, only native oxides of the metal electrodes (e.g., Al, Cr, Ti, and Ni) formed the tunnel barrier in metal-based SETs.[10–14] Moreover, the use of ALD enables formation of low-k SiO_2 dielectric on metal substrates.

II. NANODAMASCENE SET FABRICATION

Figure 1 shows the schematic of the fabrication steps in MIM nanodamascene SETs. Damascene is an inlay patterning method using CMP commonly employed in fabricating copper interconnects in integrated circuits.

The device is fabricated on a SiO_2 insulating layer thermally grown on a silicon wafer. First, polymethylglutarimide (PMGI) SF5 from MicroChem is spun on the substrate at 1500 revolutions per minute (rpm) and is subsequently baked at 180 °C for 5 min to give a 225 nm film. The pattern of the 30 nm wide island is exposed in PMGI using a Vistec EBPG 5200 100 keV EBL system with an area dose of 6.5 mC/cm^2. Following the exposure, the PMGI is developed in Xylenes for 12 min using ultrasonic agitation [Fig. 1(a)]. PMGI developed in Xylenes has been shown to have a higher contrast than polymethylmethacrylate, and can be used as a mask in SiO_2 plasma etching due to its higher etch resistance.[15] Plasmalab System 100, an inductively coupled plasma-reactive ion etcher (ICP-RIE), from Oxford Instruments is used to transfer the island pattern from PMGI to the SiO_2 substrate in a 15 s etch step using a fluorine-based chemistry at 8 mTorr composed of 20 standard cubic centimeter per minute (sccm) Ar, 5 sccm C_4F_8, 15 sccm CHF_3, and 20 sccm CF_4 [Fig. 1(b)]. The RIE power of 150 W and the ICP power of 1000 W result in a DC bias of 290 V and a SiO_2 etch rate of 360 nm/min. MR-Rem 400 from Micro Resist Technology, heated to 70 °C, is used to strip the PMGI mask. Next, the etched island pattern is filled

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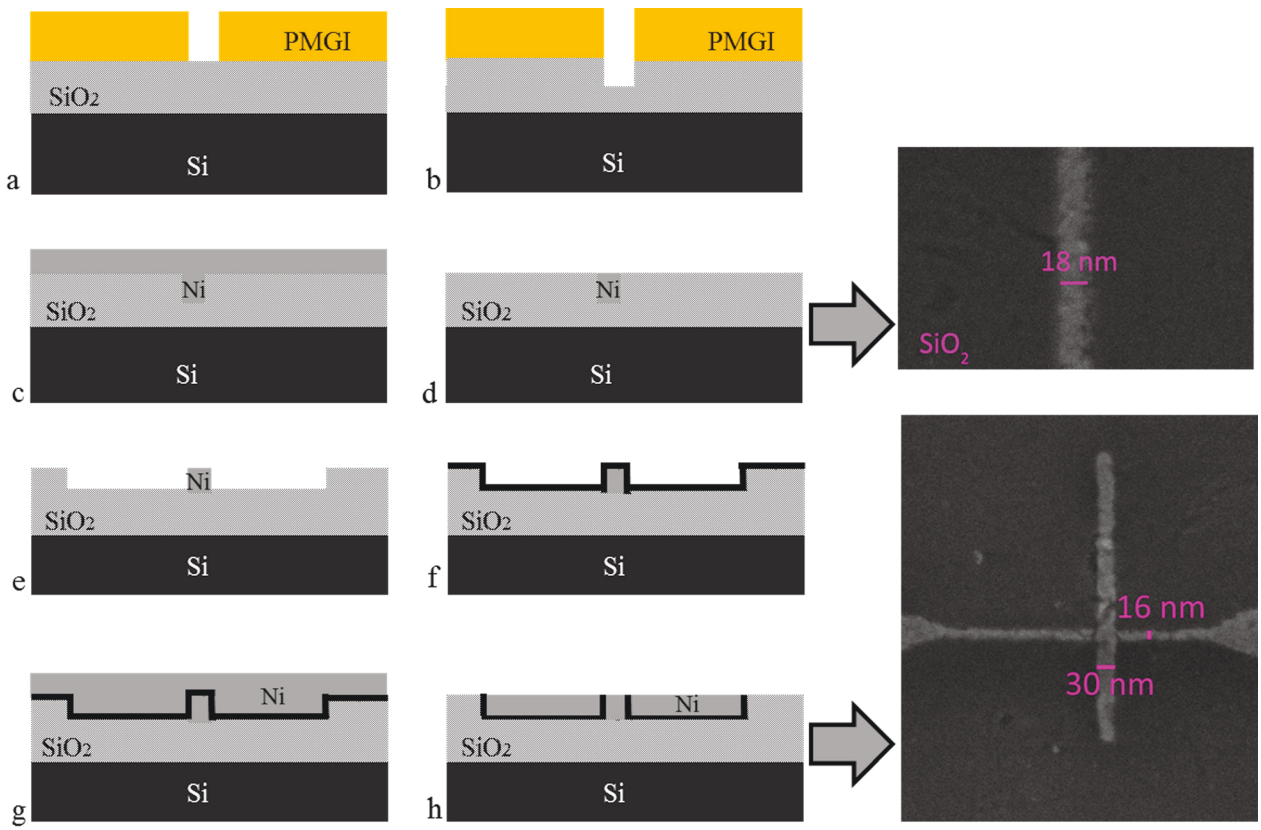

FIG. 1. (Color online) Schematic of nanodamascene SET fabrication steps: (a) Island pattern is exposed on PMGI during an EBL. (b) The developed PMGI is used as a mask to transfer the island pattern in the underlying oxide with an ICP etch step. (c) PMGI is removed from the sample, and a blanket Ni evaporation is performed on the sample. (d) In a CMP step, metal overburden is polished off the sample leaving the island trench filled with Ni, as shown in the image taken with SEM. (e) During a second EBL and ICP etch, the pattern of the source and drain is transferred to the thermal SiO_2 substrate. (f) Plasma Enhanced Atomic Layer Deposition (PEALD) is used to form the dielectric barrier on the island. (g) Blanket Ni evaporation fills the source and drain trenches. (h) Ni overburden on the thermal SiO_2 field is polished away during a second CMP, and the SEM image shows the junctions between the island, source, and drain.

with Ni in a blanket 100 nm Ni evaporation [Fig. 1(c)]. The subsequent Ni CMP step using Eminess Ultra Sol A19, alumina based slurry at $p\mathrm{H} = 4$, diluted 50% with Deionized (DI) water, removes the Ni in the field, leaving only the Ni in the island trench [Fig. 1(d)]. Platen and carrier head rotation speed of 60 rpm, 125 ml/min of slurry dispensing rate on the pad, and 0.7 pound force per square inch (psi) of applied pressure on the wafer carrier result in 360 nm/min Ni polish rate in an Orbis CMP system from Logitech. After polishing the metal overburden on the oxide, a perpendicular line to the island is written in PMGI during the second EBL to form the pattern of the source and drain. A similar etch recipe is used to transfer the pattern into the SiO_2 [Fig. 1(e)]. It is worth mentioning that the plasma etch recipe is designed to leave vertical sidewalls in the oxide. A re-entrant profile in the island (where the angle between the sidewalls and the bottom of the trench is more than 90°) results in an undercut in the adjacent source and drain trench, which is challenging to refill with metal evaporation, and unfilled voids lower the fabrication yield. Next, MR-Rem 400 followed by a 10 s ashing step in DryTek plasma asher strips PMGI from the substrate, and 9 cycles of PEALD Al_2O_3 tunnel barrier is deposited using trimethylaluminum (TMA) and O_2 plasma at 300 °C [Fig. 1(f)]. During TMA introduction in the first step of PEALD, chamber pressure is held at 15 mTorr for 40 ms, while the pressure is held at 15 mTorr for 2 s in second step of 40 sccm Ar + 60 sccm O_2 plasma. The described PEALD recipe has a nominal Al_2O_3 deposition rate of 0.11 nm/cycle. The residual carbon on the deposited Al_2O_3 must be cleared with a 10 s ashing step in Drytek plasma asher. Based on our observations, the two ashing steps mentioned above play an important role in the adhesion of Ni to the dielectric and can significantly affect Ni CMP results. Next, 200 nm blanket Ni is deposited by e-beam evaporation [Fig. 1(g)], and using CMP with the similar conditions as mentioned above for 25 s, the Ni on the field is removed, leaving the trenches filled with metal [Fig. 1(h)]. By controlling the depth of the final CMP polishing step, the depth and hence the cross-sectional area of the device can be reduced, which can give a higher charging energy. The proposed self-aligned process enables fabrication of ultrasmall tunnel junctions, down to a few nanometers in each dimension, and thus using this process, an operating temperature of the SET up to 70 K should be possible.

III. RESULTS AND DISCUSSION

Figure 2 shows a scanning electron microscopy (SEM) micrograph of the tested device, fabricated using the process described above.

Electrical measurement of the device is performed using standard lock-in techniques with a 0.3 mV excitation voltage at 38 Hz. The wire-bonded sample is attached to the ^{3}He pot of a closed cycle refrigerator; the temperature is monitored by a thermometer attached to the chip carrier.

The oscillations of the differential drain–source conductance, G_{ds}, as a function of gate potential, the Coulomb blockade oscillations (CBOs) at $V_{ds} = 0$ V and $T \sim 0.46$ K are shown in Fig. 3. A relatively small peak to valley ratio ($\sim$2) is indicative of low E_c/k_BT ratio.

Charging diagram of the device, also referred to as the Coulomb diamond plot, is shown in Fig. 4(a). For comparison, we performed simulations of the charging diagram [Fig. 4(b)] based on orthodox Coulomb blockade theory for an MIM SET with $C_d = C_s = 145$ aF and $C_g = 21$ aF at 0.46 K, using code developed in Ref. 16.

The value of gate capacitance is chosen to replicate the period of Coulomb blockade oscillations while the values of junction capacitances are chosen based on the sample geometry: a 45 nm wide, 40 nm deep rib is expected to result in junction capacitance of $C_d = C_s = \varepsilon_o \varepsilon A/d = 143$ aF, where ε_o and $\varepsilon = 9$ are, respectively, the vacuum permittivity and the dielectric constant of Al_2O_3, A is the junction area, and $d \sim 1$ nm is the thickness of 9 cycles Al_2O_3 tunnel barrier, based on the 0.11 nm/cycle nominal growth rate. The expected charging energy based on geometry is 0.27 meV. Although Coulomb diamonds in the blockaded regions of Fig. 4(a) are distinguishable and the height of the diamonds in V_{ds} is similar to the simulations, there is a noticeable discrepancy between theoretical predictions and the experimental observations outside the central diamonds.

Based on the theory,[17] in MIM SETs at low temperature ($k_BT \ll E_C$) the differential conductance at $V_{ds} = 0$ oscillates between the peaks (G_P) and the valleys (G_V) of CBOs, where $G_P = G_0/2$, $G_V \approx G_0 \exp(-E_C/k_BT)$, and G_0 is the differential

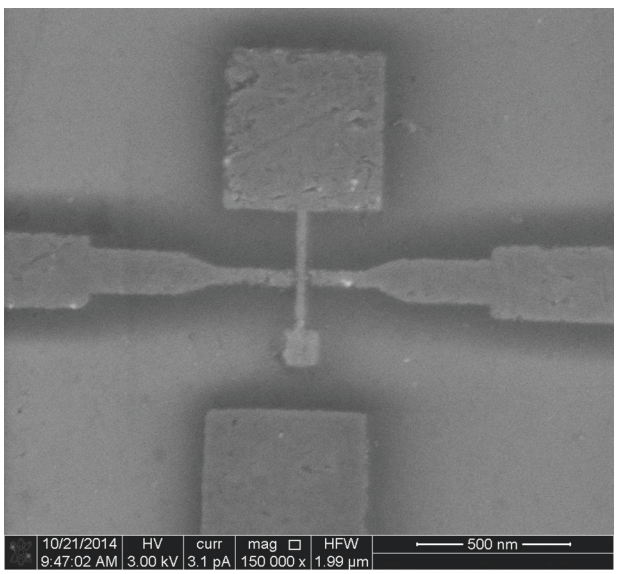

FIG. 2. SEM image of the nanodamascene SET. The 500 × 500 nm^2 pad is attached to the island to make it visible in the optical microscope. In the newer batch of devices, this pad has been detached from the island to further lower its capacitance.

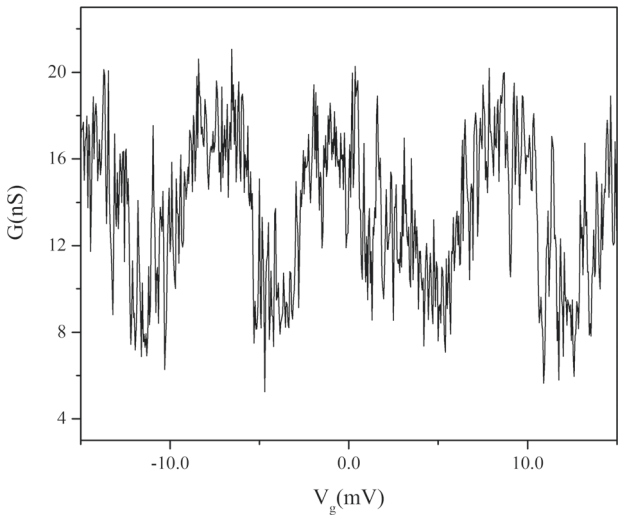

FIG. 3. Coulomb blockade oscillations of the device measured at 0.46 K.

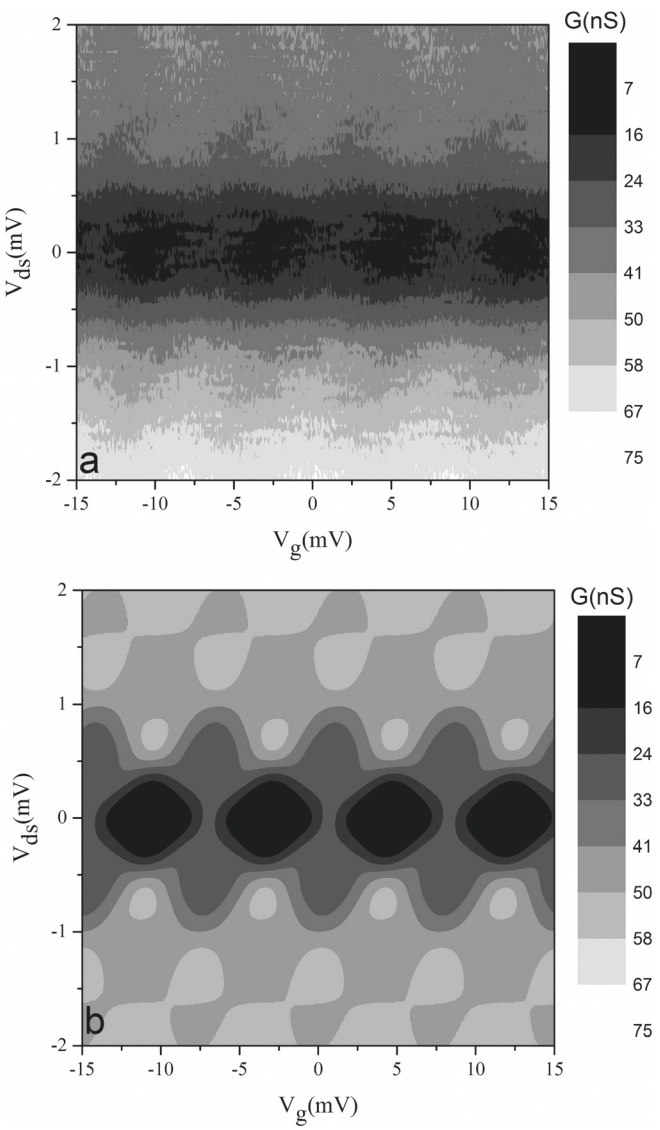

FIG. 4. (a) Coulomb diamonds of the fabricated nanodamascene SET measured at 0.46 K, (b) simulated Coulomb diamonds with $C_d = C_s = 145$ aF and $C_g = 21$ aF.

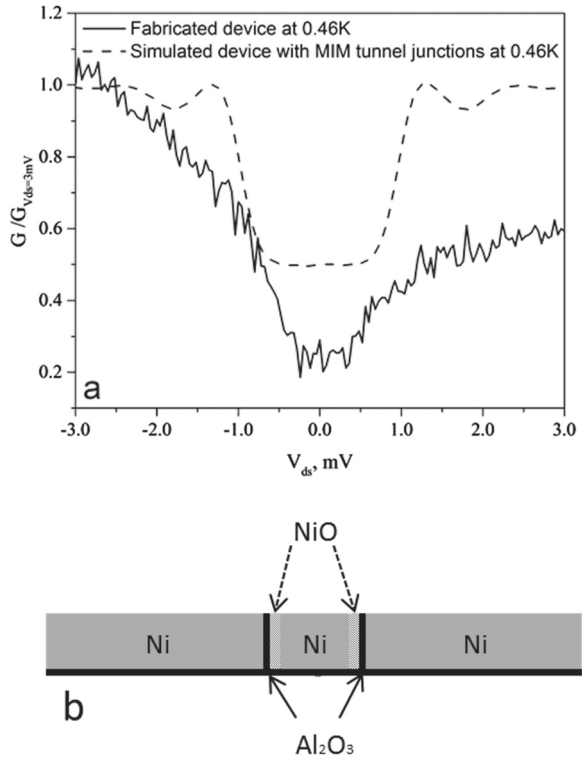

FIG. 5. (a) Differential conductance of the fabricated and simulated devices vs DC bias applied across source and drain (V_{ds}) for $V_g = 8$ mV, where $G(V_g)$ is at maximum. For the simulations the conductance is normalized by the G_0 (i.e., G ($V_{ds} \gg E_C/e$) and for the experimental data the $G(V_{ds} = 3$ mV) is used for normalization($V_{ds} = 3$ mV $\gg E_C/e = 0.27$ mV). (b) Schematic diagram of the parasitic NiO formed in the drain- and source-island junction as the island is subjected to the O_2 plasma step in PEALD of Al_2O_3. The top surface of the island is also oxidized but is most probably polished away during the second CMP step.

conductance at $k_BT \gg E_C$. For large applied source–drain bias, $V_{ds} \gg E_C/e$, the differential conductance is almost constant, and approaches the high temperature limit, G_0. However, for the fabricated device measured at 0.46 K, the differential conductance at peaks of CBOs (e.g., for $V_g = 8$ mV in Fig. 3) is $G_P(V_{ds} = 0) \sim 18$ nS, that is, by more than an order of magnitude smaller than the room temperature value $G_0(V_{ds} = 0) \approx 1\ \mu$S.

Figure 5(a) shows an experimental $G_{ds}(V_{ds})$ dependence measured at a peak of CBO at $V_g = 8$ mV (solid black curve), along with the $G_{ds}(V_{ds})$ for the simulated device (dashed black curve). To get a comparable scale in y-axis, the conductance of both devices is normalized. Clearly, in the simulations, G_{norm} changes from 0.5 at $V_{ds} = 0$ to ≈ 1 at $V_{ds} = 3$ mV, whereas in experiment, G_{norm} decreases well below 0.5 at $V_{ds} = 0$. There is also a noticeable asymmetry in the experimental curve.

It is therefore reasonable to assume that there must be a parasitic thermally activated resistive component in series with the tunnel junctions that results in the observed deviations from the simulated MIM SET characteristics.

We believe that these experimental observations are consistent with the presence of NiO layers in series with the tunnel barriers, as schematically illustrated in Fig. 5(b); this oxide appears as an extra "parasitic" resistance in series with the tunnel junctions. The formation of metal oxides during plasma enhanced ALD has already been studied for different metallic substrates,[18] and our recent studies[19] confirm the formation of parasitic NiO layers during PEALD process. Thin NiO layers on Ni have been reported to exhibit electrical properties consistent with a presence of a small (<0.2 eV) potential barrier.[20] At room temperature, the charge carriers have enough energy to overcome this barrier and thus its contribution to total resistance is small. As the device is cooled down, the resistance of NiO layers exponentially increase, since fewer carriers are thermally excited, and this leads to an increased contribution of parasitic in-series resistance, and consequently to the reduction of the measured S-D conductance. A noticeable asymmetry in the experimental data of Fig. 5(a) can be attributed to a random nonuniformity in the parasitic oxide in the junctions.[21] We are currently studying different techniques to achieve the reduction of this layer back to metallic Ni to improve the performance and increase the yield of the fabricated devices.

IV. SUMMARY AND CONCLUSIONS

We have presented the first experimental demonstration of a nanodamascene-fabricated metallic SET, fabricated using atomic layer deposition, chemical mechanical polishing, and other CMOS compatible processing steps. Atomic layer deposition provides precise formation of the tunneling barriers while chemical mechanical polishing enables the fabrication of features potentially smaller than those possible with lift-off. Our devices showed the effects of a parasitic NiO that is formed during the PEALD of Al_2O_3, which is believed to cause a change of conductance other than that expected from Coulomb blockade when the device is cooled down or is excited with DC bias across the source and drain. NiO reduction is currently under investigation and will be reported elsewhere.

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