

Variance-based Digital Logic for Energy Harvesting Internet-of-Things

Sri Harsha Kondapalli, Xuan Zhang and Shantanu Chakrabartty

Department of Electrical and Systems Engineering
Washington University in St. Louis, MO, USA 63130
Email: sriharshakondapalli@wustl.edu

Abstract—In this paper we propose a novel approach for designing digital circuits that uses the variance of a signal to represent Boolean logic levels. The variance-based logic (VBL) representation enables embedding of rectification and multiplication modules within the basic logic cells and unlike AC-coupled or energy-recovery logic circuits the proposed approach obviates the need for any phase synchronization. As a result, VBL representation can be used for designing low-latency digital circuits that are directly powered by a combination of energy transducers with different frequency and source impedance characteristics. We present some representative examples of VBL circuits that can be implemented in a standard CMOS process and we present measurement results from fabricated prototype.

I. INTRODUCTION

Paramount to the concept of a smart city of the future is the idea of a smart civil infrastructure that can self-monitor and predict any impending failures. Also in the case of an extreme event (e.g. earthquakes or fire) the infrastructure can self-identify portions that would require immediate repair and prioritize areas for emergency response. To facilitate this grand-vision, we have been working towards a framework of infrastructural Internet-of-Things (i-IoT) using an array of self-powered embedded structural health monitoring sensors [1]. This is illustrated in Fig. 1 (a), where an array of self-powered sensors is shown to be embedded inside a pavement structure and are also attached to the span of a bridge. Examples of such embedded sensors have been previously reported [2] and Fig. 1(b)-(d) shows some representative prototypes. These sensors continuously monitor variations in mechanical strain at critical points of the structure and store the statistics in an on-board non-volatile memory. Wireless retrieval of the stored data is achieved using a radio-frequency identification (RFID) interface and in our previous works [1] this functionality was demonstrated without considering any real-time constraints. However, when the sensors are deployed in large-scale, as is the case for an i-IoT framework, the RFID reader will be typically mounted on a vehicular platform (a maintenance truck or an aerial drone, as shown in Fig. 1(a)) and the sensor data needs to be retrieved in real-time. As an example, for a truck with a span (size of RF antenna) of 10 cm, moving at a speed of 60-90 mph the interrogation latency amounts approximately 2.5-3.7 milliseconds, during which the RFID interface has to be energized and interrogated.

Current RFID and other RF-based energy harvesting systems use a charge multiplying approach to accumulate and

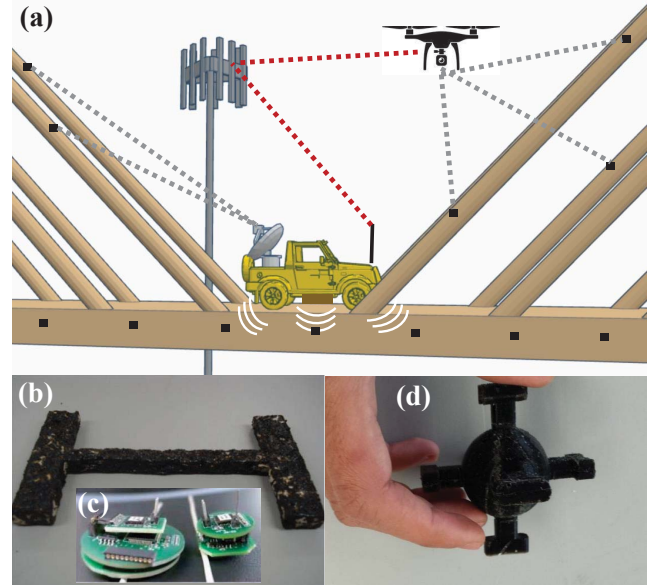


Figure 1. (a) Framework of an i-IoT comprising of embedded sensors that are wirelessly interrogated using a vehicular RFID interface [1].(b)-(d) Examples of fully packaged self-powered sensors with an integrated RFID interface [1].

store energy on a battery or super-capacitor. This is illustrated in Fig. 2(a) where the accumulated energy is used to power the computation and communication module. However, this approach incurs significant latency (or start-up time) [3] as sufficient energy needs to be accumulated to meet the needs of different modules. One of ways to overcome this latency is to eliminate the need for AC-DC conversion, similar to the techniques proposed in [4]- [5]. This approach is illustrated in Fig. 2(b) where the logic gates and communication modules are directly powered by the incoming interrogation signal. The principle is very similar to the well known charge recovery logic [6] and adiabatic dynamic logic [7] where complementary logic computation is performed in each of the respective phases of the AC signal. However, this requires some form of phase and frequency synchronization which is difficult to achieve in practical conditions. Also, this approach does not scale when multiple sources of energy (with different frequency and impedance characteristics) are available.

To overcome the limitations of the conventional and the AC coupled approaches, we present an alternative approach to digital logic design that is more amenable to energy harvesting

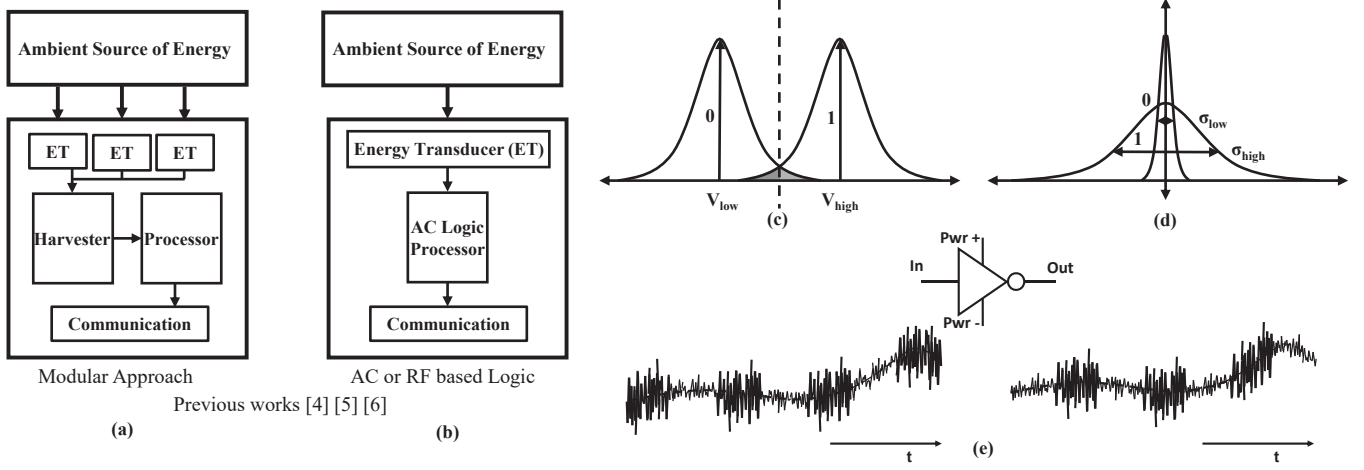


Figure 2. (a) Conventional approach where energy is accumulated before the processor and communication modules are activated; (b) AC/RF based logic where the processor is directly driven by the transducer's AC signal; (c) logic representation for both conventional and AC coupled logic; (d) proposed variance based logic representation; (e) Waveforms of the signal observed at the input and output of an VBL based NOT gate.

systems. The approach uses the statistical variance of the signal instead of the signal's statistical mean to represent different logic levels. The variance-based logic (VBL) representation enables embedding of rectification and multiplication modules within basic digital logic units and unlike AC-coupled or energy-recovery logic circuits the proposed approach obviates the need for any phase synchronization. In section II we introduce the concept of VBL and describe the topology of basic CMOS based VBL circuit. In section III, we verify the functionality of VBL circuits using measured results from fabricated prototypes. Using the basic VBL cells we synthesize a digital state-machine and demonstrate the benefits of the proposed approach in-terms of system latency.

II. VBL BASED DIGITAL CIRCUITS

Conventional energy-harvesting devices use power harvesting circuits to rectify and regulate the available ambient energy in a manner that results in two binary signal levels (V_{high} and V_{low}). These signal levels typically represent the Boolean logic states (denoted by 0 and 1) and is used in the evaluation and representation of different types of digital functions. Because real-world signals are noisy these binary levels are statistically represented by their probability distributions that are centered about their respective means V_{low} and V_{high} , as shown in Fig 2 (c). The variance of each of the distribution captures the effect of noise and signal fluctuations which is a function of the operating environment and applications respectively. In the proposed VBL, as illustrated in Fig 2 (d), logic 0 is represented by a probability density function (PDF) with a small variance (σ_{low}) whereas logic 1 is represented by a PDF with a large variance (σ_{high}). Note that the respective means for both the distributions are the same (shown as 0 in Fig. 2(d)), unlike the conventional representation which is shown in Fig 2 (c). From an energy harvesting point of view, logic 0 (signal with low variance) could correspond to an energy-sink like a ground plane (or a large capacitor), that is readily available

in most systems. Whereas, logic 1 (signal with high variance) could be represented by a random signal with a finite energy, which could be the ambient energy source. Fig 2 (e) shows an example signal representation for a VBL based NOT gate where a bit sequence 1,0,1,0,1 applied to the input. Note that the signal variance (within a finite measurement window) switches according to the bit-sequence, whereas the signal mean (which is unimportant in the proposed representation) could potentially drift. The output of the VBL based NOT gate produces a complementary sequence as represented by the switching of the variance of the signal.

To understand how a variance-based logic can be implemented at a circuit level, consider a generic architecture of any combination logic, as shown in Fig. 3(a). This architecture can be viewed to comprise of a measurement module and a transformation module. The measurement module determines the state of the input signal, which for a conventional logic, would be by measuring the signal mean. For instance, a CMOS implementation of a conventional logic achieves this by averaging the input signal on a capacitor (typically the gate-capacitance of a MOSFET transistor), as shown in Fig. 3(c) for the case of an inverter (Fig. 3 (b)). The transformation module (Fig. 3 (d)) then generates the output signal state by selectively switching the load C_{Load} , to gnd or to V_{dd} through Z_L depending on the measured input state. This is illustrated for a conventional NOT gate, where the switch can be implemented using an NMOS transistor and the load Z_L can be a PMOS transistor. Similarly, for a variance-based logic the measurement module would need to determine the state of the input variance (high or low) using one of several approaches: (a) measure the energy of the input signal; or (b) use a peak detector to track the maximum deviation of the input signal. Fig. 3 (f) shows a simple peak detector stage (formed by the diode D, an NMOS N and a capacitor C_m) that could be used for measuring the variance of the input signal.

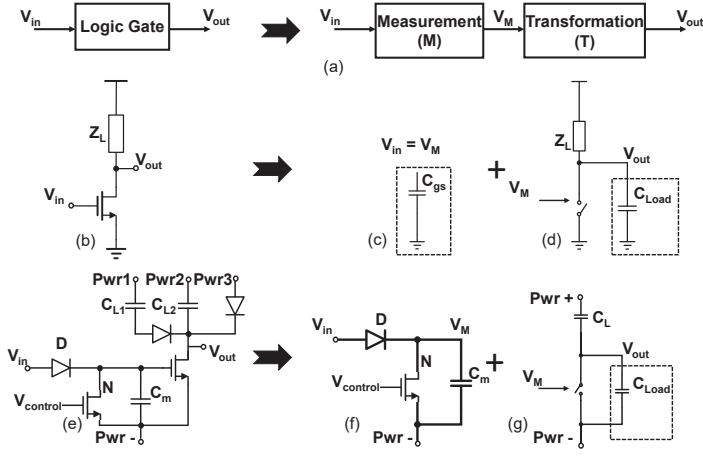


Figure 3. (a) Implementation of a generic logic gate as a combination of measurement and transformation modules. (b) Schematic of a NOT logic gate using a conventional approach – formed using circuit for (c) measuring the signal mean and (d) transforming the output signal based on the mean. (e) Equivalent implementation of a variance-based NOT gate where (f) and (g) show the corresponding variance measurement and transformation modules.

Once the state of input signal variance has been determined, similar to the conventional logic, the transformation module for a variance-based logic can simply couple or decouple the ambient energy source (labeled as $Pwr+$ in Fig. 3 (g)) to the output through a coupling capacitance C_L . A gate controlled NMOS transistor ($=V_{control}$), as shown in Fig. 3 (f), implements a leakage resistance which ensures that the variance measured during the previous cycle is erased before the measurement is repeated. Note that there can be several ways to implement the erase functionality that could yield better performance in terms of speed and energy-efficiency. Fig. 3 (e) shows a general implementation of NOT gate using Variance based logic where the source of power could be any combination of $Pwr1$, $Pwr2$ or $Pwr3$ indicating the operation of gate using multiple coupled sources. In particular, $Pwr2$ could be a primary power source (for e.g. vibration), $Pwr1$ could correspond to a supplementary AC source (strain variations) and $Pwr3$ could be a DC coupled source (for e.g. a solar-cell). Using the basic measurement and transformation circuits shown in Fig. 3 (f)-(g), the proposed variance-based logic could be extended to implement other logic functions like a NOR gate or a D-FlipFlop. Note that the example circuit shown in Fig. 3 (d) implements only a single-ended variant of the variance-based logic where only one of the outputs from an energy transducer is used. Most energy transducers (piezoelectric transducer or an RF antenna) are fully-differential in nature, so a fully-differential implementation would be required to exploit the entire range of signal variance.

III. RESULTS

We have implemented basic VBL based circuits like inverters, ring-oscillators, and NOR logic gates in a $0.5 \mu m$ CMOS process and Fig. 4 shows the micrograph of the fabricated prototype. For the measurement results presented in this section, the value of the leakage resistance (determined by $V_{control}$) and the coupling capacitance C_L were chosen such that the

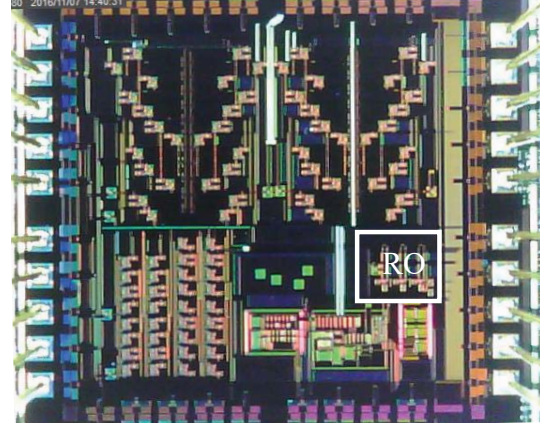


Figure 4. Micrograph of the fabricated chip in a $0.5 \mu m$ CMOS process.

logic circuits could be driven at a desired frequency. The energy source (high-variance source) in all these experiments were emulated using a 100KHz 2V ($=V_{pp}$) source and the logic transitions were generated using square-wave modulation with a frequency of 500 Hz. The measured result corresponding to a NOT gate is shown in Fig. 5 for different values of the leakage resistance (or control-gate voltage $V_{control}$). The results confirm the functionality of VBL based NOT gate where the output variance switches from low to high when the input variance switches from high to low. Also, as shown in Fig. 5, smaller values of the leakage resistance (larger value of $V_{control}$) produces different rise-times (delays). The next set of measurements verified the functionality of a 3-stage ring-oscillator (RO) and Fig. 6 shows the measured oscillation frequency when both $V_{control}$ and the magnitude of the input signal frequency (or input energy) is varied. The measured results show that the output frequency of the VBL based RO is strong function of the input energy (which is expected) and a function of the leakage resistance. Therefore, the RO frequency seems to adjust itself to the available input energy which is really important in energy harvesting systems.

The measured responses from the VBL based logic cells could be used to generate a behavioral model and to synthesize more complex processing units, similar to the conventional logic synthesis approach. In the next set of experiments we used the VBL logic cells to implement a 4-bit Johnson counter that is directly driven by a random energy source. For comparison we implemented an equivalent counter using conventional logic cells and is driven by a power conditioning unit formed by a rectifier and a multiplier. Fig. 7 (a) shows the output waveform (Q0-Q4) of a conventional 4 bit ring counter that is clocked at a frequency of 10KHz and powered by a regulated 3-stage voltage multiplier. The shaded region in the plot of around 2.8 ms duration illustrates the startup latency of the rectifier/multiplier, which is the time taken to reach the steady-state voltage of 3V. For the VBL-based counter, a Gaussian noise-source is used as an input. The corresponding waveforms for each stage of the counter (Q0-Q4) are shown in Fig. 7 (b). The waveforms indicate that VBL based counter

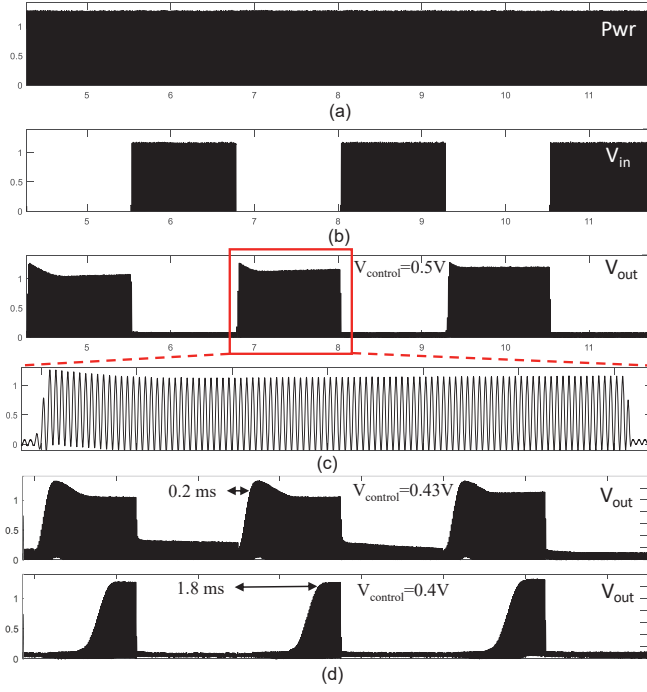


Figure 5. (a) Power source (Pwr), (b) Input signal (V_{in}) and (c)-(d) Measured output response of a VBL-based NOT gate for different values of $V_{control}$.

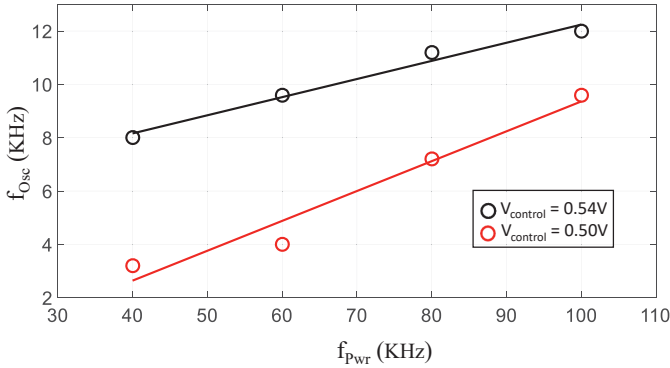


Figure 6. Measured oscillation frequency of a 3-stage VBL ring oscillator when the frequency of power source is varied from 40 KHz to 100 KHz.

demonstrates a latency of 50 μs and completes two cycles of operation by the end of 0.8 ms. This result clearly shows the advantage of the proposed VBL-based digital circuits to design low-latency digital circuits. This attribute would be important for designing real-time wireless interrogation circuits for IoTs.

IV. CONCLUSION

This paper provides an alternate and novel approach for building logic gates that operate on the statistical variance of the input signal, which we call variance-based logic. The approach could potentially combine the functionalities of energy harvesting and digital computation and the approach could be applied to a wide variety of energy transducers. With help of prototype, we have demonstrated the performance of basic digital cells and proposed the feasibility of a simple state machine. The advantage of this new logic design in

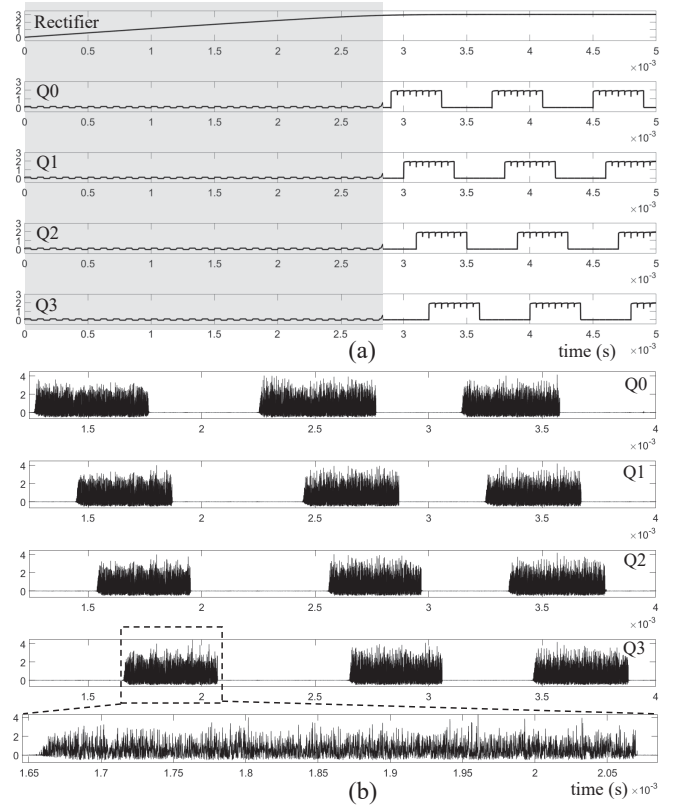


Figure 7. Simulation results of a 4 bit johnson counter using: (a) conventional logic gates; and (b) using VBL based gates.

terms of power and delay, when compared to the conventional logic gates, is unknown and is the subject of future research in this area. Another benefit of using variance-based logic is that the reciprocity of the energy transducer (like an RF antenna) which can be used to wirelessly transmit logic-state information. In fact, variance-based logic shares similarity with load-modulation techniques that are commonly used in back-telemetry for passive RFIDs.

V. ACKNOWLEDGEMENT

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