Photoemission studies of biased metal-insulator-semiconductor structures

Malathi Kalyanikar and Eric Garfunkel
Department of Chemistry and Chemical Biology, Rutgers University, 610 Taylor Road, Piscataway, New Jersey 08854, USA

Sylvie Rangan, Junxi Duan, Robert Allen Bartynski, and Eva Andrei
Department of Physics and Astronomy, and Laboratory for Surface Modification, Rutgers University, 136 Frelinghuysen Road, Piscataway, New Jersey 08854, USA

Gang Liu and Leonard Feldman
Institute for Advanced Materials, Devices and Nanotechnology, Rutgers University, 607 Taylor Road, Piscataway, New Jersey 08854, USA
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X-ray photoemission is performed on a biased graphene/SiO_2(6 nm)/Si structure in order to experimentally determine the potential profile across the three layer stack. Si 2p, O 1s and C 1s core levels provide a measure of the local potential and are used to reconstruct the potential profile as a function of the depth of the photoemitting atom. It is found that the simplest potential profile able to describe the experimental data is a linear potential drop across the oxide, with offsets at each interface. The offset at the SiO_2-Si interface relates to the band bending developed in the Si substrate under the different biasing conditions. The graphene-SiO_2 interface potential offset, may result from polarization of trapped water or other polar species at the interface.

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I. INTRODUCTION

Understanding the electronic structure across multilayered systems is of crucial importance for the development of novel technologies. The band energy alignment at interfaces, often a measure of energy barrier for carriers, as well as the behavior of the energy bands across the different layers need to be determined, in particular when an extrinsic potential is applied across the system. This becomes particularly complex when defects, either interfacial or embedded into the bulk materials, fixed or mobile, neutral or charged, complicate the overall picture.

An example of a technologically relevant system is the field effect transistor (FET) in which a biased metal/oxide/semiconductor (MOS) stack controls the current flow between a source and a drain. At the heart of the device, the gate insulator plays a crucial role in sustaining the applied gate voltage across the MOS structure. The gate insulator must also establish a sufficient barrier, preferably greater than 1.5 eV, preventing electron and hole transport across the dielectric, even when the MOS structure is biased. With the drive to continuously scale devices and improve performance[1], a range of challenges are faced in terms of device architecture and of materials selection for the insulator[2,3]. Over the past decade, and amongst multiple transformations, high-k dielectrics have supplanted the traditional SiO_2 insulating gate in Si-based CMOS, allowing effective oxide thickness scaling to less than one nanometer. At these dimensions, control of the electronic structure within one nanometer of the interface has been central to performance. At another end of the materials spectrum, graphene (Gr) and organics have been competing with, and in some cases replacing inorganics in emerging applications such as light emitting diodes (OLEDs)[4,5] and organic photovoltaics (OPV)[6,7]. Here again, interface electronic structure is often central in regulating ultimate device performance.

The potential profile across organic or inorganic dielectric materials under an electric field, is traditionally described using a knowledge of the permittivity of the material. Unfortunately, accurate measurements of the potential profile across highly scaled systems, especially when working at the sub-10nm scale where interface properties and defect densities may be significant, are almost nonexistent. Such knowledge, combined with careful measurements of band offsets and alignment, are key to developing a full understanding of both electronic structure and device performance, and will remain essential as we try to develop new nanoscale technologies. In this paper, inspired by several decades of x-ray photoemission (XPS) -based techniques, a new method to probe the local potential across a biased multilayer system is proposed.

Studies of ultrathin dielectrics on semiconductors are routinely performed using surface sensitive techniques such as XPS. In XPS, the relatively short inelastic mean free path of the ejected photoelectrons results in useful information coming from the top 10 nm of a film. Lau et al, developed a form of surface charge spectroscopy several decades ago on oxide-semiconductor systems[8]. In these experiments, by exposing the dielectric surface to a constant flow of either electrons or x-rays, both positive and negative charging of a dielectric grown on a semiconductor could be achieved. The experimentally determined photoemission intensities, including broadening and peak shifts, were modeled, via some basic as-

sumptions, semiconductor band bending, potential profile across the oxide and possibly defects states.[8–13] Cohen and coworkers have extended the application of flood gun charging strategies to a wider class of interfaces using the phrase chemically resolved electrical measurements, to describe their modified method. Notable systems studied using this technique were self assembled organic monolayers on Au surfaces[14], SiO_2 and SiON grown on Si substrates[15,16], and more recently SiO_2 on a 4H-SiC substrate[17]. In the same category of experiments, Suzer et al. in addition to performing extensive work on defects and charging effects in oxides using XPS (but without external surface charging)[18–23], have also recently explored the in-plane surface potential variations using XPS imaging on in-plane biased structures[24–26]. Kobayashi et al. have physically applied a bias across a MOS stacks using 3 nm Pt films as top electrodes and performed XPS in order to determine the oxide defects density from substrates band bending evolution.[27–29] In their work, the determination of the potential profile across the stack was not performed. Lastly, recent work pertaining to the study of semiconductor-electrolyte interface in photoelectrochemical (PEC) cells was carried out using operando ambient-pressure XPS methodology[30,31]. Their work utilizes a high energy x-ray synchrotron source to probe the interfaces both within a multilayer solid system and between solid and a thin liquid electrolyte, by analyzing the potential profile across the system.

Our work, inspired in part by these prior biased-XPS studies, consists of performing XPS while fully controlling the gate voltage by using a graphene top electrode added to an oxide-semiconductor sample. Although thin Pt films have been used as top electrode in earlier studies[27], non-negligible Pt XPS peak intensity overlaps with Si 2p, preventing the crucial fine analysis of the Si 2p peak shape required in this work. Graphene has the advantage of providing a very good electrical contact that enables a uniform potential to be directly applied to the surface[32], allowing us to probe the graphene, SiO_2, and first few nanometers of the substrate Si in the MOS stack while averaging over the sample area. As a proof of concept, we have selected the well-known SiO_2-Si system to test the viability of our approach, as illustrated in Fig.1.

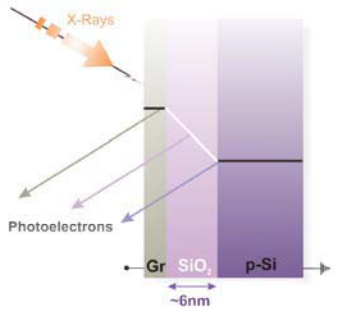

FIG. 1: A graphene-SiO_2-Si stack is biased during x-ray photoemission experiments. The graphene top electrode ensures a uniform and readily quantifiable potential to be applied to the surface, while enabling photoelectrons emitted from the SiO_2 and Si substrate to be detected.

II. EXPERIMENTAL METHODS

A. Sample preparation

In the simple MOS structure used in this study, an SiO_2/Si base structure was first prepared before adding the top contact (graphene). This oxide-substrate base consisted of a large thick (300 nm) pad oxide area, and a smaller thin (6 nm) oxide trench located within the thicker pad oxide. The thicker pad oxide region enables one to observe (in an optical microscope) the graphene layer once placed on top of the structure, and it also acts as an electrical buffer layer where electrodes can be placed. Once the graphene is placed on the substrate, gold electrodes was deposited on the graphene over the thicker pad oxide area, which is then connected electrically to an external contact for biasing and/or current measurements.

A commercially purchased degenerately doped (resistivity<0.005 ohm/cm - 10^{19} doping level) p-type Si(100) wafer is cleaned by the RCA method to remove the thin native oxide layer (RCA reference) followed by the growth of a 300 nm oxide using conventional wet-thermal oxidation. A circular window approximately 400 μm in diameter was then lithographically patterned and the SiO_2 in the patterned area was removed by wet etching. A fresh 6 nm thermal oxide layer was grown on the lithographically exposed Si in a dry oxygen atmosphere at 900°C for 3 minutes.

Graphene, CVD-grown on copper, was prepared using a procedure previously been reported[33,34] A thin layer of poly-methyl-methacrylate (PMMA) was spin-coated on the graphene-copper substrate and the substrate copper was etched away. The polymer layer was then used to transfer the graphene onto the patterned SiO_2/Si substrate and the sample was annealed to enhance the graphene conformality on the oxide structures. After a chemical wash in acetone, most of the residual polymer was removed by annealing in a forming gas (H_2-Ar) atmosphere at 350°C. For contact purposes, a thin layer of Ti (5 nm) followed by a thicker layer of Au (45 nm) was deposited on the graphene using e-beam sources. Complementary optical measurements and Raman spectroscopy were used to characterize the graphene on control samples.

B. Electrical measurements

To ensure that the patterned ultrathin oxide was of high quality and that the MOS structure was not shorted, current-voltage ($I-V$) studies were performed on control samples prepared in the same batch, and used to confirm

leakage current and breakdown voltage of the thin oxide. The leakage current observed across the dielectric when measured both in-vacuo (during XPS) and under atmosphere conditions was in the range of few nano-amperes (for an area of 1.25 x 10^{-7} m^2). The bias range was restricted during the XPS measurements on the real sample to ±2.7V to avoid possible breakdown of the dielectric.

C. Biased x-ray photoemission

The XPS biasing experiments were preformed in a Thermo Scientific ESCA 250Xi system, equipped with a monochromated Al Kα x-ray source (hν = 1486.7 eV). XPS results were collected from an area of about 200μm×200μm. In the studies reported here, the bottom of the Si substrate was grounded to the chamber and the bias was applied to the top graphene electrode via an external power supply. Multiple measurements across the biasing range were performed to ensure reproducibility of the results and to assess the error. Spectra were collected at several positions on the sample to confirm lateral bias homogeneity. Intensity variations of the x-ray source were taken into account by normalizing all photoemission peaks to the graphene C 1s signal. The gold electrode present in the sample was utilized as an internal reference for the binding energies (Au $4f_{7/2}$ and Au $4f_{5/2}$ doublets were located at 84.0 eV and 87.7 eV, respectively).

III. RESULTS AND DISCUSSION

A. Flatband potential and prerequisite definitions

Before offering a detailed analysis of the biased XPS experimental results, we define some basic concepts that will be referred to in this work.

The system under study, Gr/SiO_2/Si, will be considered as a simple MOS capacitor stack with the overlayer, graphene, acting as a ultrathin metallic electrode. The conventional representation of potential profiles across MOS stacks under different bias conditions is summarized in Fig. 2. In this representation, the p-doped silicon base is kept at ground potential and a bias V_g is applied to the metal gate (graphene), controlling the position of the Fermi level in the metal and the potential drop across the oxide-semiconductor system. As most MOS stacks are not ideal (in the sense that the Fermi levels of the isolated metal and semiconductor materials and the charge neutrality level of the dielectric are not exactly the same), an intrinsic non-zero potential profile across the stack is always present, even when no bias is applied. A small bias (termed the flatband volatage V_{fb}) is required to move the system into a flatband condition ($V_{fb} \neq 0$ at V_g=0) for most "real" systems. As shown in Fig. 2, at the flatband voltage there should ideally be no potential drop across the oxide layer and no band bending in the silicon. With a decrease in the gate voltage ($V_g < V_{fb}$ for the structure described in the figure) the system shifts to what is called the accumulation regime where the majority carriers (holes from Si) are attracted towards the negative electrode. The application of a bias attracts the majority carriers in this highly doped system to an extent such that most of the potential drop is expected to occur in the oxide layer. For $V_g > V_{fb}$, the reverse trend is seen, with the movement of the majority carriers away from the direction of bias (the depletion regime). Here the potential drop may be observed across both the oxide and the silicon substrate (in the form of band bending in the Si near the SiO_2-Si interface), as there are few carriers in the Si when biased in the depletion regime.

In order to understand the outcome of a biased photoemission experiment, a uniform series of slabs can be used to help model the photoemission signal originating from the oxide. In this "slab model", the total oxide thickness t is divided into a series of n slabs of equal thickness (d=t/n), parallel to the surface. Each slab contributes to the total photoemission peak I(E) by its intensity $I_n(E)$, such that:

$$I(E) = \sum_n I_n(E) = \sum_n I_0(E - \Delta_n) e^{-\frac{nd}{\lambda}} \qquad (1)$$

where $I_0(E)$ is the photoemission peak intensity originating from the topmost slab, Δ_n is the energy shift caused by the local potential in a given slab, d is the thickness of a slab, and λ is the attenuation length of photoelectrons in the oxide layer. In such a model, the total photoemission contribution from the oxide is obtained as the sum of I_n over the thickness of the oxide. Therefore, it is expected that applying a bias across the oxide should both shift and broaden the photoemission peak without altering the total area under the peak.

The attenuation lengths into SiO_2 have been calculated using the NIST electron effective attenuation-length database software[35], for an Al-Kα photon source and a density of 2.3 gcm^{-3}. The values obtained for electrons originating from the Si 2p and O 1s core levels, 35.3 Å and 25.7 Å, respectively, are comparable to most recent studies.[36] An oxide thickness of 60 Å is calculated from the ratio of the Si^{4+} and Si^0 photoemission intensities.

In order to determine I_0(E), one must obtain the shape and position of the oxide photoemission peaks, unperturbed by the presence of potential variations across the oxide layer. This situation corresponds to the flatband condition, and is experimentally accessible and determined for our system. The applied bias on our system was tuned until it reached the smallest FWHM for the oxide peaks.[30,37] This occurs when the system is in the flatband condition, which for our system was found to result when V_g =-0.6 eV.

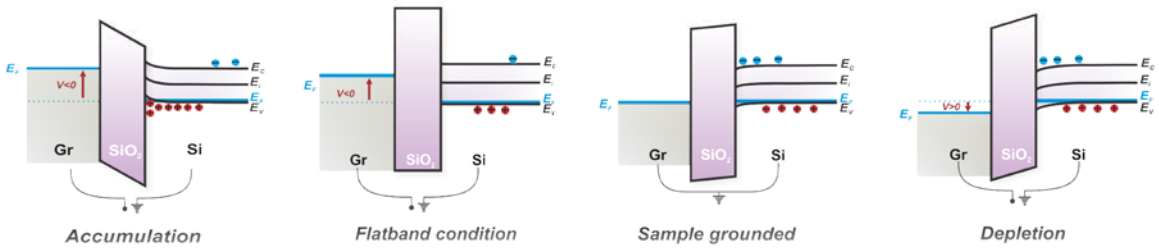

FIG. 2: Different bias regimes and their corresponding band energy diagrams.

B. Biased photoemission results

A central requirement for this experiment is the ability to apply a uniform and well-defined bias across the $Gr/SiO_2/Si$ stack. In a configuration where the silicon substrate is grounded (V=0), the Gr electrode holds the full potential supplied by the external voltage source. Since the Gr electrode is the dominant source of carbon in the system, the effective bias can be measured by following the C 1s carbon levels as shown in Fig. 3. At the flatband voltage, i.e. when a -0.6 V is applied to the graphene electrode, the maximum of the carbon peak is found at a binding energy of 284.1 eV. When biases of -2.7 V and +2.7 V are applied, the C 1s peak rigidly shifts by 2.0 V toward lower binding energies and 3.3 eV toward higher binding energies, respectively, as expected. Therefore, monitoring the carbon peak position is a viable and accurate (within 0.1 V) method to determine the top electrode potential, and agrees well with the externally applied voltage. We also note that biasing does not alter the shape of the C 1s peak, indicating that the top electrode (which may contain some carbon other than graphene such as residual polymer or adventitious carbon) is at the same potential.

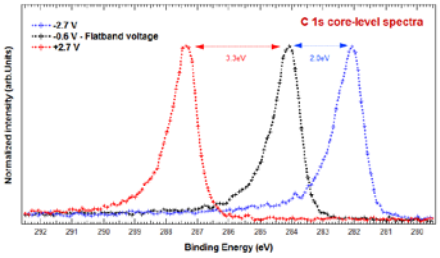

FIG. 3: C 1s core level spectra measured for three biasing conditions: -2.7 eV, -0.6 eV and +2.7 eV.

The situation is more complex when analyzing the O 1s core level. Although most of the O is located in the SiO_2 layer, a small component (<5%) of the oxygen peak can be attributed to adsorbed species at the surface of either the SiO_2 layer or the top Gr electrode. At flatband, the O 1s peak is nearly-symmetric and centered around 532.7 eV as shown in Fig. 4. When a -2.7 eV bias is applied, the O 1s peak broadens and changes shape, and the position of the most intense part of the peak shifts approximately 1.4 eV toward lower binding energies. When a +2.7 V bias is applied, the O 1s peak broadens in the other direction and shifts 2.5 eV toward higher binding energies. Here the observed shifts are not equal to the bias difference seen by the top Gr electrode, as the final peak position is the result of a weighted sum of O 1s peaks at different positions in the film, each with its own local potential, less than that of the graphene electrode. Nevertheless, the integrated area under each O 1s peak is constant, as expected in equation 1.

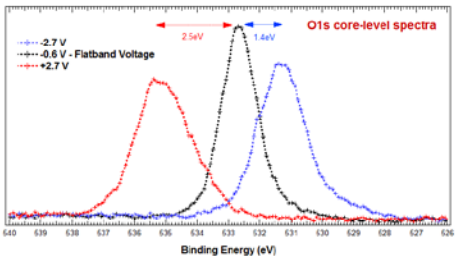

FIG. 4: O 1s core level spectra measured for three biasing conditions: -2.7 eV, -0.6 eV and +2.7 eV.

The behavior of the Si 2p core level peak region is shown in Fig. 5. The Si 2p core level spectra contains information pertaining to both the oxide (Si^{4+} oxidation state) and the silicon substrate (Si^0 oxidation state), as well as a small contribution from suboxides at the interface. The Si 2p peak consists of a symmetrical doublet (Si $2p_{3/2}$ and Si $2p_{1/2}$ with a separation of 0.63 eV); this splitting is visible (without peak fitting) in the substrate Si 2p peak although it is not immediately apparent in the Si^{4+} peak. At flatband voltage, the Si $2p_{3/2}$ component for the oxide and for the bulk silicon are found at 103.2 eV and 98.9 eV, respectively. Here, the oxide-related Si peaks clearly follow the qualitative trends observed for the O 1s oxide peak as a function of applied bias. The Si^0 peak is also modified upon biasing, although to a much less extent, as it is electrically held closer to the grounded sample. A small 0.1 eV shift toward lower binding energies is measured upon application of a -2.7 V bias, while a larger 0.6 eV shift toward higher binding energies is measured when applying +2.7 V, concurrent with visible broadening.

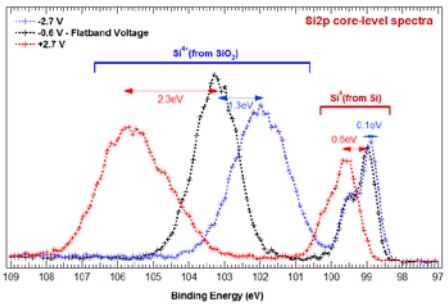

FIG. 5: Si 2p core level spectra measured for three biasing conditions: -2.7 eV, -0.6 eV and +2.7 eV.

Similar sets of XPS spectra have been acquired for different biasing conditions. A summary of the core level peak maxima shifts is reported in Fig. 6. A "relative" applied bias scale has been defined and referenced to the flatband voltage condition (redefining the zero voltage; V=0 at the flatband voltage). A line of slope 1 has been added as an aid to visualize the ideal potential shift that should be seen by the top electrode. It is first clear from this data set that the Gr electrode behaves as a metallic electrode, shifting exactly as it should, within experimental error. Additionally, both the oxide O 1s and Si 2p core levels also shift, although to a lesser extent, as discussed above. Finally, the substrate Si 2p peak does shift, although much less than the other peaks, indicating band bending in the Si substrate.

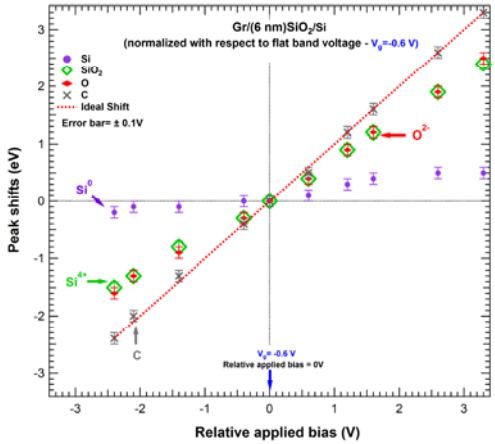

FIG. 6: Summary of the peak maxima shifts measured as a function of the relative applied bias (with respect to flatband condition set at 0 V).

These results can be qualitatively understood in the framework of conventional MOS capacitor behavior, Fig. 2. Using the flatband condition ($V_g = V_{fb}$ =-0.6 V) as a reference point, one can begin to understand the MOS potential profile when in the accumulation ($V_g < V_{fb}$) and depletion ($V_g > V_{fb}$) regimes. (Note that the inversion regime is typically attained only for larger applied biases for such samples) In particular, we observe that the band bending in the silicon substrate is more prominent in the depletion regime, a result of the larger energy swing possible in the gap while in depletion before inversion essentially fixes the maximum potential swing. At its maximum (which occurs before 2.7V), a shift of about 0.6 eV toward higher binding energies is measured for the Si^0 component of the Si 2p core level, and a broadening of the photoemission peak is observed. This broadening, although typically not observed for medium-doped Si substrates, is due to the high doping level of our substrate, therefore leading to a severe narrowing of the depletion width in the silicon substrate.[38–40] The extent and magnitude of the band bending into the silicon substrate for both positive and negative biases are comparable to recent experimental and theoretical studies of band bending measured using scanning tunnel microscopy and spectroscopy.[41,42]

Before addressing in more detail the potential profile determination across the stack, a few points regarding the method need to be mentioned. First, when measuring insulating films using photoemission, charging effects due to the creation of positive charges upon ionization need to be evaluated. In our case, as the oxide layer is connected to two conductive electrodes (Si and Gr), the effective length for charge extraction from the oxide layer is only 3 nm, thus greatly reducing charging.[43] Charging also depends on photon flux and might be time-dependent until a dynamic equilibrium is reached. In our case, no x-ray flux- or time- dependence was measurable, attributed to minimal charging for our structure.

C. Potential profile determination

In order to extract the potential profile across the MOS structure from our photoemission data set, a more quantitative analysis is needed. As a first approximation, we assume that the potential profile in the SiO_2 between the two electrodes, Gr and Si, is perfectly linear, as represented in the top part of Fig. 7(a). Using the equation 1, and using the Si 2p photoemission peak at flatband condition as reference, a simulated spectrum summing all I_n contributions over the SiO_2 thickness with a slab thickness of 1Å, is shown at the bottom of Fig. 7(a), superimposed over our experimental data obtained for an applied bias of +2.7 V. Although the general trends are correct, there are clear discrepancies between this model and the experimental spectra. More realistic models should consider non-linear potential gradients across the dielectric, especially very close to the interface where the permittivity might not be equivalent to the bulk value, as well as the possible presence of interface dipoles at both the Gr-SiO_2 and SiO_2-Si interfaces. We then explored a second level model which permits potential discontinuities at both interfaces, as illustrated in the top part of Fig. 7(b). The potential discontinuities, in essence, are dipoles located at the interfaces, which can be de-

V_g	Gr-SiO_2 offset	SiO_2-Si offset	Measured Si^0 peak shift
-3.0	-0.3	-0.3	-0.2
-2.7	-0.3	-0.2	-0.1
-2.0	-0.2	-0.1	-0.1
-1.0	0.0	0.0	0.0
-0.6	0.0	0.0	0.0
0.0	0.0	0.0	+0.1
+0.6	+0.1	+0.4	+0.3
+1.0	+0.1	+0.4	+0.4
+1.5	+0.2	+0.6	+0.5
+2.0	+0.1	+0.6	+0.5
+2.7	+0.2	+0.6	+0.5

TABLE I: Gate bias V_g, calculated bias offsets at the Gr-SiO_2 and SiO_2-Si interfaces and measured shift of the silicon substrate Si $2p_{3/2}$ peak.

termined via a χ^2 fitting procedure of our experimental data. An example of such a model spectrum for the Si 2p peak of the oxide is shown in the bottom part of Fig. 7(b). Under these simple assumptions, the result of the fit is surprisingly good.

Using the same assumptions, the potential offsets at both interfaces have been calculated from our data sets for different applied V_g and are reported in Table I. Additionally, the measured Si $2p_{3/2}$ peak shift of Si^0 is reported as a reference for the relative amount of band bending in Si, as a function of V_g.

The first noticeable characteristic of the offsets is that they are not constant as a function of the applied bias. In the case of the SiO_2-Si interface, this can be easily understood by realizing that the calculated offset closely follows the experimentally measured Si substrate peak shift of Table I. This indicates that the potential drop at this interface is directly related to the band bending in the substrate.

The situation is more complex at the Gr-SiO_2 interface. As both the relative intensity and the direction of the offset follow the applied bias, it is possible that something forming an effective dipole at the Gr-SiO_2 interface could be responsible for such behavior. Recent studies point to the presence of water at the Gr-SiO_2 interface for preparation conditions similar to ours[44], where either CVD-grown graphene is deposited onto SiO_2 in atmospheric conditions using solution-based process, or where graphene is prepared via exfoliation[45–47]. Although annealing can help removing some interface adsorbates, some may still become trapped at the interface. If the impurity species is polar or very polarizable, (water has the highest dielectric constant for any solvent) they can contribute significantly to an interface offset[45]. When placed in an applied potential, higher permittivity molecular species trapped at the interface can rotate or reorganize, resulting in an interface dipole that changes with field strength and orientation.

In order to establish a scale for the value of such interface dipole, we can consider the extreme case of a surface fully covered with water molecules in which the dipoles are all aligned perpendicularly to the surface plane. Considering for water a dipole D=1.84 Debye and a molecular diameter $\delta \sim 3$ Å, the interface dipole can be estimated from a planar capacitor formula as $\Delta V = D/\epsilon_0 \times \mathrm{A}$, where A is the footprint of a molecule ($\mathrm{A}=\pi(\delta/2)^2$) and ϵ_0 is the vacuum permittivity, to 9.8 V. This is obviously an unrealistic value as the water coverage may be smaller and the dipoles will likely not all orient favorably, but this gives some credibility to the role of polar adsorbates as one explanation for interface dipoles of the order of 0.3 eV. In this picture, as illustrated in Fig. 8, larger biases would tend to orient a larger number of adsorbates, creating a dipole in the opposite direction to the applied bias.

Overall, the information accessed using biased XPS on our Gr/SiO_2/Si sample can be summarized as follows. The results obtained for our bias range are in good agreement with the band diagram model of Fig. 2. Above and below the experimentally measured flatband voltage, accumulation and depletion modes can be probed using XPS. Assuming a linear potential drop across the oxide layer with bias-dependent potential drops at both the Gr-SiO_2 and SiO_2-Si interfaces can reproduce the experimental broadening and energies of all photoemission peaks under biasing conditions.

IV. CONCLUSION

In summary, we have performed a biased-XPS experiment in which the gate bias is fully controlled, to investigate the electrostatic potential profile across a Gr-SiO_2-Si stack. The shifts in binding energies of electrons photoemitted from different physical positions (in depth) in this structure as a function of external bias provides a unique method to follow changes in potential across the dielectric. A detailed analysis of the shape of the C 1s, O 1s and Si 2p core level spectra, indicates that the simplest potential profile able to describe the experimental data is a linear potential drop across the oxide, with offsets at each interface. The offset at the SiO_2-Si interface is simply related to the band bending developed in the Si substrate under the different biasing conditions, thereby depicting the amount of potential distribution across the oxide-semiconductor region. A qualitative understanding of the graphene-SiO_2 interface potential offset, in the studied bias range, can possibly be related to the polarization of the trapped water and other molecular species at the interface.

It is notable that thermally grown oxides provide the best SiO_2/Si interface qualities with reported defects densities as low as 10^9 cm^{-2}. Other technologically relevant oxides such as high-k dielectrics typically display higher defect densities inhomogeneously distributed in the oxide, possibly resulting in a non-linear potential drop across the dielectric. Using a Gr electrode as a top contact in biased-XPS measurements is shown to be a powerful tool to ultrathin heterostructures and their

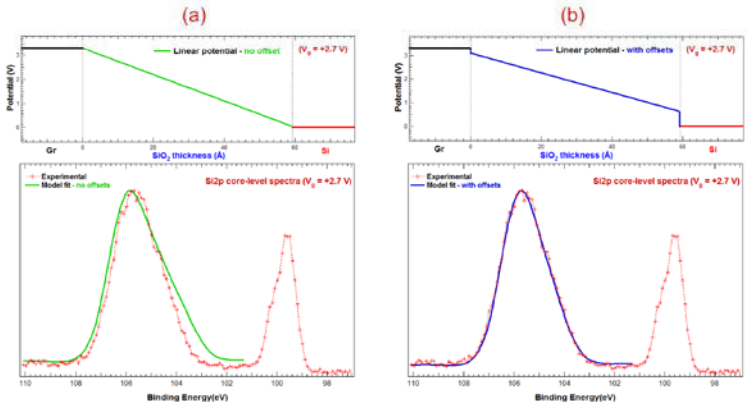

FIG. 7: Models for the potential profile determination across the Gr-SiO_2-Si structure. a) A model with asimple linear potential profile in the dielectric does not result in a convincing simulation of the experimental biased-XPS data. b) When potential offsets at each interfaces are added to a linear potential drop across the dielectric, the simulated spectrum follows the biased-XPS data quite accurately.

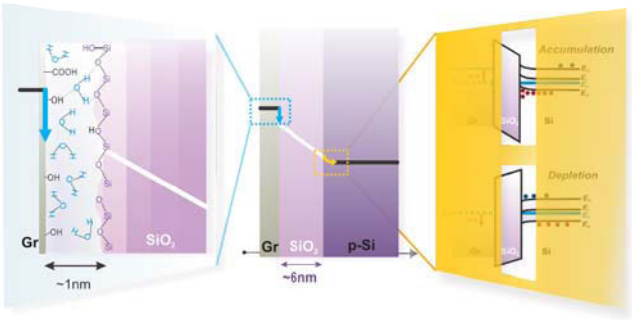

FIG. 8: Potential profile picture obtained from the biased-XPS measurements. A linear potential drop exists across the dielectric, while two interface potential offsets are found related to band bending in the silicon and existing dipoles at the Gr-SiO_2 interface.

interfaces. As opposed to a simple energy alignment picture of the electronic bands without applied bias, here the response of the system to an applied bias could allow a better characterization of interfacial species, ultimately improving the performance of existing devices, or help lead to the design of new ones.

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