Doped Organic Transistors -

Increased Stability and Reproducibility for Active Matrix Displays†

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Abstract

Doping Organic Field-Effect Transistors (OFETs) is increasingly accepted as a means to increase their performance and stability, in particular for AM displays. A theory of doped depletion type OFETs is presented. The benefits of channel doping are discussed, in particular in terms of a reduction of gate bias stress effects.

Author Keywords

Organic Field-Effect Transistors; Organic Doping; Stability; Gate Bias Stress

1. Objectives and Background

Recent progress in the design of organic semiconductors resulting in charge carrier mobilities close to or even exceeding 10 cm^2/Vs has renewed interest in exploring the use of organic field-effect transistors (OFETs) as transistors elements in optical displays [1], [2]. In addition to the display market, OFETs are seen as a key technology for flexible and smart sensor systems [3], or more generally for low-cost printed electronic systems [4]. Furthermore, the organic electrochemical transistor [5], which can be seen as a doped organic depletion transistor as well [6], acts as an ion to electron transducer that is heavily discussed for its use in the field of organic bio-electronics [7].

However, a major concern for the use of organic transistors in larger integrated circuits is their large spread in device parameters, e.g. in their threshold voltage or transconductance, and a continuous shift in their transfer characteristic due to gate-bias stress. Following the example of inorganic transistors, these drawbacks can be abated by doping the organic semiconductor [8], [9]. Doping fills trap states deep in the HOMO/LUMO gap of the organic semiconductor [10], rendering them inactive during normal operation of the transistor and hence increasing the stability of OFETs [11], [12].

Despite these advances in OFET technology due to organic doping, an analytical model describing doped transistors is missing. Often, as a first approximation, doped transistors are described as either operating in the depletion mode or in accumulation mode [9], depending on the applied gate and drain voltages. However, this treatment neglects that under realistic operation conditions the doped transistor channel is both, depleted close to the drain electrode, whereas excess charge carriers are accumulated close to the source electrode.

In the following, a closed analytical solution of doped organic depletion transistors is presented. The model is tested by systematic, temperature dependent data. The influence of doping on device stability is discussed as well.

2. Results

Analytical Model: The general setup of a p-type organic depletion FET is shown in Figure 1a [9]. In contrast to intrinsic, i.e. undoped OFETs, doped organic layers are included underneath the source and drain contact and at the organic semiconductor/gate oxide interface. Not only do the doped layers underneath the source and drain contacts ensure the formation of a quasi-ohmic contact and hence a reduction in the contact resistance [13], [14], but the doped layer in the channel region has as well a significant influence on device operation.

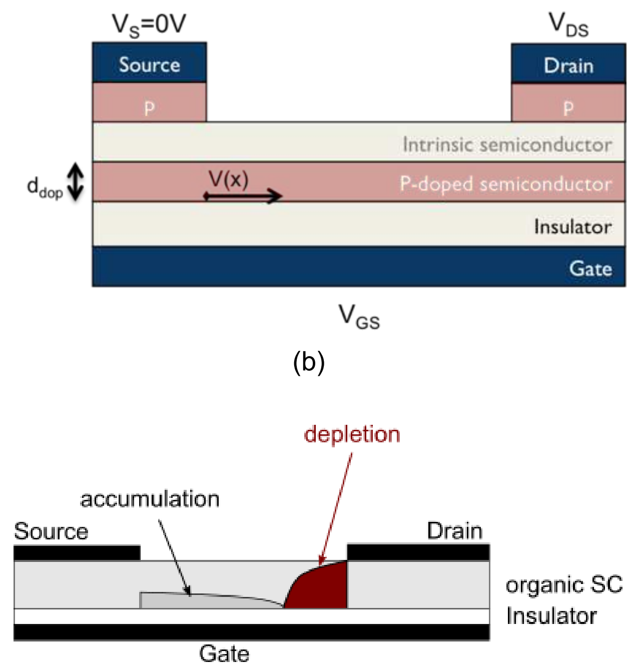


Figure 1: (a) General setup of a doped organic transistor. Doping the channel of the transistor leads to a precise control of the threshold voltage and an increase in device stability. **(b)** Charge carrier distribution inside the channel of a doped transistor at saturation. Close to the source, charge is accumulated, whereas the doped channel is depleted close to the drain.

In order to describe the influence of channel doping analytically, the hole density $p(x,y)$ in the transistor channel can be written as

$$p(x,y) = -\frac{1}{e}C_i\big(V_{GS} - V_{FB} - V(x)\big)\delta(y) + N_A(y) \qquad \text{(Eq. 1)}$$

(d: thickness of transistor channel, V_{FB}: flatband voltage of the MIS capacitance of the transistor, e: elementary charge, C_i: gate capacitance per unit area, $\delta(y)$: Dirac Delta function, $N_A(y) = N_A$ for $0 \leq y \leq d_{dop}$, and d_{dop}: thickness of the doped layer).

In the linear regime, the drift equation $I_D = we\int_0^\infty p\mu_p E_x dy$ has to be integrated from the source at $x = 0$ to the drain at $x = L$ to obtain the drain current I_D (w: width of the transistor, μ_p: hole mobility, E_x: x-component of the electric field):

$$-\int_0^L I_D dx = \mu_p w C_i \int_0^{V_{DS}} -V_{GS} + V_{FB} + V(x) + \frac{d_{dop} e N_A}{C_i} dV \quad \text{(Eq. 2)}$$

which yields

$$I_D = \frac{\mu_p w}{L} C_i \left\{ -(V_{GS} - V_{th})V_D + \frac{V_{DS}^2}{2} \right\}$$

with the threshold voltage $V_{th} = V_{FB} + \frac{e\, d_{dop} N_A}{C_i}$. In fact, this relation between doping concentration, thickness of the doped layer and threshold voltage is often observed experimentally [2], [9], [15].

In the saturation regime, the discussion of the charge distribution becomes more complex (cf. Figure 1b). In contrast to the linear regime, the transistor channel of a doped transistor operates in the accumulation regime close to the source electrode (where the potential drop across the gate insulator $\Delta V = V_{GS} - V(x)$ is negative, cf. Figure 1a), and in the depletion regime close to the drain electrode (where ΔV is positive).

To describe this behavior, the integral shown in Equation 2 has to be adapted [16]:

$$I_{D,sat} = \frac{\mu_p w C_i}{L} \int_0^{V_{GS}-V_{FB}} -V_{GS} + V_{th} + V(x) dV + \frac{\mu_p w}{L} e N_A \int_{V_{GS}-V_{FB}}^{V_{DS,sat}} \left(d_{dop} - d_{dep}(x)\right) dx \quad \text{(Eq. 3)}$$

In Equation 3, d_{dep} denotes the thickness of the depletion layer, which is given by [9]

$$d_{dep}(x) = \frac{\epsilon_s}{C_i} \left\{ \sqrt{1 + \frac{2C_i^2 (V_{GS} - V_{FB} - V(x))}{e N_A \epsilon_s}} - 1 \right\} \quad \text{(Eq. 4)}$$

(ϵ_s: dielectric constant of the organic semiconductor). Combining Equation 3 and 4 leads to the dependence of the saturation $I_{D,sat}$ current on the gate-source voltage V_{GS}, the thickness of the doped layer d_{dop} and the doping concentration N_A:

$$I_{D,sat} = -\frac{\mu_p w C_i}{2L} \left[(V_{GS} - V_{th})^2 + \frac{2}{3} \frac{e d_{dop} N_A}{C_i} \cdot (V_{PO} - V_{th}) \right] \quad \text{(Eq. 5)}$$

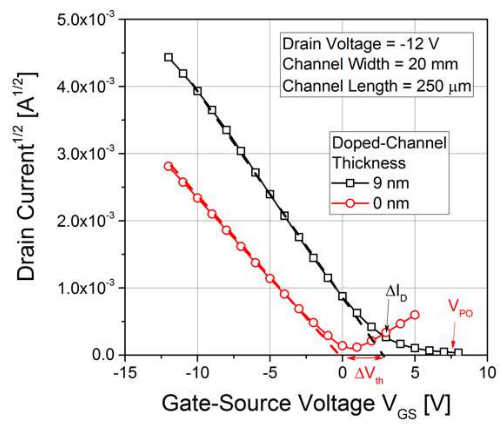
In Equation 5, V_{PO} is the pinch-off voltage, given by ($C_s = \frac{\epsilon_s}{d_{dop}}$)

$$V_{PO} = \frac{e N_A d_{dop}}{2 C_s} + V_{th} \quad \text{(Eq. 6)}$$

Equation 6 shows that the IV characteristic of a doped transistor resembles the characteristic of an intrinsic transistor (first term in Equation 6), but is corrected for an additional, constant term that is caused by the conduction through the doped layer (second term in Equation 6). Furthermore, the shift of the threshold voltage with the doping concentration is identical to the shift observed in the linear regime.

Experimental Verification: The model discussed above predicts that the transfer characteristic of a doped transistor strongly depends on the thickness of the doped layer d_{dop}. Indeed, Figure 2 confirms the general trends of the model. In Figure 2a, the transfer characteristic of an intrinsic transistor and a doped transistor ($d_{dop} = 9nm$) are compared (for experimental details, please refer to [17]). Following Equation 5, the transfer characteristics show an almost perfect linear relation between $\sqrt{I_{D,sat}}$ and V_{GS}. Furthermore, as predicted by the model, the threshold voltage, defined as the intercept of the linear fit shown in Figure 2a with the voltage axis, increases with the thickness of the doped layer (cf. Figure 2b as well). The current at the threshold voltage $I_{D,sat}(V_{GS} = V_{th}) = \frac{2}{3} \frac{e d_{dop} N_A}{C_i} \cdot (V_{PO} - V_{th})$ (cf. Eq, 5) increases with increasing doping, i.e. more voltage has to be applied to the gate to turn the transistor off (the pinch-off voltage V_{PO}). Additionally, Figure 2b shows as well the temperature dependency of the threshold voltage, which is caused by the activation energy of the doping process, leading to varying values of N_A and consequently a shift in V_{th}.

(a)



(b)

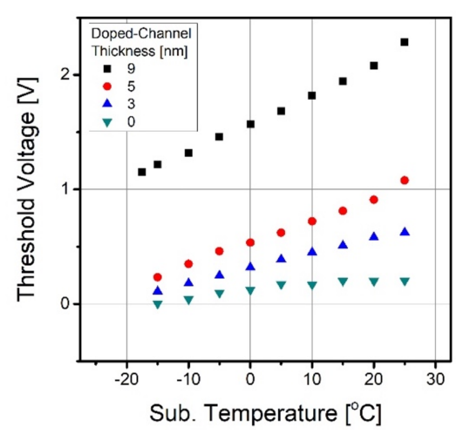


Figure 2: *(a) Comparison of an intrinsic (red) and a doped transistor (black). As predicted by the model, doping leads to a shift in threshold voltage ΔV_{th}, an increase in current at the threshold voltage ΔI_D, and an increase in the pinch-off voltage V_{PO}. The threshold voltage of doped OFETs with*

increasing thickness of the doped layer (0, 3, 5, 9nm) is plotted in (b). The threshold voltage shift decreases with decreasing temperature, which can be interpreted as a freeze out of the doping process.

***Reduced Gate-Bias Stress**:* Doping not only provides an additional handle to tune the transistor behavior but makes them more reliable. An example is shown in Figure 3, where the shift in the threshold voltage due to gate bias stress is plotted vs. the stress time. Overall, the shift in the threshold voltage is in the range of 1.2V for the intrinsic device. This value is reduced to approx. 0.7V for doped devices. Interestingly, the gate bias stress behavior is not further improved for thicker doped layers, which indicates that the doped layer has an effect mainly at the organic semiconductor/gate oxide interface.

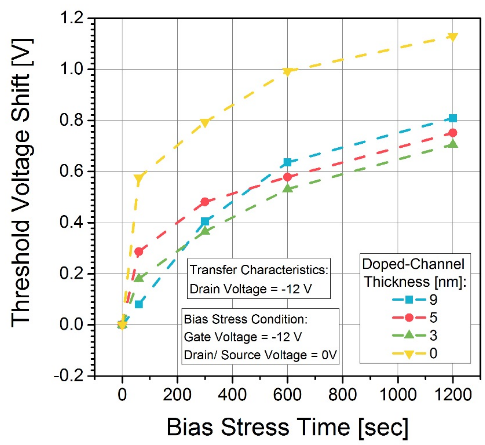


***Figure 3:** Gate-Bias Stress for doped transistors. Channel doping reduces the shift in the threshold voltage. However, the effect does not depend on the thickness of the doped layer, which indicates that the interface between the gate oxide and the doped layer dominates this behavior.*

***Electrochemical Doping – The Organic Electrochemical Transistor**:* In the previous examples, the transistor channel is depleted electrostatically, i.e. by a positive voltage applied to the gate electrode. However, in organic electrochemical transistors, the doped channel can be depleted or de-doped electrochemically by controlling ion migration into the active layer. Bernards et al. proposed a simple model of electrochemical transistors and proposed that these transistors can be treated mathematically as depletion transistors [6]. Indeed, as shown in Figure 4, this model leads to a good description of the transistor behavior. The output characteristic clearly shows a linear regime at low V_{DS}, before the drain current saturates at increased V_{DS}. However, the simple model treats ion and electron transport separately, which leads to some inconsistencies in the theoretical description.

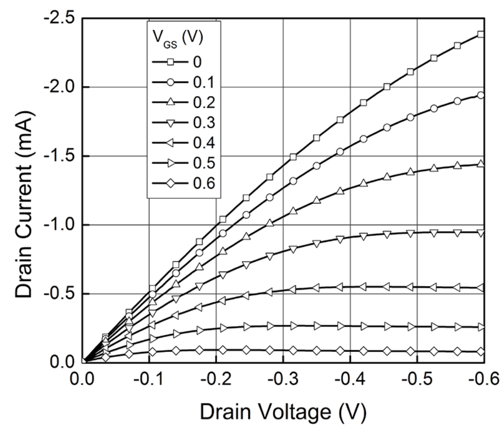


***Figure 4:** Output Characteristic of an organic electrochemical transistors. The transistor can be described as depletion transistors and shows a linear and a saturation regime.*

3. Impact

An analytical solution for doped organic transistors is derived, which is used to systematically discuss transistor behavior. It is shown that the threshold voltage of doped transistors can be influenced by the thickness of the doped layers and the temperature. Furthermore, the gate bias stress of these transistors is reduced, which is a major benefit in particular for larger integrated circuits.

4. Acknowledgements

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5. References

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