Transport Properties and Device Prospects of Ultra-thin Black Phosphorus on Hexagonal Boron Nitride

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Black phosphorus has reemerged as a promising layered material with significant potential for future nanoelectronic applications due to its high mobility and tunable bandgap. Several recent studies have demonstrated an improvement in the transport properties of black phosphorus Schottky barrier MOSFETs when insulated from SiO_2 substrates using hexagonal boron nitride (or when fully encapsulated). The improvement is typically characterized using extractions of mobility based on the empirical relationship between conductivity and carrier density. However, this does not provide insight into the mechanisms associated with the transport improvement, nor it allows accounting for differences in intrinsic (e.g., bandgap, effective mass) and extrinsic (e.g., trap density/distribution, Schottky barrier heights) properties in the analysis. Here we present a modeling approach for Schottky-barrier MOSFETs with low-dimensional channel materials based on the Landauer theory. Our approach uses self-consistent calculation of the channel potential based on the concept of quantum capacitance to extend the model validity into the on-state where transport is limited by scattering in the channel. Our analysis demonstrates an (energy-averaged) scattering mean free path that is > 5 times larger for BP devices with an underlying hexagonal boron nitride layer compared to devices with BP directly on SiO_2.

The electronic and transport properties of layered nanomaterials are currently under extensive investigation for electronic[1], optoelectronic[2], thermoelectric[3], and other potential device applications[4–6]. Black phosphorus (BP) is a layered material that can be fabricated as an ultra-thin (i.e., few-layer) conducting channel and has gained significant interest for next-generation nanoelectronic devices because of its high mobility and tunable bandgap[7–9]. BP nanoelectronic devices are typically constructed as Schottky-barrier (SB)-MOSFETs with metallic source/drain contacts and an insulated gate electrode[10,11]. In general, the transport properties of layered channel materials are affected by the underlying substrate (and the quality of their interfaces), as these introduce disorder and scattering due to charged impurities and other mechanisms, reducing the intrinsic performance of the channel[12,13]. Therefore, recent studies have demonstrated a significant improvement in the transport properties of BP channels when using hexagonal boron nitride (hBN) insulation or encapsulation[7,11,12,14]. Having an atomically smooth surface with nearly negligible dangling bonds and charge traps[15], hBN can be used to insulate the BP channel from the roughness and impurities at the SiO_2 surface, thus achieving an improved transport characteristics.

Here we first present an experimental investigation of the transport properties in BP SB-MOSFETs based on measurements of current-voltage (I_{ds}-V_{gs}) characteristics as a function of channel length (L). This investigation compares results from devices with thin BP channels on SiO_2 as well as devices with a thin layer of hBN between the BP channel and the SiO_2 substrate. The experimental characterization reveals larger on-state currents (I_{on}) in devices with hBN insulating the BP channel, as well as the expected reduction in I_{on} with increasing L for both type of devices. The measurements of I_{on} can be converted into mobility using $\mu = \sigma/(qn_s)$, by calculating the conductivity as $\sigma = (I_{on}/V_{ds})(L/W)$, and approximating the sheet carrier density as $n_s = (C_{ox}/q)(V_{gs} - V_{th})$ above some specified threshold voltage V_{th}. However, this analysis does not consider that current depends not only on geometry, but also on the intrinsic properties of the BP channel and other extrinsic properties of the device, that may vary between different samples. For example, the BP thickness-dependent energy bandgap and the SB heights at

the source/drain contacts[10], and the density and energy distribution of near-interfacial traps[16,17]. It also requires an ambiguous definition of threshold voltage and does not consider that this threshold may vary depending on the charge contribution due to ionized traps, while trap ionization itself is a voltage-dependent mechanism.

Instead, we present an approach to accurately model current flow due to transmission across the Schottky barriers at the source/drain contacts as well as the on-state scattering-limited transmission across the channel region. It extends previous modeling efforts based on the Landauer formalism that use the WKB approximation to calculate tunneling probabilities across the Schottky barriers, which are only valid for off-state operation[10]. The modeling approach is based on a self-consistent solution of the channel potential using the quantum capacitance of the channel and a voltage-dependent density of ionized (i.e., charged) interface traps with non-uniform energy distributions. It also incorporates a channel length (L) and scattering limited transmission across the channel. Therefore, it enables analyzing the impact of scattering on the transport properties of SB MOSFETs as a function of channel length. It incorporates charged-impurity scattering as a function of ionized trap density obtained using the self-consistent solution of the channel potential, as well as phonon-assisted scattering, allowing us to study transport in devices having different substrate characteristics.

We successfully apply the modeling approach to analyze and compare the transport properties of BP devices on SiO_2 with and without an underlying hBN layer. Model fits to the L-dependent experimental I_{ds}-V_{gs} data allows extractions of the backscattering mean free path (λ) averaged over the energy range where current flows for a given biasing condition. This energy-average λ is analyzed as a function of carrier density allowing a direct comparison between the two types of devices indicating > 5x improvement when insulating the BP channel with a thin hBN layer due to reduced charged impurity and phonon scattering.

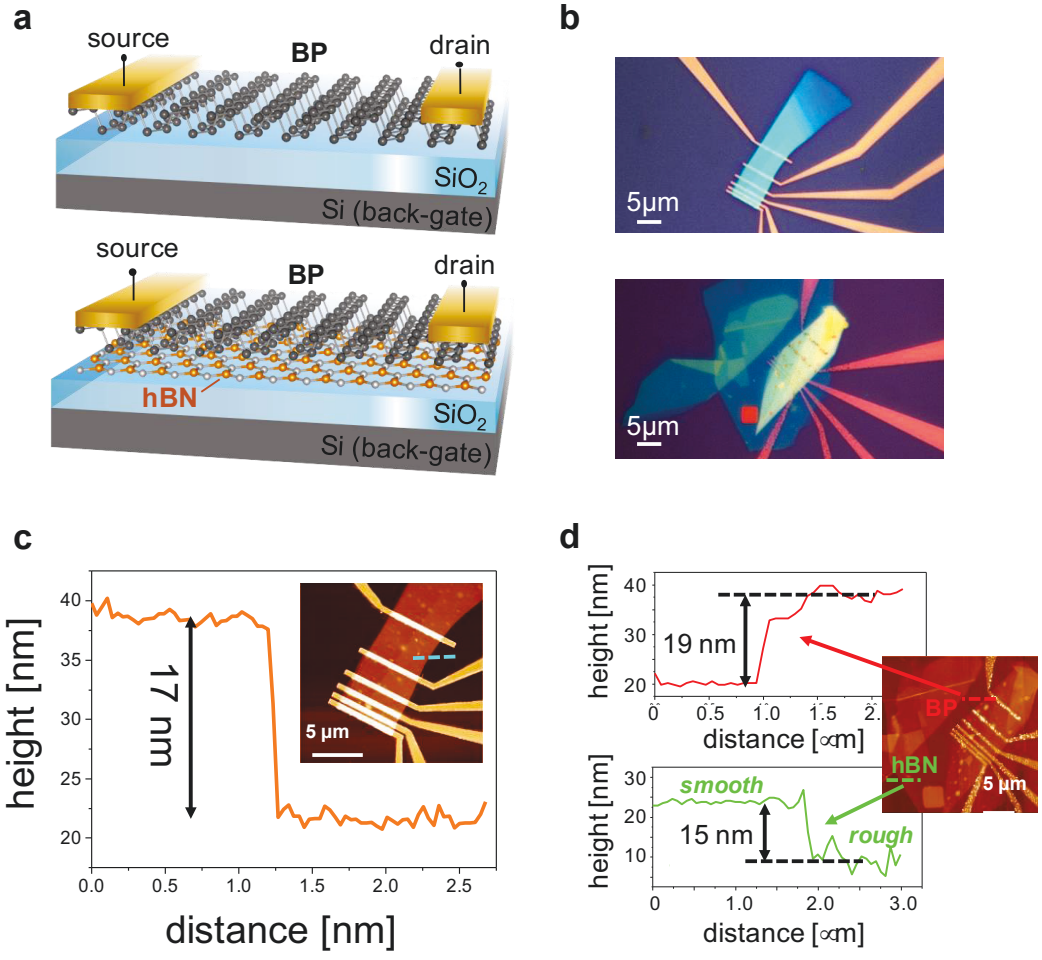

Figure 1. (a) Schematic, (b) optical, and (c)-(d) AFM image of the BP SB-MOSFET devices used in this study. The BP channel is either directly on the SiO_2 substrate or insulated with hBN. Various channel lengths are achieved using multiple metal leads on the same SiO_2/BP and SiO_2/hBN/BP samples. (c) and (d) indicate the measured thickness of the BP and hBN layers.

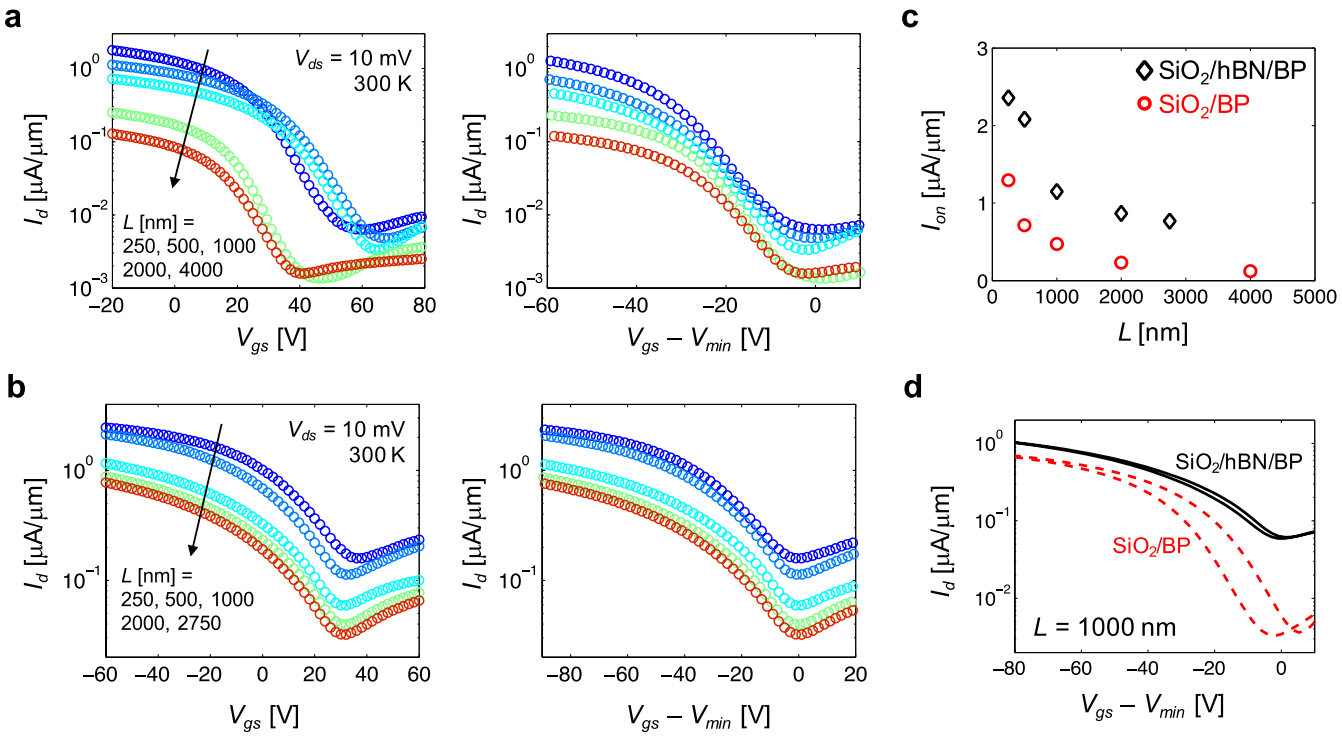

Figure 2. (left) Transfer characteristics (I_d-V_{gs}) for increasing channel lengths (L), and (right) the transfer characteristics with gate voltage axis offset by voltage at the minimum current (V_{min}) for (a) SiO_2/BP, and (b) SiO_2/hBN/BP devices. (c) Extracted on-state current (I_{on}) as a function of channel length indicating transport improvement in devices with hBN insulating layer. (d) Dual gate sweep transfer characteristics (offset by V_{min}) demonstrating a reduction in gate hysteresis for SiO_2/hBN/BP devices.

Device Fabrication. Shown in Fig. 1a are schematic images of the devices used in this study. These consist of a thin-film BP channel on SiO_2/Si substrates with and without an insulating layer of hBN. In Fig. 1b and Fig. 1c we respectively show optical and AFM images of the devices. Devices were fabricated by mechanical exfoliation of BP thin films on PDMS followed by dry transfer onto 300 nm SiO_2 on silicon substrates. For devices with BP on hBN, the hBN was first exfoliated and transferred onto 300 nm SiO_2 followed by BP exfoliation and dry transfer to form the SiO_2/hBN/BP heterostructure. BP samples with similar thickness (~18 nm) were carefully selected for both types of devices by visualizing the optical contrast of BP flakes on PDMS. Moreover, BP flakes with rectangular shapes over a length > ~20 μm were selected to allow fabricating FETs with various channel lengths on the same sample. Exfoliation and transfer was performed in an Argon-filled glovebox (mbraun Inc.) with oxygen and water concentrations well below 0.1 part-per-million (ppm) to ensure high-quality samples. These were subsequently coated with poly (methyl methacrylate) (PMMA) resist and pattered for metallization using a Raith 20 kV electron-beam lithography system. Cr/Au (5/30 nm) contacts were formed by thermal evaporation using a Kurt J Lesker Nano 36 system and lift-off process. Following electrical characterization, AFM was used to measure thickness of the BP and hBN layers. AFM surface profiles indicating these thicknesses are shown in Fig. 1c and 1d.

Channel length dependent characteristics of BP devices. Fig. 2a plots the transfer characteristics (I_d-V_{gs}) of BP on SiO_2 SB-MOSFETs (labeled as SiO_2/BP in Fig. 2 and onward) with increasing channel lengths (L). These are low-field (i.e., near equilibrium) measurements using a drain-to-source voltage of V_{ds} = 10 mV, and at room temperature. While these SB MOSFETs are constructed on the same exfoliated BP sample, they are still vulnerable to device-to-device variation as evidenced by the different "turn-on" (or threshold) voltages. These differences can be attributed to variation in the impact of trapped charge in the SiO_2 and of adsorbed contaminants on the surface of the BP[10,18]. The electrostatic effect of these charged impurities is a positive voltage shift on the I_d-V_{gs} characteristics, typically described as p-type doping of the channel[19], and easily identified by the voltage at which the drain current reaches a minimum value (denoted here as V_{min}). We note that the large positive values of V_{min} on SiO_2/BP devices indicate a significant impact of charged impurities located near the channel. To obtain a better comparison of the transfer characteristics as a function of L, we can offset the voltage axis as shown in Fig. 2a by plotting I_d as a function of $V_{gs} - V_{min}$.

Similarly, in Fig. 2b we plot I_d-V_{gs} curves for devices with the hBN layer underneath the BP channel (labeled as SiO_2/hBN/BP in Fig. 2 and onward), as well as the characteristics offset by V_{min}. SiO_2/hBN/BP devices have smaller V_{min} and less device-to-device variation, indicating a

reduced effect of charged impurities. A smaller on/off ratio results from a slightly thicker BP channel in the SiO_2/hBN/BP devices[9]. From the offset characteristics we can extract drain current at an equivalent on-state biasing condition (I_{on}) for increasing L. In Fig. 2c we plot I_{on} as a function of L for both the SiO_2/hBN/BP and SiO_2/BP devices. I_{on} is extracted at $V_{gs} - V_{min} = -60$ V for SiO_2/BP devices and -90 V for SiO_2/hBN/BP devices to account for the difference in effective oxide thickness (EOT). Here, both types of devices reveal an $\sim 1/L$ (i.e., ohmic) dependence of I_{on} indicating a scattering-limited transport regime. The results in Fig. 2c suggest an improvement in transport efficiency for devices with hBN, as indicated by a larger I_{on}. The improvement in transport is in agreement with the observation of reduced variation and lower V_{min} in devices with hBN insulating the channel from the effects of charged impurities in SiO_2. Thus, transport improvement can be attributed in part to a reduction in scattering due to the hBN layer screening the Coulomb potential of charged impurities in SiO_2[12,13]. Additionally, a reduction in scattering from surface phonons is expected as the hBN layer significantly lowers surface roughness at the channel interface as verified by the AFM surface profile characterization (cf. Fig. 1d) [13,20].

Further evidence of the hBN layer screening the effects of charged impurities is provided in Fig. 2d. Here we show the transfer characteristics obtained using dual gate voltage sweeps for devices with $L = 1000$ nm. A significant reduction in gate hysteresis is measured for devices with hBN. Gate hysteresis is attributed to a dynamic screening of the gate electric field resulting from charge trapping near the interface of the channel and the gate dielectric[21,22]. Here, the hBN layer separates the BP channel from traps in the SiO_2, effectively diminishing their dynamic charge contribution resulting in a reduction of gate hysteresis. We note that while the impact of "slow" traps in SiO_2 that contribute to hysteresis can be eliminated with the introduction of the hBN layer, interface traps that can much faster respond to changes in gate bias are still present. These traps are presumably located in a thin (~1-2 nm) native phosphorus oxide (PO_x) layer directly adjacent to the BP channel[23,24]. These interface traps will not significantly contribute to gate hysteresis, as their occupancy responds immediately to changes in bias (i.e., over the timescales of interest)[22]. However, they have an electrostatic effect on the subthreshold slope and contribute to scattering when in their charged state [12,25,26]. As the native PO_x layer results from ambient exposure during BP sample exfoliation[23], it exists on both the SiO_2/BP and the SiO_2/hBN/BP devices. Thus, their electrostatic and scattering contributions must be considered in our analysis of transport in both types of BP SB-MOSFETs.

The experimental analysis presented in this section provides a good qualitative description of the differences in the electrical characteristics of SiO_2/BP and SiO_2/hBN/BP devices. In the following section we present a modeling approach that allows a better understanding and a quantitative analysis of the transport properties in BP SB-MOSFETs. Applying the model to examine our experimental results enables a direct comparison of transport performance in both types of devices as a function of carrier density, while considering differences in channel thickness and corresponding energy bandgap, electron and hole Schottky barrier heights at the source/drain contacts, density and energy distribution of interface traps, and scattering mechanisms in the channel.

Modeling of SB-MOSFETs. In SB-MOSFETs, charge transport consists of the sum of thermionic and tunneling current components. Ambipolar transfer characteristics result from the combination of electron and hole current branches, flowing respectively in the conduction and valence bands. The relative strength of electron and hole branches is determined by the alignment of the Fermi levels in the source/drain contacts and the electronic bands in the channel. Fig. 3a illustrates the charge transport mechanisms in the SB-MOSFET using an electronic band diagram. The contacts are considered to be large reservoirs of electrons maintaining near equilibrium conditions described using (equilibrium) Fermi functions with Fermi levels E_{Fs} and $E_{Fd} = E_{Fs} - qV_{ds}$ respectively at the source and drain. The role of the gate-to-source voltage (V_{gs}) is to shift the energy level of the bands in the channel region with respect to E_{Fs}, effectively modulating the tunneling barriers at the source/drain Schottky contacts. Equivalently, we can define a channel potential (qV_C) to describe the shift in E_{Fs} (i.e., the electrochemical potential) with respect to fixed bands in the channel of the device. As indicated in Fig. 3a we use the middle of the gap as the reference for qV_C. For the biasing condition illustrated in Fig. 3a (i.e., large negative V_{gs}) the source/drain Fermi levels align with the top of the valence band (E_V) and a large hole current flows. Hole current consists of tunneling (across the barrier) and thermionic (over the barrier) components, subjected to scattering in the channel. Transmission probabilities across the source, channel, and drain regions are respectively denoted as T_S, T_C, and T_D. While there is no tunneling current for electrons at this biasing condition, there is a small thermionic component limited by a large barrier for injection from the drain into the conduction band in the channel.

The transport mechanisms described above are modeled using the Landauer formalism[27,28] where (hole) current is expressed as

$$I = \frac{2q}{h}\int_{-\infty}^{E_V} T(E)M(E)[f(E, E_{Fs}) - f(E, E_{Fd})]dE. \qquad (1)$$

Here, f is the Fermi function, $M(E) = (g_v/\pi\hbar)[2m_h^*(E_V - E)]^{1/2}$ is the number of modes inside the valence band of the 2-D channel (i.e., for $E < E_V$), where g_v is the valley degeneracy

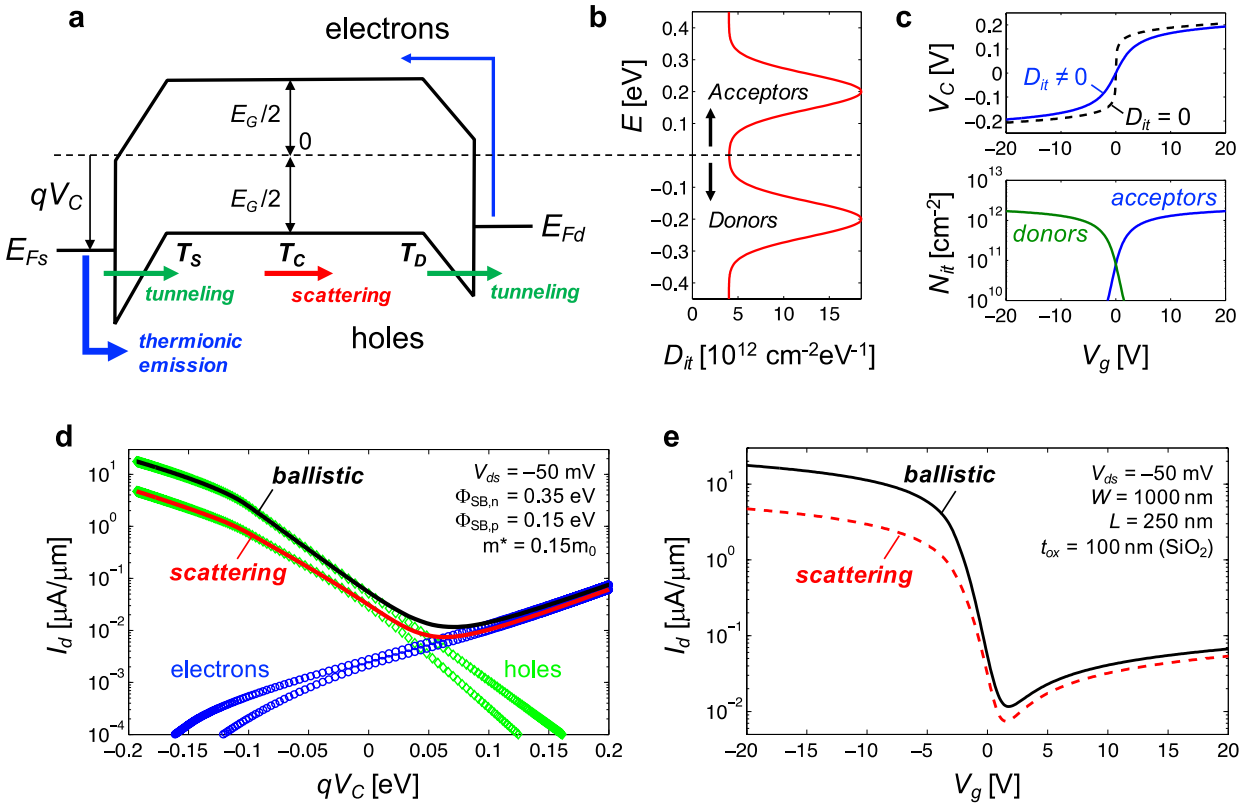

Figure 3. (a) Electronic band diagram of the SB MOSFET indicating the charge transport mechanisms. (b) Typical Gaussian distribution of acceptor and donor-like interface traps used in model calculations. (c) (top) Self-consistent calculation of the channel potential as a function of gate bias with and without interface traps; (bottom) density of ionized traps based on self-consistent solution of channel potential. (d) Calculation of drain current components (i.e., electron and hole currents) for both ballistic and scattering-limited transport in the channel. (e) Ballistic and scattering-limited transfer characteristics.

and m_h^* is the hole effective mass in the valence band. The transmission coefficient $T(E)$ is obtained based on the series combination of scatterers and is given by[28]

$$T = \left[1 + \left(\frac{\lambda - T_S}{T_S}\right) + \left(\frac{\lambda - T_D}{T_D}\right) + \left(\frac{\lambda - T_C}{T_C}\right)\right]^{-1}. \quad (2)$$

For energies between E_V and the peak of the barrier for holes, T_S and T_D are calculated using the WKB approximation for tunneling probability across a triangular shaped barrier as[10]

$$T_{WKB} = \exp\left\{-\frac{2\pi}{h}\int_0^{x_0}\sqrt{2m_h^*[E - E_V(x)]}\,dx\right\}. \quad (3)$$

Scattering in the channel is modeled using an energy-dependent backscattering mean-free-path $\lambda(E)$ from which we obtain transmission across the channel as

$$T_C = \frac{\lambda(E)}{\lambda(E) + L}. \quad (4)$$

Here we use a power-law $\lambda(E) = \lambda_0[(E_V - E)/(k_B T_L)]^r$ that is valid for common scattering mechanisms and allows simple analytical modeling while providing general insight about transport[29–31].

The Fermi level at the source/drain is respectively given by $E_{Fs} = qV_C + qV_{ds}/2$ and $E_{Fd} = qV_C - qV_{ds}/2$. The relationship between V_C and V_{gs} is determined by capacitive coupling of the gate to the channel[21,32,33] and is calculated as

$$V_C = (V_g - V_{FB})\frac{C_{ox}}{C_{ox} + C_q(V_C)}, \quad (5)$$

where C_q is the quantum capacitance of the channel given by

$$C_q(V_C) = \frac{q^2}{4k_B T_L}\int_{-\infty}^{+\infty} D(E)\,\mathrm{sech}^2\left(\frac{E - V_C}{2k_B T_L}\right)dE, \quad (6)$$

and $D(E)$ is the density of states in the channel (containing both conduction and valence bands)[32]. In (4), the flat-band voltage V_{FB} accounts for the work-function difference between the gate and the channel (Φ_{MS}) and also contains the charge contribution from ionized (i.e., charged) interface traps. Interface traps can be acceptor-like (charged when occupied by electrons) or donor-like (charged when empty) and trap occupancy is calculated using Fermi functions[21,34]. The resulting expression for V_{FB} is given by

$$V_{FB}(V_C) = \Phi_{MS} - \frac{q}{C_{ox}}\left\{\int_{-\infty}^{+\infty} D_{it,a}(E)f(E, qV_C)dE - \int_{-\infty}^{+\infty} D_{it,d}(E)[1 - f(E, qV_C)]dE\right\}, \quad (7)$$

where $D_{it,a}(E)$ and $D_{it,d}(E)$ are the energy-distributions of the acceptor and donor-like interface trap densities respectively. Eq. (5) is a transcendental equation since both C_q and V_{FB} are functions of the channel potential, and must be solved numerically to obtain a self-consistent solution of V_C.

Figs. 3b-3e illustrate an example of calculations based on the proposed modeling approach for a general SB-MOSFET with a 2-D nanomaterial channel. In Fig. 3b we plot the $D_{it,a}$ and $D_{it,d}$ used in the calculations, where energy is shown in the vertical axis to align with energy band diagram in Fig. 3a. Here we use a typical "u-shaped" distribution modeled by the combination of two Gaussian components, one for acceptor-like traps centered near E_C, and one for donor-like traps centered near E_V. In Fig. 3c we show the self-consistent solution of V_C as a function V_g obtained using (6) as well as the density of *ionized* traps corresponding to the two integral terms in (7). Here we use SiO_2 as the gate dielectric with a thickness of t_{ox} = 100 nm, and we set Φ_{MS} to 0 V. As the magnitude of V_g increases, interface traps are charged resulting in a "stretch-out" or reduction in sharpness of the V_C-V_g characteristics (also shown for references is the case with no traps, i.e., D_{it} = 0). The impact of interface traps on the V_C-V_g characteristics is more visually obvious in the off-state region where $C_q << C_{ox}$ and $V_C \sim V_g$. At larger gate voltages C_q increases rapidly, pinning V_C.

Fig. 3d plots I_d per unit width as a function of qV_C showing the electron (circles) and hole (diamonds) components, as well as the total current (lines), for both ballistic and scattering-limited transport in the channel. These calculations are for V_{ds} = –50 mV, for a device having W = 1000 nm and L = 250 nm. A larger hole current component is achieved since the Schottky barrier heights ($\Phi_{SB,n}$ and $\Phi_{SB,p}$) are set such that the Fermi levels align closer to the E_V at the contacts. Here we use $\Phi_{SB,n}$ = 0.35 eV and $\Phi_{SB,p}$ = 0.15 eV, such that the bandgap $E_g = \Phi_{SB,n} + \Phi_{SB,p}$ = 0.5 eV. In this example, electron and hole effective masses are set to m^* = $0.15m_0$. For the case of scattering-limited transport, transmission across the channel is given by (4) using a power-law $\lambda(E)$ corresponding to charged-impurity scattering. Here, $\lambda_0 \sim N_0/N_{it}$, i.e., mean-free-path is inversely proportional to the density of charged (i.e., ionized) impurities (N_0 is a constant), and r = 3/2[29,30,35]. In Fig. 3e we plot the transfer characteristics (I_d-V_{gs}) for both the ballistic and scattering cases. A reduction in I_d is obtained at large negative V_g when scattering is included in the calculations. Compared to the off-state response, a larger effect of scattering on I_d in the on-state (e.g., for V_g < ~ –5 V) is calculated. This is due to having a scattering-limited transmission (i.e., $T \sim T_C$) in the on-state, while in the off-state transmission is dominated by tunneling across the source/drain Schottky barriers. Additionally, N_{it} increases with V_g resulting in a reduction of the charged-impurity scattering mean free path and a corresponding lowering of T_C.

Discussion: Transport in BP SB-MOSFETs. We now apply the modeling approach to analyze the electrical characteristics of SiO_2/BP and SiO_2/hBN/BP and to discuss transport improvement resulting from insulating the BP channel with hBN. Fits of model calculations to the transfer characteristics of SiO_2/BP devices are shown in Fig. 4a. We model electron and hole conduction at energy levels near E_C and E_V using parabolic bands. The electron and hole effective masses are set respectively to $m_e^* = 0.15m_0$ and $m_h^* = 0.14m_0$, and Schottky barrier heights for electrons and holes are respectively set to $\Phi_{SB,n}$ = 0.34 eV and $\Phi_{SB,p}$ = 0.10 eV, based on BP thickness-dependent values reported in literature[10,36]. The model calculations in Fig. 4a are obtained by adjusting $D_{it,a}(E)$, $D_{it,d}(E)$, and $\lambda(E)$ (as explained below) to simultaneously fit experimental data from all devices with different L. Here, rather than changing model parameters to account for device-to-device variation and obtain a better match to data from individual devices, we use a unique set of parameters and a unique distribution of interface traps. This allows us to use model calculations based on the experimental fit to analyze transport properties as a function of L.

In Fig. 4b we show fits of model calculations to the transfer characteristics of SiO_2/hBN/BP devices with increasing L. In this case we use the same values for effective masses, but set the Schottky barriers to $\Phi_{SB,n}$ = 0.20 eV and $\Phi_{SB,p}$ = 0.13 eV in order to model a reduction in E_g due to a having a slightly thicker BP channel[10] resulting in smaller on/off ratios[9] as observed experimentally. Following the same procedure as above, model calculations are obtained by adjusting $D_{it,a}(E)$, $D_{it,d}(E)$, and $\lambda(E)$ to fit the experiments. Fig. 4c plots $D_{it,a}(E)$ and $D_{it,d}(E)$ used in model calculations for both the SiO_2/BP and SiO_2/hBN/BP devices. Interface traps are modeled using Gaussian distributions that peak near E_C and E_V for acceptor and donor-like traps respectively. The similarity in the shape of the distributions used for the fits is expected as these are associated with traps in the native PO_x layer that is present in both cases. In our calculations, two separate carrier scattering mechanisms are considered, charged-impurity and phonon scattering. We use $1/\lambda(E) = 1/\lambda_{ci}(E) + 1/\lambda_{ph}(E)$ with power-law models for the individual mechanisms where r = 3/2 for charged impurity scattering and r = 1/2 for phonon scattering[29–31,35,37,38]. For charged-impurity scattering λ_0 depends on the density of ionized interface traps (N_{it}) and is modeled as $\lambda_{0ci} = N_{0ci}/N_{it}$, while phonon scattering is modeled using a constant λ_{0ph}. Thus, N_{0ci} and λ_{0ph} are the fitting parameters associated with scattering.

Fig. 4d shows calculations of I_{on} as a function of L in good agreement with the experimental extractions. Larger λ_{0ci} and λ_{0ph} required to fit SiO_2/hBN/BP data indicates transport improvement (i.e., longer mean-free-path). To obtain a quantitative determination of improvement in the transport properties we extract the energy-averaged mean free path as

$$\langle\langle \lambda(E) \rangle\rangle = \frac{\int \lambda(E) M(E)(f_s - f_d) dE}{\int M(E)(f_s - f_d) dE}. \quad (8)$$

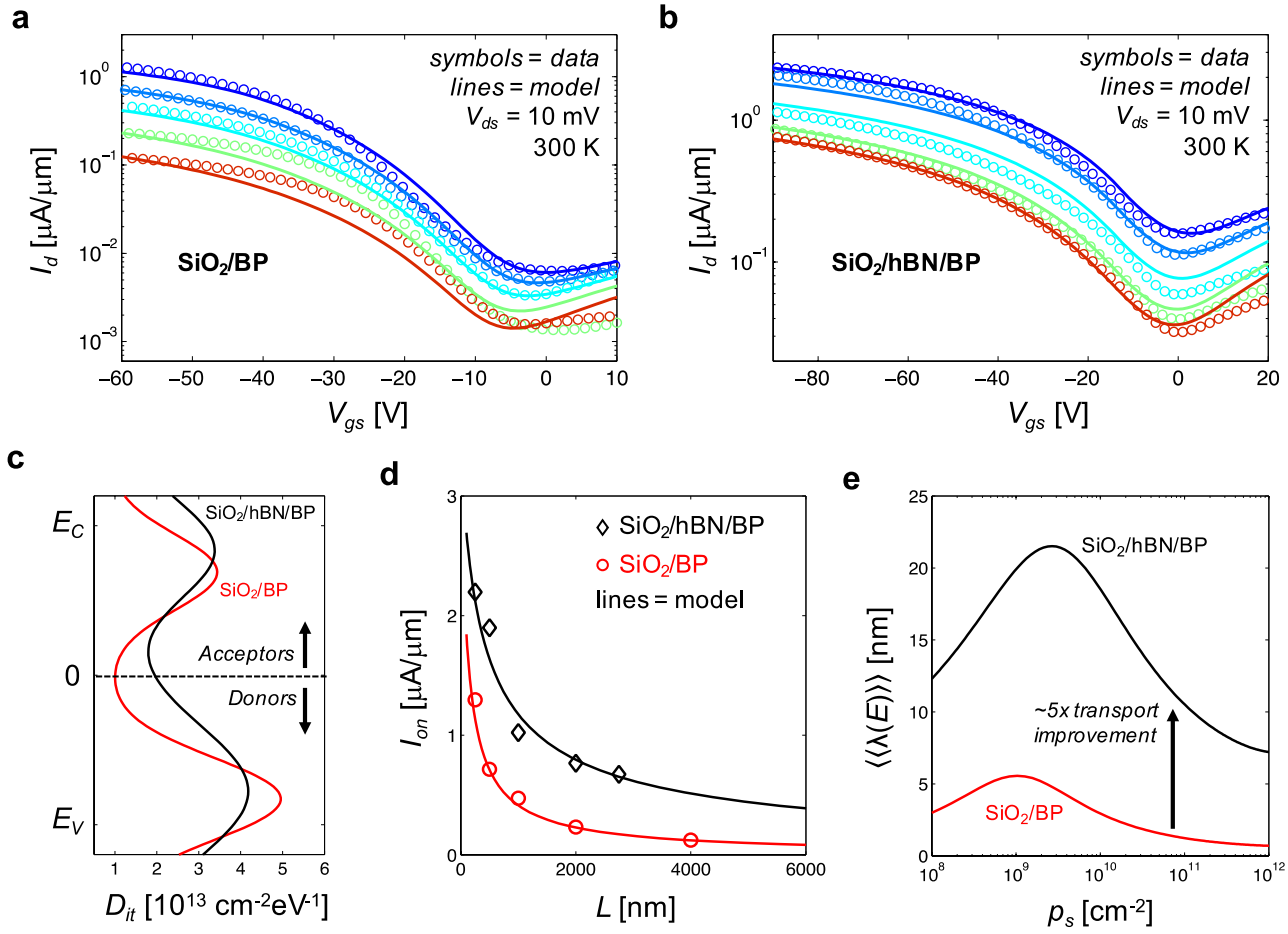

Figure 4. Fits of model calculations to the experimental I_d-V_{gs} characteristics of (a) SiO_2/BP and (b) SiO_2/hBN/BP SB-MOSFETs with increasing channel length L. (c) The energy distribution of acceptor- and donor-like interface traps used to fit experimental data. (d) Model calculation and experimental extractions of the on-current I_{on} as a function of L for both the SiO2/BP and SiO2/hBN/BP SB MOSFETs showing good agreement. (e) Calculations of the energy-averaged mean-free-path as a function of hole sheet density based on the experimentally verified model for both type of devices. Results indicate transport improvement due to larger mean free path for charged impurity and phonon scattering.

In (8), $f_s = f(E, E_{Fs})$ and $f_d = f(E, E_{Fd})$. $\langle\langle\lambda(E)\rangle\rangle$ represents a weighted average of $\lambda(E)$ over the energy range where most of the current flows for a given bias (as determined by the density of modes and the difference in the Fermi functions, i.e., the "Fermi-window"). Additionally, calculating carrier (hole) sheet density as $p_s = \int_{-\infty}^{E_V} D(E)[1 - f(E, qV_C)]dE$ allows a direct comparison of $\langle\langle\lambda(E)\rangle\rangle$ between both types of devices. In other words, by comparing the average mean free path as a function of carrier density we eliminate discrepancies due to differences in device characteristics (e.g., geometry, gate dielectric thickness, BP channel thickness, trap density/distribution, etc.), allowing a fundamental comparison of transport properties. In Fig. 4e we plot $\langle\langle\lambda(E)\rangle\rangle$ as a function of p_s for both SiO_2/BP and SiO_2/hBN/BP devices. In both cases, $\langle\langle\lambda(E)\rangle\rangle$ peaks at $p_s \sim 10^9$ cm^{-2} (i.e., in the off-state) where the density of ionized traps is small. Increasing $p_s > \sim 10^9$ cm^{-2} correlates with an increase in the density of ionized donor-like traps resulting in a reduction of $\langle\langle\lambda(E)\rangle\rangle$. Similarly, $p_s < \sim 10^9$ cm^{-2} correlates to an increase in the density of ionized acceptor-like traps, also lowering $\langle\langle\lambda(E)\rangle\rangle$ due to enhanced charged-impurity scattering. A significant transport improvement in SiO_2/hBN/BP devices corresponds to a larger mean free path as indicated in Fig. 4b (i.e., > 5x in the on-state). This is due to a reduction in both charged-impurity and phonon scattering mechanisms, as determined by fits to experimental I_d-V_{gs} data as a function of L.

Conclusion. Using a comprehensive and accurate modeling approach based on the Landauer formalism we analyze the transport properties of SB-MOSFETs with BP channels on SiO_2 with and without an insulating hBN layer. The modeling approach uses a self-consistent solution of the channel potential based on the quantum capacitance of the channel, and incorporates the electrostatic and scattering impact of interface traps having non-uniform energy distributions. It also includes a phonon component to account for roughness at the BP channel interface and its contribution to surface phonon scattering. A detailed comparison of model

calculations and experimental data allows analyzing the transport properties of SiO_2/hBN/BP and SiO_2/BP SB-MOSFETs as a function of channel length. This analysis enables the extraction of an energy-averaged mean-free-path that includes both charged-impurity and phonon scattering mechanisms. We provide a direct comparison of the energy-averaged mean-free-path as a function of carrier density for both types of devices based on the experimentally-validated model. The comparison reveals a mean free path that is > 5 times larger in the on-state for devices with hBN insulating the BP from SiO_2. This is attributed to a screening of the scattering potential from charged-impurities in the SiO_2, as well as a reduction in phonon scattering mechanisms due to improved surface roughness in the BP channel.

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