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# Diagnostic Test Generation that Addresses Diagnostic Holes

Irith Pomeranz

***Abstract*— A diagnostic test generation procedure targets fault pairs in a set of target faults with the goal of distinguishing all the fault pairs. When a fault pair cannot be distinguished, it prevents the diagnostic test set from providing information about the faults, and consequently, about defects whose diagnosis would have benefited from a diagnostic test for the indistinguishable fault pair. This is referred to in this paper as a diagnostic hole. The paper observes that it is possible to address diagnostic holes by targeting different $but\ related$ fault pairs, possibly from a different fault model. As an example, the paper considers the case where diagnostic test generation is carried out for single stuck-at faults, and $related$ bridging faults are used for addressing diagnostic holes. Considering fault detection, an undetectable single stuck-at fault implies that certain related bridging faults are undetectable. The paper observes that, even if a pair of single stuck-at faults is indistinguishable, a related pair of bridging faults may be distinguishable. Based on this observation, diagnostic tests for pairs of bridging faults are added to a diagnostic test set when the related single stuck-at faults are indistinguishable. Experimental results of defect diagnosis for defects that do not involve bridging faults demonstrate the importance of eliminating diagnostic holes.**

***Index Terms*— Bridging faults, defect diagnosis, diagnostic test generation, set of candidate faults, stuck-at faults.**

## I. Introduction

Defect diagnosis is important as part of a yield improvement process for providing information about defects that occur in faulty circuits. A defect diagnosis procedure computes a set of candidate faults that are likely to be present in the faulty circuit given the output response of the circuit to a test set [1]. In many cases, a fault detection test set provides sufficient fail data for a defect diagnosis procedure to produce a small and accurate set of candidate faults.

When a fault detection test set is not sufficient for defect diagnosis, a diagnostic test set can be used. A diagnostic test set is produced by a diagnostic test generation procedure [1]-[21]. Similar to test generation for fault detection, diagnostic test generation targets a set of faults $F$. In contrast to test generation for fault detection, where the goal is to detect every fault in $F$, the goal of diagnostic test generation is to distinguish every pair of faults in $F$. A pair of faults $(f_i, f_j)$ is distinguished by a test $t$ if the faults produce different output responses to $t$. In this case, a defect diagnosis procedure can compare the responses of $f_i$ and $f_j$ with the response of the faulty circuit, and decide which one of the faults is more likely to be present in the circuit. If a pair of faults $(f_i, f_j)$ is not distinguished, the faults produce the same output response to every test. In this case, the defect diagnosis procedure is unable to decide which one of the faults is more likely to be present in a faulty circuit. Both faults are either included or excluded together from the set of candidate faults.

Two approaches exist for diagnostic test generation. The first approach generates a diagnostic test set that is independent of the faulty circuits that need to be diagnosed. In this case, $F$ is the set of all the target faults from a selected fault model. Typically, the target faults are single stuck-at or transition faults since the numbers of faults for these fault models are such that it is practical to consider all the faults. The diagnostic test generation procedure attempts to distinguish all the fault pairs in $F$. Examples of this approach are the procedures described in [1]-[6].

The second approach applies a diagnostic test generation procedure only after defect diagnosis has already been applied to faulty circuits based on a fault detection test set. In this case, the goal of diagnostic test generation is to address specific faulty circuits for which the sets of candidate faults are large. Let $C$ be a large set of candidate faults that was obtained for a faulty circuit. Using $F = C$, the diagnostic test generation procedure targets fault pairs from $C$. With a diagnostic test set that distinguishes fault pairs from $C$, the faulty circuit produces additional fail data that is relevant to the candidate faults in $C$. The defect diagnosis procedure can use this additional information for narrowing down the set of candidate faults. Examples of this approach are the procedures described in [7], [18], [20] and [21].

The second approach may target faults from different fault models that appear together in a set of candidate faults. For example, a large set of candidate faults $C$ may consist of stuck-at, stuck-open and bridging faults. In this case, diagnostic test generation is carried out for mixed pairs of faults from $C$. Only one fault model is typically used for the first approach because of the computational effort of diagnostic test generation for all the fault pairs in $F$, and the number of tests required for a diagnostic test set.

With both approaches, the presence of indistinguishable fault pairs in $F$ prevents the diagnostic test set from providing information about the behavior of the faults. This affects the ability to diagnose defects whose diagnosis would have benefited from diagnostic tests for the indistinguishable fault pairs. This situation is referred to in this paper as a diagnostic hole. To address diagnostic holes, the paper makes the following new observation. As an example, the discussion focuses on the set of all the single stuck-at faults as the main target of diagnostic test generation under the first approach, with bridging faults being used for addressing diagnostic holes. However, different fault models can be considered in a similar

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way under the first or second approach to diagnostic test generation.

Considering fault detection, a single stuck-at fault being undetectable implies that certain bridging faults, whose detection conditions include the detection of the single stuck-at fault, are also undetectable. Such a bridging fault is referred to as related to the stuck-at fault. However, if a pair of single stuck-at faults is indistinguishable, the pair of related bridging faults may be distinguishable. A test that distinguishes the pair of related bridging faults, when applied to a faulty circuit, provides additional information that is otherwise missing because of the indistinguishable pair of stuck-at faults. This allows diagnostic holes that are created by indistinguishable pairs of single stuck-at faults to be addressed by using diagnostic tests for pairs of related bridging faults. The bridging faults do not have to be realistic. By allowing arbitrary related bridging faults to be used, the procedure has more flexibility to generate additional diagnostic tests and improve the quality of defect diagnosis.

While a test hole is caused by missing tests for fault detection, a diagnostic hole is caused by missing diagnostic tests. The observation above indicates that addressing diagnostic holes can be done by distinguishing pairs of related faults from different fault models.

Motivated by this discussion, the paper suggests a new approach to diagnostic test generation. In this new approach, diagnostic test generation is carried out for two sets of faults, as follows.

(1) Diagnostic test generation is first carried out for a set $F_0$ of target faults (the set of all the single stuck-at faults in this paper).

(2) Let $P_0$ be the set of indistinguishable fault pairs in $F_0$. For every fault pair in $P_0$, one or more pairs of related faults are included in $P_1$ (in this paper, four-way bridging faults are used for defining $P_1$). Diagnostic test generation is carried out for $P_1$ to address the associated diagnostic holes.

Experimental results demonstrate that, although the fault pairs in $P_0$ are indistinguishable, related fault pairs in $P_1$ are distinguishable, and contribute new tests to the diagnostic test set. Moreover, when defect diagnosis is carried out with the enhanced diagnostic test set, more accurate results are obtained for defects that do not involve bridging faults.

It should be noted that both diagnostic test generation procedures and defect diagnosis procedures are important for ensuring accurate diagnosis. The main contribution of the paper is to diagnostic test generation, and not to defect diagnosis. In the context of defect diagnosis, realistic bridging faults are used since they are more likely to be present in the circuit. This property is not necessary when performing diagnostic test generation. In addition, by focusing on pairs of bridging faults that are related to indistinguishable pairs of stuck-at faults, the diagnostic test generation procedure described in this paper is different from a general diagnostic test generation procedure that targets multiple fault models. Specifically, the number of bridging fault pairs that the procedure targets is determined by the number of indistinguishable stuck-at fault pairs, and not by the total number of bridging fault pairs.

The paper is organized as follows. Section II discusses the two approaches to diagnostic test generation in more detail. Section III discusses the relationship between single stuck-at faults and four-way bridging faults. This relationship allows pairs of four-way bridging faults to address diagnostic holes that are caused by indistinguishable pairs of single stuck-at faults. Section IV describes the diagnostic test generation procedure that addresses diagnostic holes, and presents results of diagnostic test generation. Section V describes an experiment that employs a defect diagnosis procedure to demonstrate the effects of the improved diagnostic test set, and presents experimental results.

## II. Diagnostic Test Generation

Diagnostic test generation is more time consuming than test generation for fault detection, and diagnostic test sets are larger than fault detection test sets. The second approach to diagnostic test generation reduces these overheads by targeting only fault pairs that appear in large sets of candidate faults. However, this approach also generates a different diagnostic test set for every faulty circuit. This can be a disadvantage when different faulty circuits are tested in parallel.

The procedure described in [21] attempts to partition the faulty circuits into a small number of groups where every group requires its own test set. However, it still requires different test sets for different groups.

The first approach to diagnostic test generation computes the same diagnostic test set regardless of the faulty circuits that need to be diagnosed. Computing a single diagnostic test set removes the need for multiple test sets altogether. It also has the advantage that diagnostic test generation is applied only once.

Because of the computational effort and number of diagnostic tests, the first approach uses a single fault model. Considering the accuracy of defect diagnosis, this is justified by the following considerations.

In the case of fault detection, a test set that is generated for a set of target faults $F$, such as single stuck-at faults, is also effective in detecting defects whose behaviors are not identical to those of single stuck-at faults. This is because the tests set up the activation and propagation conditions necessary for detecting faults as well as defects. Analogously, in the case of defect diagnosis, a test set that distinguishes a pair of faults in a set of target faults $F$ is also effective in distinguishing defects whose behaviors are not identical to those of the target faults.

This argument is strengthened by the fact that many defect diagnosis procedures attempt to match the behavior of a faulty circuit with the behaviors of faults from specific fault models [22]-[24]. In this case, distinguishing between fault pairs from the fault models that are used by the defect diagnosis procedure helps the procedure provide smaller sets of candidate faults. This is true even if the defects present in the faulty circuit have different behaviors.

This argument fails when an indistinguishable fault pair leaves a diagnostic hole. In this case, the test set fails to provide information about the faults, and more important, about defects whose diagnosis would have benefited from a diagnostic test for the indistinguishable fault pair. Diagnostic holes are also important when large sets of candidate faults provide the targets for diagnostic test generation. Diagnostic holes are addressed in this paper in the context of the first approach using single stuck-at and bridging faults. However, the resulting approach to diagnostic test generation can be applied with different sets of faults, and under the second approach.

## III. Single Stuck-At and Four-Way Bridging Faults

For the discussion in this paper, $g/a$ denotes the fault where line $g$ is stuck at the value $a$. A four-way bridging fault $g/a/h$ is defined in [25]-[26] as follows.

The fault is associated with two lines, $g$ and $h$, and a value $a$. In the presence of the fault, the value $a$ on line $h$ dominates the value of line $g$, and causes it to assume the value $a$. If a test assigns $g = a'$ and $h = a$ in the fault-free circuit, the presence of the fault results in the fault effect $a'/a$ on $g$. To detect the fault, the test needs to assign $h = a$ and detect the fault $g/a$.

The four-way bridging fault $g/a/h$ is related to the single stuck-at fault $g/a$ in that the detection conditions of $g/a/h$ contain the detection conditions of $g/a$. If $g/a$ is undetectable, then $g/a/h$ is also undetectable.

The relationship between pairs of related faults is discussed next. Let $(g_0/a_0, g_1/a_1)$ be a pair of detectable but indistinguishable single stuck-at faults. The pair $(g_0/a_0/h_0, g_1/a_1/h_1)$ consists of related four-way bridging faults, where $g_0/a_0/h_0$ is related to $g_0/a_0$, and $g_1/a_1/h_1$ is related to $g_1/a_1$. The ability to address the diagnostic hole that is created by the pair $(g_0/a_0, g_1/a_1)$ is based on the possibility that $(g_0/a_0/h_0, g_1/a_1/h_1)$ is distinguishable even though $(g_0/a_0, g_1/a_1)$ is not. This possibility can be explained as follows.

The fact that $g_0/a_0$ and $g_1/a_1$ are detectable but $(g_0/a_0, g_1/a_1)$ is indistinguishable implies that every test either detects both faults on the same outputs, or does not detect any one of them. Let us consider a test that detects both faults. If the test assigns $h_0 = a_0$ and $h_1 = a_1'$, or $h_0 = a_0'$ and $h_1 = a_1$, then it detects one of the four-way bridging faults of the pair, but not the other. In this case, the test distinguishes the fault pair $(g_0/a_0/h_0, g_1/a_1/h_1)$.

The following example illustrates this possibility. Figure 1 shows the combinational logic of ISCAS-89 benchmark $s27$. Line numbers are shown in square brackets. For every line, its value under a test is shown following the line number.

The pair of single stuck-at faults (14/1,20/0) is indistinguishable. Let us consider the pair of four-way bridging faults (14/1/3,20/0/15) that is related to the indistinguishable fault pair (14/1,20/0).

Under the test shown in Figure 1, the faults 14/1 and 20/0 are detected, and they create the same fault effects on lines 24 and 26.

The bridging fault 14/1/3 is not detected because line 3 assumes the value zero, and the value one is needed for activating the bridging fault. The bridging fault 20/0/15 is detected because line 15 assumes the value zero, and the fault 20/0 is detected. Consequently, the pair of bridging faults (14/1/3,20/0/15) is distinguished by the test.

A diagnostic test for the pair of related bridging faults (14/1/3,20/0/15), when used as part of a diagnostic test set, provides additional information about the defects that are present in a faulty circuit. The information is related to the sites of the faults 14/1 and 20/0. This information is not otherwise available because the pair of stuck-at faults (14/1,20/0) is indistinguishable. Additional diagnostic information is obtained even without requiring that the bridging faults 14/1/3 and 20/0/15 would be realistic bridging faults.

The relationship between pairs of single stuck-at and bridging faults is used in the next section to address diagnostic holes of a diagnostic test set for single stuck-at faults.

## IV. Diagnostic Test Generation Procedure that Addresses Diagnostic Holes

This section describes the diagnostic test generation procedure that addresses diagnostic holes because of indistinguishable fault pairs using single stuck-at and four-way bridging faults as the target fault models.

### A. Phase 1 of the Procedure

The procedure first targets the set $F_0$ of single stuck-at faults. Any diagnostic test generation procedure can be used for producing a diagnostic test set $T_0$ for the fault pairs in $F_0$. The diagnostic test generation procedure from [5] is used in this paper. The procedure starts from a fault detection test set $T_{sa}$ for single stuck-at faults by initially assigning $T_0 = T_{sa}$. It adds to $T_0$ diagnostic tests for pairs of single stuck-at faults that are not distinguished by $T_{sa}$. After diagnostic test generation for $F_0$, the pairs of faults that are not distinguished by $T_0$ are included in $P_0$.

It should be noted that, during diagnostic test generation, it is not necessary to consider all the fault pairs from $F_0$ explicitly. Diagnostic fault simulation is used for computing the equivalence classes of $T_0$ initially, and as new tests are added to it. An equivalence class contains faults that are not distinguished by $T_0$. Faults in different equivalence classes are distinguished by $T_0$. The diagnostic test generation procedure targets pairs of faults from the same equivalence class of $T_0$. After diagnostic test generation for $F_0$ is complete, the number of indistinguished fault pairs is typically small. At this point, the set $P_0$ can be represented as a set of pairs.

### B. Phase 2 of the Procedure

Diagnostic test generation continues in the second phase to address the diagnostic holes given by $P_0$. For a parameter denoted by $b > 0$, the procedure targets a set of bridging fault pairs that is denoted by $P_b$. In $P_b$ there are $b$ pairs of four-way bridging faults for every fault pair in $P_0$. It is possible to use $b > 1$ since every single stuck-at fault $g/a$ is related to several four-way bridging faults of the form $g/a/h$. The use of $b > 1$ increases the likelihood that one or more of the pairs of bridging faults will be distinguished, and contribute to the

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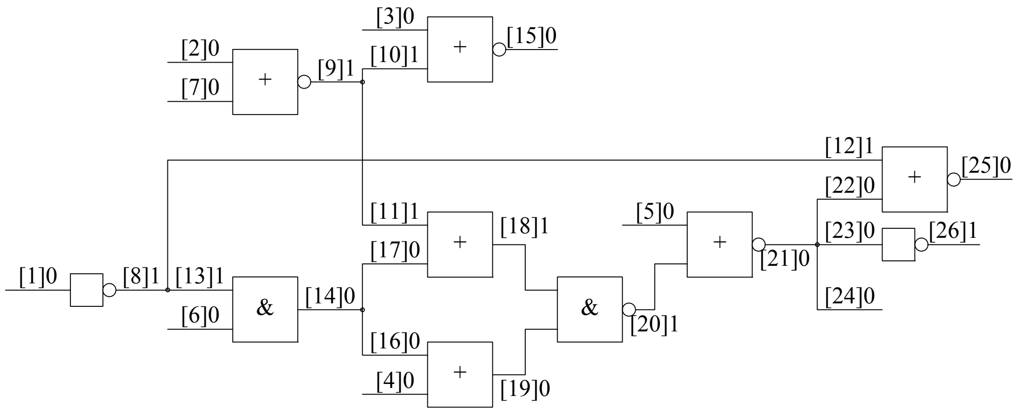


Fig. 1. Example of diagnostic hole

elimination of the diagnostic hole. The selection of a value for $b$ will be discussed later. The selection of $P_b$ for a given value of $b$ proceeds in several steps as described next.

For every pair of faults $(g_0/a_0, g_1/a_1) \in P_0$, the faults $g_0/a_0$ and $g_1/a_1$ are included in a set that is denoted by $D_0$. The faults in $D_0$ require related bridging faults in order to define pairs of bridging faults that will be included in $P_b$.

In the example of $s27$, the circuit has two indistinguishable fault pairs, (4/0,11/0) and (14/1,20/0). This results in $D_0 = \{4/0, 11/0, 14/1, 20/0\}$.

Related bridging faults are included in a set that is denoted by $B_0$. For every fault $g_i/a_i \in D_0$, a constant number $b_1 \geq b$ of bridging faults is added to $B_0$. The use of $b_1 \geq b$ allows for undetectable bridging faults that will not be used for defining bridging fault pairs. The bridging faults based on $g_i/a_i \in D_0$ are computed as follows.

The procedure finds a set of lines $H_i$ that will be used for defining bridging faults of the form $g_i/a_i/h_i$, with $h_i \in H_i$. It is possible to select $H_i$ based on a layout analysis that yields realistic bridging faults [27]. However, realistic bridging faults tend to be easy-to-detect [28]. Hard-to-detect faults are selected in [28]. However, these faults tend to be undetectable. To avoid selecting only easy- or hard-to-detect bridging faults, in this paper, $H_i$ includes every line $h_i$ such that there is no directed path in the circuit from $h_i$ to $g_i$. From $H_i$, the procedure selects $b_1$ lines randomly. For every randomly selected line $h_i \in H_i$, the procedure adds the fault $g_i/a_i/h_i$ to $B_0$.

Next, the procedure performs fault simulation with fault dropping of $B_0$ under $T_0$. Faults that are not detected by $T_0$ are removed from $B_0$. These faults will not be used for defining bridging fault pairs.

In the example of $s27$, with $b_1 = 8$, the detectable bridging faults shown in Table I are obtained for the faults in $D_0$.

Next, for every pair of bridging faults $(g_0/a_0, g_1/a_1) \in P_0$, the procedure adds up to $b$ faults to $P_b$ as follows. Let $B_0(g_0/a_0)$ include the bridging faults from $B_0$ that have the form $g_0/a_0/h_0$, for different lines $h_0$. Let $B_0(g_1/a_1)$ include the bridging faults from $B_0$ that have the form $g_1/a_1/h_1$, for different lines $h_1$. Of all the fault pairs in $B_0(g_0/a_0) \times B_0(g_1/a_1)$ that do not have any lines in common, the procedure selects $b$ fault pairs randomly. The random selection ensures that every fault appears in approximately the same number of fault pairs in $P_b$.

In the example of $s27$, with $b = 8$, the fault pairs shown in Table II are added based on the bridging faults shown in Table I.

Diagnostic fault simulation is carried out next for the fault pairs in $P_b$ under the test set $T_0$. Fault pairs that are not distinguished by $T_0$ are targeted by the diagnostic test generation procedure. Again, the procedure from [5] is used. The resulting diagnostic test set that includes $T_0$ and the new diagnostic tests added to it is denoted by $T_b$.

In the example of $s27$, the fault pairs that are marked with $T0$ under column $dist$ are distinguished by $T_0$. With $b = 8$, diagnostic test generation distinguishes the fault pairs that are marked with $T8$ under column $dist$. Two tests are added to $T_8$ to distinguish these three fault pairs.

TABLE I
EXAMPLE OF BRIDGING FAULTS

| $g_i/a_i$ | $B_0$ |
|---|---|
| 4/0 | 4/0/15 4/0/14 4/0/25 4/0/26 |
| 11/0 | 11/0/8 11/0/25 11/0/5 11/0/14 11/0/20 11/0/15 |
| 14/1 | 14/1/7 14/1/26 14/1/25 14/1/15 14/1/4 14/1/19 |
| 20/0 | 20/0/21 20/0/25 20/0/15 20/0/3 |

TABLE II
EXAMPLE OF PAIRS OF BRIDGING FAULTS

| $P_8$ | dist |
|---|---|
| (4/0/26,11/0/20) | |
| (4/0/25,11/0/20) | |
| (4/0/15,11/0/25) | |
| (4/0/26,11/0/8) | T8 |
| (4/0/14,11/0/5) | |
| (4/0/26,11/0/15) | |
| (4/0/14,11/0/25) | |
| (4/0/25,11/0/8) | T8 |
| (14/1/25,20/0/21) | T0 |
| (14/1/26,20/0/21) | |
| (14/1/26,20/0/15) | T0 |
| (14/1/19,20/0/3) | T8 |
| (14/1/4,20/0/15) | T0 |
| (14/1/19,20/0/25) | T0 |
| (14/1/4,20/0/25) | T0 |
| (14/1/7,20/0/25) | T0 |

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TABLE III
DIAGNOSTIC TEST GENERATION (ISCAS-89)

| circuit | b | tests | ratio | pairs | indist | ntime |
|---|---|---|---|---|---|---|
| s526 | 0 | 60 | 1.00 | - | 34 | 4.29 |
| s526 | 1 | 64 | 1.07 | 34 | 1 | 4.79 |
| s526 | 32 | 108 | 1.80 | 1088 | 55 | 19.21 |
| s641 | 0 | 42 | 1.00 | - | 7 | 6.00 |
| s641 | 1 | 43 | 1.02 | 7 | 0 | 6.33 |
| s641 | 32 | 55 | 1.31 | 224 | 3 | 12.33 |
| s820 | 0 | 133 | 1.00 | - | 42 | 3.37 |
| s820 | 1 | 139 | 1.05 | 42 | 22 | 4.88 |
| s820 | 32 | 187 | 1.41 | 1344 | 610 | 71.83 |
| s953 | 0 | 88 | 1.00 | - | 3 | 2.09 |
| s953 | 32 | 95 | 1.08 | 96 | 41 | 7.42 |
| s1196 | 0 | 159 | 1.00 | - | 28 | 2.48 |
| s1196 | 1 | 169 | 1.06 | 28 | 10 | 2.95 |
| s1196 | 32 | 235 | 1.48 | 896 | 279 | 25.48 |
| s1423 | 0 | 71 | 1.00 | - | 148 | 7.47 |
| s1423 | 1 | 102 | 1.44 | 148 | 1 | 7.75 |
| s1423 | 32 | 251 | 3.54 | 4736 | 28 | 14.72 |
| s5378 | 0 | 168 | 1.00 | - | 524 | 12.71 |
| s5378 | 1 | 182 | 1.08 | 524 | 1 | 12.86 |
| s5378 | 32 | 296 | 1.76 | 16768 | 23 | 15.77 |
| s9234 | 0 | 340 | 1.00 | - | 1474 | 14.97 |
| s9234 | 1 | 474 | 1.39 | 1474 | 12 | 15.48 |
| s9234 | 32 | 1114 | 3.28 | 47168 | 426 | 33.66 |
| s13207 | 0 | 281 | 1.00 | - | 2926 | 13.06 |
| s13207 | 1 | 584 | 2.08 | 2926 | 10 | 13.34 |
| s13207 | 32 | 1481 | 5.27 | 93632 | 281 | 26.37 |
| s15850 | 0 | 212 | 1.00 | - | 3576 | 21.35 |
| s15850 | 1 | 459 | 2.17 | 3576 | 7 | 21.67 |
| s15850 | 32 | 1284 | 6.06 | 114432 | 332 | 37.21 |
| s38417 | 0 | 337 | 1.00 | - | 4323 | 12.59 |
| s38417 | 1 | 751 | 2.23 | 4323 | 5 | 12.69 |
| s38417 | 32 | 2199 | 6.53 | 138336 | 49 | 15.70 |
| s38584 | 0 | 376 | 1.00 | - | 2730 | 5.97 |
| s38584 | 1 | 564 | 1.50 | 2730 | 33 | 6.02 |
| s38584 | 32 | 1716 | 4.56 | 87360 | 963 | 8.77 |

TABLE IV
DIAGNOSTIC TEST GENERATION (ITC-99)

| circuit | b | tests | ratio | pairs | indist | ntime |
|---|---|---|---|---|---|---|
| b03 | 0 | 28 | 1.00 | - | 2 | 3.00 |
| b03 | 1 | 29 | 1.04 | 2 | 0 | 3.50 |
| b03 | 32 | 32 | 1.14 | 64 | 6 | 6.00 |
| b04 | 0 | 56 | 1.00 | - | 3 | 2.12 |
| b04 | 1 | 57 | 1.02 | 3 | 0 | 2.13 |
| b04 | 32 | 64 | 1.14 | 96 | 2 | 2.34 |
| b05 | 0 | 70 | 1.00 | - | 129 | 3.22 |
| b05 | 1 | 95 | 1.36 | 129 | 6 | 3.48 |
| b05 | 32 | 216 | 3.09 | 4128 | 104 | 10.64 |
| b07 | 0 | 60 | 1.00 | - | 3 | 2.10 |
| b07 | 1 | 61 | 1.02 | 3 | 0 | 2.10 |
| b07 | 32 | 65 | 1.08 | 96 | 10 | 2.66 |
| b08 | 0 | 66 | 1.00 | - | 64 | 5.50 |
| b08 | 1 | 71 | 1.08 | 64 | 35 | 9.00 |
| b08 | 32 | 84 | 1.27 | 2048 | 951 | 199.50 |
| b09 | 0 | 29 | 1.00 | - | 2 | 2.00 |
| b09 | 1 | 30 | 1.03 | 2 | 0 | 2.00 |
| b09 | 32 | 32 | 1.10 | 64 | 6 | 3.33 |
| b10 | 0 | 51 | 1.00 | - | 5 | 2.14 |
| b10 | 1 | 52 | 1.02 | 5 | 4 | 2.43 |
| b10 | 32 | 67 | 1.31 | 160 | 56 | 10.57 |
| b11 | 0 | 77 | 1.00 | - | 35 | 2.86 |
| b11 | 1 | 79 | 1.03 | 35 | 13 | 3.25 |
| b11 | 32 | 115 | 1.49 | 1120 | 400 | 27.94 |
| b14 | 0 | 529 | 1.00 | - | 326 | 3.00 |
| b14 | 1 | 571 | 1.08 | 326 | 42 | 3.20 |
| b14 | 32 | 811 | 1.53 | 10432 | 1283 | 14.29 |
| b15 | 0 | 467 | 1.00 | - | 411 | 2.62 |
| b15 | 1 | 497 | 1.06 | 411 | 37 | 2.69 |
| b15 | 32 | 803 | 1.72 | 13152 | 1019 | 6.39 |
| b20 | 0 | 620 | 1.00 | - | 453 | 2.83 |
| b20 | 1 | 693 | 1.12 | 453 | 21 | 2.92 |
| b20 | 32 | 1275 | 2.06 | 14496 | 508 | 6.37 |

### C. Results of Diagnostic Test Generation

The diagnostic test generation procedure is applied to benchmark circuits using $b_1 = 64$, and $b = 1, 2, 4, ..., 32$. Several values of $b$ are considered in order to show the effects of $b$ on the results and select an appropriate value.

With $b = 1, 2, 4, ..., 32$, the diagnostic test generation procedure produces diagnostic test sets that are denoted by $T_1$, $T_2$, $T_4$, ..., $T_{32}$. In addition, the test set $T_0$ is used as a baseline for comparison.

The results are shown in Tables III-V as follows. For every circuit, the results are shown for $T_0$, $T_1$ and $T_{32}$. Intermediate test sets are omitted to avoid reporting on a large number of test sets. $T_1$ is omitted if it does not contain more tests than $T_0$.

For every test set, after the circuit name, column $b$ shows the value of $b$. Column $tests$ shows the number of tests in $T_b$. Column $ratio$ shows the increase in the number of tests relative to $T_0$, which is computed as $|T_b|/|T_0|$.

Column $pairs$ shows the number of bridging fault pairs that are included in $P_b$ for $b > 0$. A dash is entered for $b = 0$. Column $indist$ shows the number of indistinguished fault pairs in $P_b$ for $b \geq 0$. In the case of $b = 0$, the faults are single stuck-at faults. For $b > 0$, the faults are bridging faults.

Column $ntime$ shows information about the run time for producing $T_b$, where $b \geq 0$. Initially, $T_0 = T_{sa}$. The run time for fault simulation and diagnostic fault simulation of $T_{sa}$ is denoted by $\rho_{sa}$. Let the run time for producing $T_b$ be $\rho_b$. The normalized run time is defined as $\rho_b/\rho_{sa}$, and it shows the increase in run time, relative to the diagnostic fault simulation time of $T_{sa}$, because of the need to generate diagnostic tests. The normalized run time is reported in column $ntime$.

The following points can be seen from Tables III-V. For $b \geq 1$, the diagnostic test generation procedure targets approximately $b|P_0|$ pairs of bridging faults, where $|P_0|$ is the number of indistinguished pairs of stuck-at faults. Although not all the pairs of bridging faults are distinguished, a significant fraction of them are.

The number of tests grows with $b$. For many of the circuits, the number of tests less than doubles even with $b = 32$. The increase is higher when the number of indistinguished single stuck-at faults is large. In this case, addressing the diagnostic holes requires more tests.

The normalized run time also increases with $b$. However, it is not always higher for a larger circuit. This indicates that the procedure scales similar to a diagnostic fault simulation procedure.

A value for $b$ can be selected based on the test set size that can be accommodated. Tables III-V show only the extreme test sets with $b = 0$, 1 and 32. There are also intermediate test sets that may be used, with intermediate numbers of tests.

## V. DEFECT DIAGNOSIS

When diagnostic tests are added to $T_0$ in order to form the diagnostic test set $T_b$, for $b > 0$, the expectation is that a defect

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TABLE V
DIAGNOSTIC TEST GENERATION (IWLS-05)

| circuit | b | tests | ratio | pairs | indist | ntime |
|---|---|---|---|---|---|---|
| aes_core | 0 | 251 | 1.00 | - | 2086 | 3.85 |
| aes_core | 1 | 291 | 1.16 | 2086 | 5 | 3.87 |
| aes_core | 32 | 587 | 2.34 | 66752 | 10 | 4.04 |
| des_area | 0 | 139 | 1.00 | - | 188 | 4.74 |
| des_area | 1 | 145 | 1.04 | 188 | 0 | 4.77 |
| des_area | 32 | 219 | 1.58 | 6016 | 25 | 5.91 |
| i2c | 0 | 68 | 1.00 | - | 8 | 2.39 |
| i2c | 32 | 86 | 1.26 | 256 | 0 | 2.55 |
| pci_spoci_ctrl | 0 | 169 | 1.00 | - | 40 | 2.69 |
| pci_spoci_ctrl | 1 | 178 | 1.05 | 40 | 1 | 2.78 |
| pci_spoci_ctrl | 32 | 232 | 1.37 | 1280 | 241 | 14.60 |
| sasc | 0 | 53 | 1.00 | - | 25 | 3.18 |
| sasc | 1 | 56 | 1.06 | 25 | 0 | 3.21 |
| sasc | 32 | 77 | 1.45 | 800 | 1 | 3.66 |
| simple_spi | 0 | 77 | 1.00 | - | 24 | 2.75 |
| simple_spi | 1 | 79 | 1.03 | 24 | 0 | 2.77 |
| simple_spi | 32 | 109 | 1.42 | 768 | 3 | 3.16 |
| spi | 0 | 556 | 1.00 | - | 59 | 2.87 |
| spi | 1 | 561 | 1.01 | 59 | 3 | 2.93 |
| spi | 32 | 624 | 1.12 | 1888 | 55 | 5.21 |
| steppermotordrive | 0 | 38 | 1.00 | - | 20 | 5.33 |
| steppermotordrive | 1 | 41 | 1.08 | 20 | 4 | 6.00 |
| steppermotordrive | 32 | 71 | 1.87 | 640 | 88 | 40.67 |
| systemcaes | 0 | 155 | 1.00 | - | 1451 | 9.78 |
| systemcaes | 1 | 189 | 1.22 | 1451 | 2 | 9.87 |
| systemcaes | 32 | 391 | 2.52 | 46432 | 52 | 10.97 |
| systemcdes | 0 | 96 | 1.00 | - | 252 | 7.15 |
| systemcdes | 1 | 111 | 1.16 | 252 | 0 | 7.25 |
| systemcdes | 32 | 213 | 2.22 | 8064 | 20 | 8.78 |
| tv80 | 0 | 576 | 1.00 | - | 491 | 3.28 |
| tv80 | 1 | 641 | 1.11 | 491 | 17 | 3.43 |
| tv80 | 32 | 1212 | 2.10 | 15712 | 379 | 7.17 |
| usb_phy | 0 | 44 | 1.00 | - | 23 | 3.60 |
| usb_phy | 1 | 54 | 1.23 | 23 | 0 | 3.69 |
| usb_phy | 32 | 96 | 2.18 | 736 | 6 | 5.80 |
| wb_dma | 0 | 101 | 1.00 | - | 94 | 4.12 |
| wb_dma | 1 | 115 | 1.14 | 94 | 0 | 4.15 |
| wb_dma | 32 | 197 | 1.95 | 3008 | 13 | 5.15 |

TABLE VI
DEFECT DIAGNOSIS (ISCAS-89)

| | | | cand | | cand red | | resol | | prec | |
|---|---|---|---|---|---|---|---|---|---|---|
| circuit | $i$ | $m_i$ | 0 | 32 | % | b | 0 | 32 | 0 | 32 |
| s526 | 87 | 5 | 15 | 10 | 33.33 | 4 | 0.200 | 0.300 | 0.600 | 0.600 |
| s526 | 20 | 7 | 30 | 25 | 16.67 | 2 | 0.233 | 0.280 | 1.000 | 1.000 |
| s526 | 56 | 9 | 33 | 29 | 12.12 | 4 | 0.242 | 0.276 | 0.889 | 0.889 |
| s526 | 93 | 6 | 26 | 24 | 7.69 | 2 | 0.231 | 0.250 | 1.000 | 1.000 |
| s641 | 90 | 6 | 36 | 25 | 30.56 | 2 | 0.111 | 0.160 | 0.667 | 0.667 |
| s641 | 12 | 5 | 23 | 17 | 26.09 | 4 | 0.217 | 0.294 | 1.000 | 1.000 |
| s641 | 64 | 5 | 29 | 22 | 24.14 | 4 | 0.103 | 0.136 | 0.600 | 0.600 |
| s641 | 83 | 9 | 39 | 31 | 20.51 | 2 | 0.179 | 0.226 | 0.778 | 0.778 |
| s820 | 57 | 6 | 25 | 18 | 28.00 | 1 | 0.160 | 0.222 | 0.667 | 0.667 |
| s820 | 19 | 10 | 38 | 29 | 23.68 | 16 | 0.105 | 0.138 | 0.400 | 0.400 |
| s820 | 93 | 10 | 32 | 27 | 15.62 | 4 | 0.281 | 0.333 | 0.900 | 0.900 |
| s820 | 52 | 9 | 22 | 19 | 13.64 | 8 | 0.136 | 0.158 | 0.333 | 0.333 |
| s953 | 40 | 9 | 34 | 33 | 2.94 | 16 | 0.147 | 0.152 | 0.556 | 0.556 |
| s1196 | 79 | 6 | 14 | 11 | 21.43 | 1 | 0.357 | 0.455 | 0.833 | 0.833 |
| s1196 | 2 | 11 | 47 | 38 | 19.15 | 8 | 0.213 | 0.263 | 0.909 | 0.909 |
| s1196 | 3 | 6 | 21 | 17 | 19.05 | 1 | 0.190 | 0.235 | 0.667 | 0.667 |
| s1196 | 22 | 12 | 53 | 43 | 18.87 | 8 | 0.208 | 0.256 | 0.917 | 0.917 |
| s1423 | 90 | 11 | 37 | 26 | 29.73 | 1 | 0.297 | 0.423 | 1.000 | 1.000 |
| s1423 | 44 | 7 | 48 | 35 | 27.08 | 1 | 0.146 | 0.200 | 1.000 | 1.000 |
| s1423 | 14 | 9 | 42 | 32 | 23.81 | 1 | 0.143 | 0.188 | 0.667 | 0.667 |
| s1423 | 62 | 8 | 48 | 37 | 22.92 | 1 | 0.146 | 0.189 | 0.875 | 0.875 |
| s5378 | 72 | 7 | 43 | 29 | 32.56 | 1 | 0.140 | 0.207 | 0.857 | 0.857 |
| s5378 | 41 | 12 | 39 | 33 | 15.38 | 1 | 0.231 | 0.273 | 0.750 | 0.750 |
| s5378 | 1 | 11 | 48 | 41 | 14.58 | 1 | 0.229 | 0.268 | 1.000 | 1.000 |
| s5378 | 86 | 10 | 45 | 39 | 13.33 | 2 | 0.222 | 0.256 | 1.000 | 1.000 |
| s9234 | 7 | 14 | 85 | 73 | 14.12 | 1 | 0.153 | 0.178 | 0.929 | 0.929 |
| s9234 | 5 | 7 | 29 | 26 | 10.34 | 1 | 0.172 | 0.192 | 0.714 | 0.714 |
| s9234 | 80 | 14 | 141 | 127 | 9.93 | 1 | 0.092 | 0.102 | 0.929 | 0.929 |
| s9234 | 23 | 14 | 81 | 73 | 9.88 | 4 | 0.136 | 0.151 | 0.786 | 0.786 |
| s13207 | 50 | 14 | 143 | 87 | 39.16 | 1 | 0.098 | 0.161 | 1.000 | 1.000 |
| s13207 | 41 | 12 | 93 | 70 | 24.73 | 1 | 0.118 | 0.157 | 0.917 | 0.917 |
| s13207 | 56 | 14 | 79 | 60 | 24.05 | 1 | 0.127 | 0.167 | 0.714 | 0.714 |
| s13207 | 31 | 11 | 63 | 48 | 23.81 | 8 | 0.159 | 0.208 | 0.909 | 0.909 |
| s15850 | 39 | 12 | 94 | 59 | 37.23 | 16 | 0.117 | 0.186 | 0.917 | 0.917 |
| s15850 | 5 | 7 | 31 | 21 | 32.26 | 1 | 0.226 | 0.333 | 1.000 | 1.000 |
| s15850 | 85 | 7 | 84 | 69 | 17.86 | 1 | 0.071 | 0.087 | 0.857 | 0.857 |
| s15850 | 45 | 7 | 42 | 35 | 16.67 | 1 | 0.143 | 0.171 | 0.857 | 0.857 |
| s38417 | 0 | 8 | 61 | 33 | 45.90 | 1 | 0.131 | 0.242 | 1.000 | 1.000 |
| s38417 | 67 | 13 | 71 | 43 | 39.44 | 1 | 0.183 | 0.302 | 1.000 | 1.000 |
| s38417 | 11 | 15 | 90 | 70 | 22.22 | 8 | 0.167 | 0.214 | 1.000 | 1.000 |
| s38417 | 42 | 14 | 59 | 47 | 20.34 | 16 | 0.237 | 0.298 | 1.000 | 1.000 |
| s38584 | 93 | 15 | 80 | 68 | 15.00 | 1 | 0.175 | 0.206 | 0.933 | 0.933 |
| s38584 | 79 | 8 | 25 | 24 | 4.00 | 16 | 0.320 | 0.333 | 1.000 | 1.000 |
| s38584 | 92 | 14 | 33 | 32 | 3.03 | 32 | 0.394 | 0.406 | 0.929 | 0.929 |

diagnosis procedure will produce more accurate results based on $T_b$. This section describes experiments to demonstrate this effect.

### *A. Basic Setup and Results*

The defect diagnosis procedure from [24] is used in this section. The procedure receives as input the output response of a faulty circuit. It uses a set of modeled faults $F$ (single stuck-at faults for the experiments in this paper) to define a set of candidate faults. For every fault in $F$ it compares the output response in the presence of the fault to the output response of the faulty circuit. The comparison yields a score that measures the extent to which the output response of the fault matches that of the faulty circuit. The faults in $F$ are ranked based on their scores, and the highest ranked faults are included in the set of candidate faults. The procedure from [24] performs the ranking for every output separately to ensure that every output value is accounted for.

The procedure is applied to defects that consist of multiple stuck-at faults (different defects are considered later in this section). A defect $d_i = \{d_{i,0}, d_{i,1}, ..., d_{i,m_i-1}\}$ consists of $m_i$ single stuck-at faults that are present in the circuit together. The faults are selected randomly. For $d_i$ and a test set $T_b$, the procedure produces a set of candidate faults that is denoted by $C_{i,b}$. The following parameters measure the accuracy of diagnosis.

(1) The size of $C_{i,b}$ should be as small as possible.

(2) The overlap between $C_{i,b}$ and $d_i$ is defined as $V_{i,b} = C_{i,b} \cap d_i$. The overlap should be as large as possible.

(3) The ratio $|V_{i,b}|/|C_{i,b}|$ is also referred to as the diagnostic resolution. A higher ratio implies that more of the candidate faults match the defect that is present in the circuit. Therefore, the ratio should be as large as possible.

(4) The ratio $|V_{i,b}|/m_i$ is also referred to as the diagnostic precision. A higher ratio implies that more of the defects that are present in the circuit are included in the set of candidate faults. Therefore, the ratio should be as large as possible.

The effects of diagnostic test generation are studied for defects that produce large sets of candidate faults under $T_0$. A set of candidate faults $C_{i,0}$ for a defect $d_i$ of multiplicity $m_i$ is considered large if it contains $2m_i$ faults or more.

To obtain such defects, it is necessary to consider defects

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TABLE VII

DEFECT DIAGNOSIS (ITC-99)

| | | | cand | | cand red | | resol | | prec | |
|---|---|---|---|---|---|---|---|---|---|---|
| circuit | $i$ | $m_i$ | 0 | 32 | % | b | 0 | 32 | 0 | 32 |
| b03 | 51 | 6 | 23 | 17 | 26.09 | 1 | 0.217 | 0.294 | 0.833 | 0.833 |
| b03 | 57 | 10 | 25 | 20 | 20.00 | 1 | 0.400 | 0.500 | 1.000 | 1.000 |
| b03 | 11 | 5 | 19 | 16 | 15.79 | 1 | 0.211 | 0.250 | 0.800 | 0.800 |
| b03 | 28 | 10 | 31 | 27 | 12.90 | 1 | 0.226 | 0.259 | 0.700 | 0.700 |
| b04 | 7 | 12 | 29 | 24 | 17.24 | 1 | 0.276 | 0.333 | 0.667 | 0.667 |
| b04 | 73 | 10 | 24 | 20 | 16.67 | 2 | 0.417 | 0.500 | 1.000 | 1.000 |
| b04 | 68 | 9 | 19 | 16 | 15.79 | 16 | 0.368 | 0.438 | 0.778 | 0.778 |
| b04 | 24 | 12 | 26 | 22 | 15.38 | 8 | 0.423 | 0.500 | 0.917 | 0.917 |
| b05 | 6 | 12 | 31 | 21 | 32.26 | 1 | 0.258 | 0.381 | 0.667 | 0.667 |
| b05 | 66 | 11 | 28 | 20 | 28.57 | 1 | 0.286 | 0.400 | 0.727 | 0.727 |
| b05 | 75 | 9 | 32 | 24 | 25.00 | 1 | 0.250 | 0.333 | 0.889 | 0.889 |
| b05 | 82 | 8 | 38 | 29 | 23.68 | 1 | 0.132 | 0.172 | 0.625 | 0.625 |
| b07 | 0 | 5 | 14 | 11 | 21.43 | 8 | 0.214 | 0.273 | 0.600 | 0.600 |
| b07 | 36 | 9 | 23 | 20 | 13.04 | 1 | 0.261 | 0.300 | 0.667 | 0.667 |
| b07 | 17 | 7 | 26 | 23 | 11.54 | 1 | 0.192 | 0.217 | 0.714 | 0.714 |
| b07 | 4 | 9 | 43 | 39 | 9.30 | 1 | 0.163 | 0.179 | 0.778 | 0.778 |
| b08 | 85 | 8 | 30 | 8 | 73.33 | 4 | 0.133 | 0.500 | 0.500 | 0.500 |
| b08 | 38 | 8 | 39 | 14 | 64.10 | 1 | 0.077 | 0.214 | 0.375 | 0.375 |
| b08 | 19 | 5 | 23 | 17 | 26.09 | 4 | 0.217 | 0.294 | 1.000 | 1.000 |
| b08 | 47 | 7 | 18 | 15 | 16.67 | 2 | 0.278 | 0.333 | 0.714 | 0.714 |
| b09 | 73 | 7 | 17 | 11 | 35.29 | 8 | 0.353 | 0.545 | 0.857 | 0.857 |
| b09 | 70 | 8 | 19 | 16 | 15.79 | 1 | 0.316 | 0.375 | 0.750 | 0.750 |
| b09 | 44 | 10 | 44 | 38 | 13.64 | 1 | 0.136 | 0.158 | 0.600 | 0.600 |
| b09 | 79 | 6 | 23 | 20 | 13.04 | 8 | 0.261 | 0.300 | 1.000 | 1.000 |
| b10 | 66 | 5 | 16 | 9 | 43.75 | 2 | 0.250 | 0.444 | 0.800 | 0.800 |
| b10 | 96 | 10 | 23 | 16 | 30.43 | 2 | 0.174 | 0.250 | 0.400 | 0.400 |
| b10 | 18 | 6 | 17 | 12 | 29.41 | 2 | 0.353 | 0.500 | 1.000 | 1.000 |
| b10 | 98 | 10 | 22 | 16 | 27.27 | 8 | 0.227 | 0.312 | 0.500 | 0.500 |
| b11 | 87 | 10 | 27 | 17 | 37.04 | 1 | 0.185 | 0.294 | 0.500 | 0.500 |
| b11 | 71 | 6 | 24 | 17 | 29.17 | 1 | 0.250 | 0.353 | 1.000 | 1.000 |
| b11 | 19 | 7 | 30 | 22 | 26.67 | 16 | 0.100 | 0.136 | 0.429 | 0.429 |
| b11 | 89 | 5 | 26 | 20 | 23.08 | 2 | 0.192 | 0.250 | 1.000 | 1.000 |
| b14 | 43 | 7 | 41 | 26 | 36.59 | 1 | 0.146 | 0.231 | 0.857 | 0.857 |
| b14 | 35 | 12 | 53 | 37 | 30.19 | 8 | 0.151 | 0.216 | 0.667 | 0.667 |
| b14 | 90 | 10 | 41 | 31 | 24.39 | 1 | 0.122 | 0.161 | 0.500 | 0.500 |
| b14 | 31 | 14 | 52 | 40 | 23.08 | 1 | 0.192 | 0.250 | 0.714 | 0.714 |
| b15 | 50 | 12 | 50 | 42 | 16.00 | 1 | 0.180 | 0.214 | 0.750 | 0.750 |
| b15 | 42 | 15 | 144 | 121 | 15.97 | 1 | 0.076 | 0.091 | 0.733 | 0.733 |
| b15 | 95 | 14 | 54 | 46 | 14.81 | 1 | 0.204 | 0.239 | 0.786 | 0.786 |
| b15 | 48 | 11 | 35 | 30 | 14.29 | 1 | 0.286 | 0.333 | 0.909 | 0.909 |
| b20 | 93 | 14 | 53 | 40 | 24.53 | 1 | 0.245 | 0.325 | 0.929 | 0.929 |
| b20 | 51 | 12 | 128 | 102 | 20.31 | 1 | 0.070 | 0.088 | 0.750 | 0.750 |
| b20 | 79 | 15 | 63 | 51 | 19.05 | 1 | 0.222 | 0.275 | 0.933 | 0.933 |
| b20 | 13 | 14 | 50 | 42 | 16.00 | 1 | 0.240 | 0.286 | 0.857 | 0.857 |

with sufficiently high multiplicities. A higher multiplicity makes it more difficult to obtain a small and accurate set of candidate faults because of interactions between the faults. Defects with high multiplicities are prevalent in early stages of the yield improvement process for a new technology, justifying their consideration. For a circuit with $L$ lines, multiplicities between $log_4 L$ and $2log_4 L$ are used for this purpose.

For every defect $d_i$, the defect diagnosis procedure computes a set of candidate faults $C_{i,0}$ by using $T_0$. It uses $d_i$ for further analysis if $|C_{i,0}| \geq 2m_i$. In this case, the procedure also computes a set of candidate faults $C_{i,b}$ based on $T_b$, for $b = 1$, 2, 4, ..., 32. After computing $C_{i,0}$, the procedure uses $F = C_{i,0}$ for $b = 1$, $F = C_{i,1}$ for $b = 2$, and in general, $F = C_{i,b/2}$ for $b > 0$. This is sufficient for checking whether the use of $T_b$ narrows down the set of candidate faults relative to $T_{b/2}$, and it reduces the run time for defect diagnosis.

The procedure terminates after finding 100 defects with large sets of candidate faults under $T_0$.

TABLE VIII

DEFECT DIAGNOSIS (IWLS-05)

| | | | cand | | cand red | | resol | | prec | |
|---|---|---|---|---|---|---|---|---|---|---|
| circuit | $i$ | $m_i$ | 0 | 32 | % | b | 0 | 32 | 0 | 32 |
| aes_core | 81 | 8 | 17 | 15 | 11.76 | 8 | 0.471 | 0.533 | 1.000 | 1.000 |
| aes_core | 15 | 13 | 36 | 32 | 11.11 | 1 | 0.361 | 0.406 | 1.000 | 1.000 |
| aes_core | 80 | 14 | 56 | 50 | 10.71 | 1 | 0.250 | 0.280 | 1.000 | 1.000 |
| aes_core | 40 | 16 | 59 | 53 | 10.17 | 2 | 0.254 | 0.283 | 0.938 | 0.938 |
| des_area | 78 | 10 | 53 | 38 | 28.30 | 1 | 0.151 | 0.211 | 0.800 | 0.800 |
| des_area | 13 | 8 | 26 | 19 | 26.92 | 1 | 0.308 | 0.421 | 1.000 | 1.000 |
| des_area | 49 | 9 | 96 | 75 | 21.88 | 1 | 0.062 | 0.080 | 0.667 | 0.667 |
| des_area | 57 | 8 | 30 | 24 | 20.00 | 4 | 0.200 | 0.250 | 0.750 | 0.750 |
| i2c | 67 | 10 | 44 | 32 | 27.27 | 4 | 0.205 | 0.281 | 0.900 | 0.900 |
| i2c | 42 | 9 | 39 | 36 | 7.69 | 4 | 0.231 | 0.250 | 1.000 | 1.000 |
| i2c | 47 | 7 | 16 | 15 | 6.25 | 4 | 0.438 | 0.467 | 1.000 | 1.000 |
| i2c | 66 | 6 | 17 | 16 | 5.88 | 16 | 0.294 | 0.312 | 0.833 | 0.833 |
| pci_spoci_ctrl | 25 | 6 | 14 | 9 | 35.71 | 2 | 0.286 | 0.444 | 0.667 | 0.667 |
| pci_spoci_ctrl | 81 | 6 | 23 | 15 | 34.78 | 2 | 0.217 | 0.333 | 0.833 | 0.833 |
| pci_spoci_ctrl | 80 | 9 | 44 | 34 | 22.73 | 1 | 0.182 | 0.235 | 0.889 | 0.889 |
| pci_spoci_ctrl | 2 | 11 | 31 | 24 | 22.58 | 1 | 0.161 | 0.208 | 0.455 | 0.455 |
| sasc | 96 | 11 | 59 | 44 | 25.42 | 2 | 0.169 | 0.227 | 0.909 | 0.909 |
| sasc | 21 | 10 | 20 | 18 | 10.00 | 16 | 0.450 | 0.500 | 0.900 | 0.900 |
| sasc | 40 | 12 | 31 | 28 | 9.68 | 8 | 0.355 | 0.393 | 0.917 | 0.917 |
| sasc | 92 | 12 | 43 | 40 | 6.98 | 2 | 0.256 | 0.275 | 0.917 | 0.917 |
| simple_spi | 85 | 7 | 19 | 17 | 10.53 | 2 | 0.368 | 0.412 | 1.000 | 1.000 |
| simple_spi | 26 | 7 | 25 | 23 | 8.00 | 32 | 0.240 | 0.261 | 0.857 | 0.857 |
| simple_spi | 7 | 11 | 32 | 31 | 3.12 | 32 | 0.312 | 0.323 | 0.909 | 0.909 |
| spi | 85 | 9 | 36 | 30 | 16.67 | 2 | 0.167 | 0.200 | 0.667 | 0.667 |
| spi | 42 | 9 | 37 | 32 | 13.51 | 1 | 0.189 | 0.219 | 0.778 | 0.778 |
| spi | 12 | 8 | 30 | 26 | 13.33 | 1 | 0.267 | 0.308 | 1.000 | 1.000 |
| spi | 50 | 13 | 41 | 36 | 12.20 | 4 | 0.268 | 0.306 | 0.846 | 0.846 |
| steppermotordrive | 89 | 7 | 22 | 12 | 45.45 | 1 | 0.091 | 0.167 | 0.286 | 0.286 |
| steppermotordrive | 65 | 10 | 31 | 19 | 38.71 | 2 | 0.226 | 0.368 | 0.700 | 0.700 |
| steppermotordrive | 9 | 7 | 22 | 16 | 27.27 | 1 | 0.273 | 0.375 | 0.857 | 0.857 |
| steppermotordrive | 15 | 5 | 13 | 10 | 23.08 | 1 | 0.231 | 0.300 | 0.600 | 0.600 |
| systemcaes | 73 | 10 | 52 | 32 | 38.46 | 4 | 0.173 | 0.281 | 0.900 | 0.900 |
| systemcaes | 6 | 14 | 70 | 57 | 18.57 | 1 | 0.200 | 0.246 | 1.000 | 1.000 |
| systemcaes | 69 | 11 | 47 | 39 | 17.02 | 1 | 0.213 | 0.256 | 0.909 | 0.909 |
| systemcaes | 76 | 16 | 72 | 61 | 15.28 | 1 | 0.222 | 0.262 | 1.000 | 1.000 |
| systemcdes | 85 | 9 | 68 | 30 | 55.88 | 1 | 0.132 | 0.300 | 1.000 | 1.000 |
| systemcdes | 39 | 11 | 43 | 33 | 23.26 | 1 | 0.209 | 0.273 | 0.818 | 0.818 |
| systemcdes | 95 | 10 | 43 | 33 | 23.26 | 1 | 0.233 | 0.303 | 1.000 | 1.000 |
| systemcdes | 50 | 13 | 46 | 36 | 21.74 | 1 | 0.283 | 0.361 | 1.000 | 1.000 |
| tv80 | 25 | 11 | 58 | 49 | 15.52 | 2 | 0.172 | 0.204 | 0.909 | 0.909 |
| tv80 | 60 | 13 | 125 | 106 | 15.20 | 1 | 0.088 | 0.104 | 0.846 | 0.846 |
| tv80 | 32 | 14 | 51 | 44 | 13.73 | 1 | 0.275 | 0.318 | 1.000 | 1.000 |
| tv80 | 18 | 9 | 67 | 59 | 11.94 | 1 | 0.090 | 0.102 | 0.667 | 0.667 |
| usb_phy | 58 | 6 | 12 | 10 | 16.67 | 2 | 0.417 | 0.500 | 0.833 | 0.833 |
| usb_phy | 47 | 12 | 28 | 26 | 7.14 | 1 | 0.357 | 0.385 | 0.833 | 0.833 |
| usb_phy | 4 | 6 | 18 | 17 | 5.56 | 1 | 0.278 | 0.294 | 0.833 | 0.833 |
| usb_phy | 5 | 9 | 19 | 18 | 5.26 | 1 | 0.421 | 0.444 | 0.889 | 0.889 |
| wb_dma | 98 | 8 | 35 | 27 | 22.86 | 1 | 0.200 | 0.259 | 0.875 | 0.875 |
| wb_dma | 30 | 14 | 61 | 58 | 4.92 | 16 | 0.213 | 0.224 | 0.929 | 0.929 |
| wb_dma | 81 | 9 | 22 | 21 | 4.55 | 32 | 0.409 | 0.429 | 1.000 | 1.000 |
| wb_dma | 93 | 13 | 47 | 45 | 4.26 | 16 | 0.277 | 0.289 | 1.000 | 1.000 |

The additional diagnostic tests in $T_b$ target specific diagnostic holes that are not always relevant for a defect $d_i$. Therefore, the use of $T_b$ does not improve the results of defect diagnosis for every defect $d_i$. In addition, the defect diagnosis procedure does not always produce monotonic improvements in the results as more diagnostic tests are used. Tables VI-VIII report only on the defects where monotonic improvements are obtained. In these cases, the number of candidates is reduced starting at a certain value of $b$, the resolution is increased starting from this value, and the overlap and precision do not decrease.

For every circuit, Tables VI-VIII report on the four defects with the largest percentage reductions in the number of candidates.

Tables VI-VIII are organized as follows. After the circuit name, column $i$ shows the index of the defect $d_i$. Column $m_i$ shows its multiplicity $m_i$.

Column $cand$ shows the number of candidate faults in $C_{i,b}$, for $i = 0$ and 32. Reductions in the numbers of candidate faults may be obtained for $0 < b < 32$, but they are not reported directly.

Column $cand\ red$ subcolumn $\%$ shows the percentage reduction in the number of candidate faults between $C_{i,0}$ and $C_{i,32}$. Subcolumn $b$ shows the first value of $b$ where a reduction in the number of candidate faults is obtained.

Column $resol$ shows the resolution, $|V_{i,b}|/|C_{i,b}|$, for $b = 0$ and 32. Column $prec$ shows the precision, $|V_{i,b}|/m_i$, for $b = 0$ and 32.

The numbers of candidate faults in Tables VI-VIII are high because of the selection of defects with high multiplicities that are difficult to diagnose. When a commercial tool is applied to defects of similar multiplicities it produces similar numbers of candidate faults.

From Tables VI-VIII it can be observed that there are many cases where the use of a test set $T_b$, for $b > 0$, reduces the number of candidate faults significantly without reducing the overlap. The reduction in the number of candidates increases the diagnostic resolution. If further analysis is carried out in order to narrow down the set of candidate faults further, it is facilitated by the fact that the set of candidate faults is already smaller, increasing the resolution while preserving the precision.

There are additional cases, out of the 100 considered, that are not shown in Tables VI-VIII. For example, $s1423$ has 30 cases where the set of candidate faults is reduced between 2.27% and 29.73%; $s5378$ has 27 cases where the set of candidate faults is reduced between 1.49% and 32.56%; and $b04$ has 23 cases where the set of candidate faults is reduced between 2.00% and 17.24%.

These effects typically occur with $b \leq 16$, making it unnecessary to compute larger diagnostic test sets.

It is important to note that these effects occur even though the diagnostic holes are addressed by diagnostic tests for bridging faults, while the defects consist of multiple stuck-at faults. Consequently, these effects can be expected to be independent of the type of defects that are present in the faulty circuit.

### B. Additional Results

This subsection describes additional experiments to demonstrate different aspects of the approach described in this paper.

First, it is interesting to identify the smallest defect multiplicities that produce large sets of candidate faults, and require additional diagnostic tests as suggested here. For this study, the defect diagnosis procedure is applied to defects of multiplicities 2, 3, ..., $2log_4L$. For each multiplicity, 100 defects are selected randomly. A defect with the smallest multiplicity that benefits from additional diagnostic tests is reported in Table IX. The reported defect is the one with the largest percentage reduction in the number of candidate faults. This experiment requires large numbers of defects to be simulated, and it is applied only to several of the circuits.

TABLE IX
DEFECT DIAGNOSIS (SMALL MULTIPLICITY)

| circuit | $i$ | $m_i$ | cand 0 | cand 32 | cand red % | cand red b | resol 0 | resol 32 | prec 0 | prec 32 |
|---|---|---|---|---|---|---|---|---|---|---|
| s526 | 23 | 4 | 15 | 10 | 33.33 | 4 | 0.267 | 0.400 | 1.000 | 1.000 |
| s641 | 39 | 2 | 11 | 6 | 45.45 | 4 | 0.182 | 0.333 | 1.000 | 1.000 |
| s820 | 45 | 5 | 22 | 20 | 9.09 | 16 | 0.227 | 0.250 | 1.000 | 1.000 |
| s1196 | 78 | 3 | 18 | 11 | 38.89 | 2 | 0.167 | 0.273 | 1.000 | 1.000 |
| s1423 | 39 | 2 | 14 | 8 | 42.86 | 8 | 0.143 | 0.250 | 1.000 | 1.000 |
| b03 | 7 | 2 | 8 | 2 | 75.00 | 1 | 0.250 | 1.000 | 1.000 | 1.000 |
| b04 | 60 | 2 | 9 | 7 | 22.22 | 2 | 0.222 | 0.286 | 1.000 | 1.000 |
| b05 | 73 | 2 | 7 | 4 | 42.86 | 1 | 0.286 | 0.500 | 1.000 | 1.000 |
| b07 | 0 | 2 | 7 | 4 | 42.86 | 8 | 0.143 | 0.250 | 0.500 | 0.500 |
| b08 | 60 | 3 | 10 | 7 | 30.00 | 1 | 0.200 | 0.286 | 0.667 | 0.667 |
| des_area | 31 | 2 | 6 | 4 | 33.33 | 2 | 0.333 | 0.500 | 1.000 | 1.000 |
| pci_spoci_ctrl | 4 | 2 | 5 | 3 | 40.00 | 4 | 0.400 | 0.667 | 1.000 | 1.000 |
| sasc | 19 | 3 | 7 | 6 | 14.29 | 32 | 0.286 | 0.333 | 0.667 | 0.667 |
| steppermotordrive | 11 | 2 | 7 | 4 | 42.86 | 1 | 0.286 | 0.500 | 1.000 | 1.000 |
| usb_phy | 72 | 2 | 6 | 5 | 16.67 | 1 | 0.333 | 0.400 | 1.000 | 1.000 |

TABLE X
EXTENDED DIAGNOSTIC TEST GENERATION

| circuit | basic 0 | basic 32 | extended 0 | extended 32 |
|---|---|---|---|---|
| s526 | 60 | 108 | 115 | 149 |
| s641 | 42 | 55 | 76 | 83 |
| s820 | 133 | 187 | 302 | 350 |
| s953 | 88 | 95 | 125 | 131 |
| s1196 | 159 | 235 | 257 | 307 |
| s1423 | 71 | 251 | 199 | 324 |
| b03 | 28 | 32 | 40 | 46 |
| b04 | 56 | 64 | 104 | 107 |
| b05 | 70 | 216 | 165 | 283 |
| b07 | 60 | 65 | 94 | 99 |
| b08 | 66 | 84 | 374 | 381 |
| b09 | 29 | 32 | 249 | 254 |
| b10 | 51 | 67 | 97 | 115 |
| b11 | 77 | 115 | 202 | 234 |
| des_area | 139 | 219 | 254 | 306 |
| pci_spoci_ctrl | 169 | 232 | 266 | 318 |
| sasc | 53 | 77 | 234 | 249 |
| systemcdes | 96 | 213 | 182 | 251 |
| usb_phy | 44 | 96 | 100 | 132 |

Table IX demonstrates that there are defects with smaller multiplicities than the ones in Tables VI-VIII that produce large sets of candidate faults, and benefit from additional diagnostic tests based on distinguishable bridging faults.

It is also important to demonstrate that an extended diagnostic test set for single stuck-at faults does not obviate the need to address diagnostic holes. The diagnostic test set for single stuck-at faults is denoted by $T_0$. To obtain an extended test set for $T_0$, every pair of single stuck-at faults that are not distinguished by a fault detection test set $T_{sa}$ is targeted four times, to produce four diagnostic tests. These tests are added to $T_0$ to obtain a larger and more comprehensive test set than the basic one used earlier in this section. Diagnostic test generation for bridging faults is applied as before starting from the extended test set $T_0$.

The extended test sets obtained for several circuits are described in Table X. Column $basic$ repeats the number of tests in $T_0$ and $T_{32}$ from Tables III-V. Column $extended$ shows the number of tests in $T_0$ and $T_{32}$ using the extended test set.

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TABLE XI

DEFECT DIAGNOSIS (EXTENDED DIAGNOSTIC TEST SET)

| | | | cand | | cand red | | resol | | prec | |
|---|---|---|---|---|---|---|---|---|---|---|
| circuit | $i$ | $m_i$ | 0 | 32 | % | b | 0 | 32 | 0 | 32 |
| s526 | 30 | 7 | 36 | 30 | 16.67 | 8 | 0.194 | 0.233 | 1.000 | 1.000 |
| s641 | 64 | 5 | 29 | 22 | 24.14 | 16 | 0.103 | 0.136 | 0.600 | 0.600 |
| s820 | 32 | 9 | 51 | 38 | 25.49 | 4 | 0.098 | 0.132 | 0.556 | 0.556 |
| s953 | 19 | 7 | 20 | 16 | 20.00 | 16 | 0.350 | 0.438 | 1.000 | 1.000 |
| s1196 | 81 | 6 | 14 | 11 | 21.43 | 2 | 0.357 | 0.455 | 0.833 | 0.833 |
| s1423 | 75 | 6 | 25 | 19 | 24.00 | 4 | 0.200 | 0.263 | 0.833 | 0.833 |
| b03 | 40 | 5 | 19 | 12 | 36.84 | 1 | 0.211 | 0.333 | 0.800 | 0.800 |
| b04 | 6 | 12 | 29 | 27 | 6.90 | 8 | 0.276 | 0.296 | 0.667 | 0.667 |
| b05 | 66 | 11 | 31 | 20 | 35.48 | 1 | 0.258 | 0.400 | 0.727 | 0.727 |
| b07 | 16 | 5 | 17 | 13 | 23.53 | 16 | 0.294 | 0.385 | 1.000 | 1.000 |
| b08 | 7 | 8 | 18 | 15 | 16.67 | 8 | 0.222 | 0.267 | 0.500 | 0.500 |
| b09 | 37 | 10 | 22 | 19 | 13.64 | 1 | 0.227 | 0.263 | 0.500 | 0.500 |
| b10 | 78 | 6 | 15 | 11 | 26.67 | 8 | 0.333 | 0.455 | 0.833 | 0.833 |
| b11 | 72 | 6 | 31 | 21 | 32.26 | 2 | 0.194 | 0.286 | 1.000 | 1.000 |
| des_area | 77 | 13 | 76 | 50 | 34.21 | 1 | 0.145 | 0.220 | 0.846 | 0.846 |
| pci_spoci_ctrl | 8 | 11 | 56 | 42 | 25.00 | 4 | 0.125 | 0.167 | 0.636 | 0.636 |
| sasc | 24 | 12 | 35 | 34 | 2.86 | 4 | 0.286 | 0.294 | 0.833 | 0.833 |
| systemcdes | 51 | 11 | 42 | 32 | 23.81 | 1 | 0.262 | 0.344 | 1.000 | 1.000 |
| usb_phy | 68 | 9 | 30 | 27 | 10.00 | 1 | 0.300 | 0.333 | 1.000 | 1.000 |

TABLE XII

DEFECT DIAGNOSIS (MULTIPLE STUCK-AT AND BRIDGING FAULTS)

| | | | | cand | | cand red | | resol | | prec | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| circuit | $i$ | $m_i$ | br | 0 | 32 | % | b | 0 | 32 | 0 | 32 |
| s526 | 1 | 6 | 3 | 25 | 15 | 40.00 | 4 | 0.200 | 0.333 | 0.833 | 0.833 |
| s641 | 91 | 6 | 4 | 46 | 26 | 43.48 | 1 | 0.130 | 0.231 | 1.000 | 1.000 |
| s820 | 6 | 5 | 4 | 49 | 14 | 71.43 | 1 | 0.041 | 0.143 | 0.400 | 0.400 |
| s953 | 67 | 10 | 5 | 43 | 37 | 13.95 | 2 | 0.186 | 0.216 | 0.800 | 0.800 |
| s1196 | 20 | 10 | 4 | 64 | 42 | 34.38 | 2 | 0.125 | 0.190 | 0.800 | 0.800 |
| s1423 | 78 | 6 | 2 | 25 | 14 | 44.00 | 1 | 0.200 | 0.357 | 0.833 | 0.833 |
| b03 | 60 | 7 | 4 | 20 | 15 | 25.00 | 4 | 0.300 | 0.400 | 0.857 | 0.857 |
| b04 | 83 | 11 | 5 | 52 | 31 | 40.38 | 1 | 0.115 | 0.194 | 0.545 | 0.545 |
| b05 | 87 | 7 | 4 | 28 | 15 | 46.43 | 1 | 0.179 | 0.333 | 0.714 | 0.714 |
| b07 | 56 | 5 | 2 | 14 | 12 | 14.29 | 16 | 0.214 | 0.250 | 0.600 | 0.600 |
| b08 | 11 | 7 | 3 | 32 | 10 | 68.75 | 1 | 0.094 | 0.300 | 0.429 | 0.429 |
| b09 | 25 | 6 | 3 | 29 | 14 | 51.72 | 8 | 0.138 | 0.286 | 0.667 | 0.667 |
| b10 | 38 | 9 | 2 | 21 | 14 | 33.33 | 4 | 0.238 | 0.357 | 0.556 | 0.556 |
| b11 | 10 | 7 | 3 | 30 | 18 | 40.00 | 2 | 0.133 | 0.222 | 0.571 | 0.571 |
| des_area | 29 | 11 | 5 | 71 | 46 | 35.21 | 1 | 0.127 | 0.196 | 0.818 | 0.818 |
| i2c | 15 | 6 | 3 | 21 | 16 | 23.81 | 2 | 0.238 | 0.312 | 0.833 | 0.833 |
| pci_spoci_ctrl | 90 | 6 | 2 | 13 | 8 | 38.46 | 1 | 0.308 | 0.500 | 0.667 | 0.667 |
| sasc | 83 | 7 | 4 | 22 | 17 | 22.73 | 16 | 0.318 | 0.412 | 1.000 | 1.000 |
| simple_spi | 71 | 11 | 9 | 41 | 25 | 39.02 | 2 | 0.195 | 0.320 | 0.727 | 0.727 |
| steppermotordrive | 94 | 5 | 4 | 24 | 13 | 45.83 | 1 | 0.083 | 0.154 | 0.400 | 0.400 |
| systemcdes | 63 | 8 | 6 | 144 | 31 | 78.47 | 1 | 0.042 | 0.194 | 0.750 | 0.750 |
| usb_phy | 45 | 10 | 8 | 45 | 23 | 48.89 | 1 | 0.111 | 0.217 | 0.500 | 0.500 |

Table X demonstrates that the extended test set $T_0$ is, in many cases, larger than the test set $T_{32}$ obtained with the basic test set $T_0$.

The results of defect diagnosis using the extended test sets are shown in Table XI. In this case, only the defect with the largest percentage reduction in the number of candidates is reported. Additional defects with significant percentage reductions are obtained, but they are not reported since they show similar behavior to that observed earlier.

Table XI shows large percentage reductions in the numbers of candidates even with an extended diagnostic test set for single stuck-at faults. Thus, performing more diagnostic test generation for single stuck-at faults does not compensate for the diagnostic holes that are created by indistinguishable stuck-at fault pairs.

Finally, additional results of defect diagnosis are shown in Tables XII, XIII and XIV. For Table XII, a defect consists of multiple stuck-at and bridging faults that are selected randomly. Since the faults are selected randomly, the bridging faults are, in general, different from the ones used for diagnostic test generation. Defects that consist of faults of different types are more difficult to diagnose, especially since the defect diagnosis procedure uses only single stuck-at faults for defining sets of candidate faults. Thus, this experiment verifies that the results of defect diagnosis are improved even when the defects are more difficult to diagnose.

As in Table XI, only the defect with the largest percentage reduction in the number of candidates is reported in Table XII. Column $br$ of Table XII shows the number of bridging faults that are included in a defect of multiplicity $m_i$.

Table XII shows large percentage reductions in the numbers of candidates even with defects that are more difficult to diagnose.

For Table XIII, a defect consists of multiple stuck-at and realistic bridging faults that are selected randomly. Realistic bridging faults are obtained using the procedure described in [27]. In this case also, large percentage reductions in the numbers of candidates are obtained.

For Table XIV, a defect consists of multiple stuck-at, bridging and interconnect open faults that are selected randomly.

TABLE XIII

DEFECT DIAGNOSIS (MULTIPLE STUCK-AT AND REALISTIC BRIDGING FAULTS)

| | | | | cand | | cand red | | resol | | prec | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| circuit | $i$ | $m_i$ | br | 0 | 32 | % | b | 0 | 32 | 0 | 32 |
| s641 | 22 | 7 | 6 | 57 | 38 | 33.33 | 2 | 0.053 | 0.079 | 0.429 | 0.429 |
| s820 | 24 | 7 | 5 | 56 | 22 | 60.71 | 1 | 0.054 | 0.136 | 0.429 | 0.429 |
| s1196 | 88 | 11 | 11 | 39 | 26 | 33.33 | 1 | 0.103 | 0.154 | 0.364 | 0.364 |
| s1423 | 55 | 12 | 7 | 48 | 21 | 56.25 | 1 | 0.146 | 0.333 | 0.583 | 0.583 |
| s5378 | 79 | 7 | 6 | 49 | 28 | 42.86 | 1 | 0.082 | 0.143 | 0.571 | 0.571 |

TABLE XIV

DEFECT DIAGNOSIS (MULTIPLE STUCK-AT, BRIDGING AND INTERCONNECT OPEN FAULTS)

| | | | | | cand | | cand red | | resol | | prec | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| circuit | $i$ | $m_i$ | br | op | 0 | 32 | % | b | 0 | 32 | 0 | 32 |
| s526 | 64 | 9 | 0 | 5 | 49 | 20 | 59.18 | 1 | 0.102 | 0.250 | 0.556 | 0.556 |
| s641 | 9 | 8 | 3 | 3 | 35 | 22 | 37.14 | 1 | 0.143 | 0.227 | 0.625 | 0.625 |
| s820 | 23 | 5 | 4 | 1 | 40 | 16 | 60.00 | 4 | 0.075 | 0.188 | 0.600 | 0.600 |
| s953 | 17 | 9 | 3 | 5 | 29 | 23 | 20.69 | 4 | 0.138 | 0.174 | 0.444 | 0.444 |
| s1196 | 37 | 6 | 1 | 4 | 37 | 17 | 54.05 | 2 | 0.108 | 0.235 | 0.667 | 0.667 |
| s1423 | 48 | 7 | 2 | 5 | 47 | 23 | 51.06 | 1 | 0.106 | 0.217 | 0.714 | 0.714 |
| b03 | 1 | 8 | 2 | 3 | 17 | 11 | 35.29 | 4 | 0.294 | 0.455 | 0.625 | 0.625 |
| b04 | 36 | 8 | 2 | 4 | 38 | 28 | 26.32 | 1 | 0.184 | 0.250 | 0.875 | 0.875 |
| b05 | 59 | 12 | 4 | 6 | 50 | 27 | 46.00 | 1 | 0.160 | 0.296 | 0.667 | 0.667 |
| b07 | 55 | 5 | 1 | 2 | 23 | 12 | 47.83 | 1 | 0.174 | 0.333 | 0.800 | 0.800 |
| b08 | 83 | 5 | 2 | 2 | 35 | 13 | 62.86 | 1 | 0.086 | 0.231 | 0.600 | 0.600 |
| b09 | 12 | 8 | 3 | 5 | 25 | 9 | 64.00 | 1 | 0.080 | 0.222 | 0.250 | 0.250 |
| b10 | 63 | 6 | 4 | 1 | 61 | 25 | 59.02 | 2 | 0.066 | 0.160 | 0.667 | 0.667 |
| b11 | 26 | 5 | 2 | 2 | 18 | 9 | 50.00 | 2 | 0.111 | 0.222 | 0.400 | 0.400 |
| des_area | 39 | 14 | 6 | 6 | 74 | 44 | 40.54 | 1 | 0.108 | 0.182 | 0.571 | 0.571 |
| i2c | 98 | 8 | 2 | 4 | 43 | 31 | 27.91 | 16 | 0.140 | 0.194 | 0.750 | 0.750 |
| pci_spoci_ctrl | 34 | 9 | 4 | 5 | 32 | 21 | 34.38 | 2 | 0.219 | 0.333 | 0.778 | 0.778 |
| sasc | 35 | 11 | 2 | 7 | 42 | 24 | 42.86 | 2 | 0.190 | 0.333 | 0.727 | 0.727 |
| simple_spi | 3 | 12 | 5 | 5 | 38 | 25 | 34.21 | 8 | 0.289 | 0.440 | 0.917 | 0.917 |
| steppermotordrive | 81 | 7 | 3 | 4 | 36 | 18 | 50.00 | 1 | 0.083 | 0.167 | 0.429 | 0.429 |
| systemcdes | 38 | 12 | 0 | 10 | 89 | 33 | 62.92 | 1 | 0.067 | 0.182 | 0.500 | 0.500 |
| usb_phy | 64 | 6 | 2 | 4 | 33 | 13 | 60.61 | 16 | 0.121 | 0.308 | 0.667 | 0.667 |

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An interconnect open fault has either three or five aggressors. Column $br$ of Table XIV shows the number of bridging faults and column $op$ shows the number of interconnect open faults that are included in a defect of multiplicity $m_i$. Again, large percentage reductions in the numbers of candidates are obtained for these defects.

## VI. Concluding Remarks

This paper observed that a diagnostic hole occurs when a fault pair from a set of target faults cannot be distinguished. It also observed that it is possible to address diagnostic holes by targeting related fault pairs from a different fault model. The paper used this observation to enhance a diagnostic test set that is computed for single stuck-at faults. When a pair of single stuck-at faults is indistinguishable, the diagnostic test generation procedure described in the paper adds diagnostic tests for related pairs of bridging faults. Experimental results of defect diagnosis for defects that do not involve bridging faults in benchmark circuits demonstrated the importance of eliminating diagnostic holes.

Although the discussion was focused on single stuck-at faults and bridging faults, this new approach to diagnostic test generation can be applied with different fault models.

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