Covering Undetected Transition Fault Sites with Optimistic Unspecified Transition Faults under Multicycle Tests

Irith Pomeranz
School of Electrical and Computer Engineering
Purdue University
West Lafayette, IN 47907, U.S.A.
E-mail: pomeranz@ecn.purdue.edu

Transition faults require scan tests with two functional clock cycles between a scan-in and a scan-out operation to activate the faults and propagate their effects to observable outputs. Multicycle tests, with two or more functional clock cycles between scan operations, provide the following advantages. (1) They potentially increase the defect coverage by exercising the circuit at-speed for several functional clock cycles. (2) They allow test compaction to be achieved. (3) Multicycle tests can address features such as multiple clock domains and partial scan. (4) They create closer-to-functional operation conditions that are important for avoiding overtesting of delay faults.

This paper explores a different advantage of multicycle tests. The advantage is related to the importance of covering the sites of transition faults that are not detected by a transition fault test set. Undetectable transition faults may exist because of logic redundancies that prevent stuck-at faults, and therefore transition faults, from being detected. In addition, standard-scan allows only broadside or skewed-load tests to be applied, reducing the achievable fault coverage further. Transition faults can also be hard-to-detect, causing a test generation procedure to abort and leave transition faults undetected.

When multicycle tests are applied at-speed, the effects of a transition fault vary depending on the duration of the extra delay of the faulty line. In [1], transition faults at the same sites but with different durations are considered as separate faults. The duration of a fault is measured in numbers of clock cycles, and it can be equal to one, two, ... clock cycles. Consideration of transition faults with different durations under the model from [1] multiplies the number of faults by the maximum duration of a fault.

For the discussion in this paper, a standard transition fault is associated with an extra delay of a single clock cycle, and transition fault test sets are assumed to target standard transition faults. This keeps the number of transition faults equal to that used when two-cycle tests are considered. This is also a practice used by commercial tools when they consider transition faults under multicycle tests. The justification for the choice of an extra delay of a single clock cycle is that these faults tend to be the hardest to detect, and their tests tend to detect the faults with the larger extra delays.

Suppose that the standard transition fault $g : a \rightarrow a'$, which delays the $a \rightarrow a'$ transition on line g, remains undetected by a test set. In this case, the test set leaves the site of $g : a \rightarrow a'$ uncovered. Leaving uncovered fault sites implies that detectable defects around these sites may go undetected. This can lead to test escapes where faulty circuits would pass the test set.

The test compaction procedure developed in this paper for multicycle tests is based on the use of what are referred to as unspecified transition faults [2] to cover the sites of undetected standard transition

faults. Unspecified transition faults are defined to capture all the possible durations of a transition fault in a single fault. Consequently, the number of unspecified transition faults is equal to the number of standard transition faults. In addition, the complexity of checking the activation and propagation conditions for unspecified transition faults is the same as for standard transition faults. Nevertheless, an unspecified transition fault may be detectable by a multicycle test when the corresponding standard transition fault is undetectable. This is a result of the fact that transition faults in the same site but with different durations may be detectable or undetectable independently.

To ensure that as many unspecified transition faults as possible are detectable when standard transition faults are not, what are referred to as optimistic unspecified transition faults are used. The use of optimistic unspecified transition faults replaces the use of transition faults with different durations, which would have increased the number of target faults substantially.

An unspecified transition fault captures all the possible durations of a delayed signal-transition in a single fault by introducing unspecified (x) values into the faulty circuit when fault effects may occur. The unspecified values indicate that the occurrence of a fault effect depends on the duration of the fault. Fault detection is assumed to occur when an unspecified value reaches an observable output.

Extending the definition from [2], an optimistic unspecified transition fault $g : a \rightarrow a'$ is activated by two consecutive clock cycles if $g = a$ or x in the first clock cycle, and $g = a'$ or x in the second clock cycle. When the fault is activated, an unspecified value is assigned to g in the faulty circuit under the second clock cycle. The fault is referred to as optimistic because of the assumption that the conditions for the activation of the fault will be created even with unspecified values on g. This causes more unspecified values to propagate through the circuit. Since unspecified values do not cancel each other, this increases the likelihood that the fault will be detected.

The test compaction procedure is illustrated by Figure 1. The procedure accepts a two-cycle test set T_2 for transition faults. It produces multicycle test sets T_3, T_4, ... For $T \geq 2$, a test in T_L has at most L functional clock cycles. The test compaction procedure has the following features.

In a multicycle test, the primary input vector is kept constant during all the functional clock cycles. This avoids the need to change the primary input vector at-speed during the test. It also avoids the storage of primary input sequences.

A complete procedure for computing multicycle tests requires sequential test generation [3]. The procedure in Figure 1 follows the lines of the procedure from [4] and computes T_L from T_2 and T_{L-1} without performing sequential test generation. Given a two-cycle test, to produce an l-cycle test for $l > 2$, the procedure adds $l-2$ functional clock cycles to the test using the same primary input vector. In [4], the

Assign $L = 3$

Construct T_L from T_2 and T_{L-1}

Simulate T_L and define ta get faults

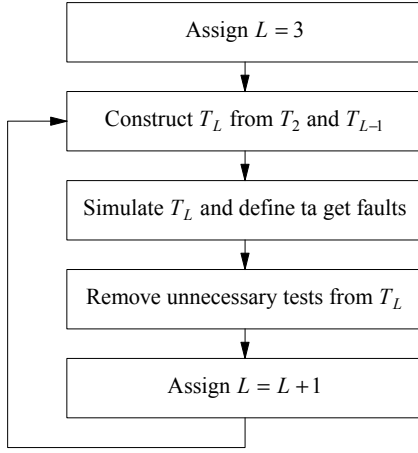Remove unnecessary tests from T_L

Assign $L = L + 1$

Fig. 1. Test compaction procedure

procedure also modifies the scan-in state and primary input vector of a test in order to increase the number of faults it detects. Experimental results for benchmark circuits show that this process is not needed when two-cycle tests are extended to detect optimistic unspecified transition faults. To create more variation in the multicycle test set, the procedure combines scan-in and primary input values from pairs of two-cycle tests. This results in a simulation-based procedure with a significantly lower computational complexity than the procedures from [3] or [4].

After T_L is created from T_2, T_{L-1} is added at its end to ensure that the fault coverage of T_L is at least as high as that of T_{L-1}. Next, fault simulation is carried out for T_L. During fault simulation, target unspecified optimistic transition faults are defined based on the undetected standard transition faults of T_L, and simulated. This is described by Procedure 1 next.

Procedure 1: Fault simulation and target faults for T_L

1) Let S be the set of standard transition faults. Simulate S under T_L. Let D_S be the subset of detected faults.
2) Assign $X = \emptyset$. For every fault $g : a \to a' \in S - D_S$, add the fault to X as an optimistic unspecified transition fault.
3) Simulate X under T_L. Let D_X be the subset of detected faults.

A combined transition fault coverage of T_L that takes into account both standard and optimistic unspecified transition faults is defined as $(|D_S| + |D_X|)/|S| \cdot 100\%$. Tests in T_L that are not necessary for achieving its combined fault coverage are removed.

The test compaction procedure is applied to benchmark circuits using $L \leq 16$. The results are shown in Table I as follows. The first row for every circuit describes the initial two-cycle test set, T_2, which is a compact two-cycle broadside test set for transition faults. The second row describes the test set obtained by the test compaction procedure with the last value of L where the standard or combined transition fault coverage is increased, or the number of clock cycles required for applying the test set is reduced.

For every test set T_L, column $tests$ subcolumn tot shows the number of tests. Subcolumn $ratio$ shows the ratio $|T_L|/|T_2|$. Column $func$ shows the average number of functional clock cycles in a test of T_L. Column $cycles$ subcolumn tot shows the number of clock cycles C_L required for the application of T_L. Subcolumn $ratio$ shows the ratio C_L/C_2. Column $trans$ shows the fault coverage of standard transition faults under subcolumn $stand$, and the combined transition fault coverage under subcolumn $comb$. Column $ntime$ shows the

TABLE I
EXPERIMENTAL RESULTS

circuit	L	tests		func	cycles		trans		ntime
		tot	ratio		tot	ratio	stand	comb	
s526	2	56	1.00	2.00	1309	1.00	57.700	57.700	1.00
s526	16	40	0.71	15.70	1489	1.14	57.700	77.091	364.90
s1423	2	69	1.00	2.00	5318	1.00	73.963	74.104	1.00
s1423	16	72	1.04	15.03	6484	1.22	74.069	81.342	434.07
s5378	2	180	1.00	2.00	32759	1.00	77.781	77.781	1.00
s5378	4	200	1.11	3.58	36694	1.12	77.781	77.989	27.42
s9234	2	355	1.00	2.00	81878	1.00	76.543	78.276	1.00
s9234	16	386	1.09	8.93	91683	1.12	76.543	79.375	489.13
s13207	2	349	1.00	2.00	234848	1.00	79.983	80.769	1.00
s13207	16	437	1.25	14.59	299396	1.27	79.983	83.902	497.16
s15850	2	262	1.00	2.00	157535	1.00	67.003	67.038	1.00
s15850	16	362	1.38	12.03	221066	1.40	67.003	71.228	531.79
s35932	2	30	1.00	2.00	53628	1.00	71.800	71.800	1.00
s35932	13	17	0.57	13.00	31325	0.58	71.800	73.492	223.41
s38417	2	648	1.00	2.00	1063060	1.00	97.106	97.123	1.00
s38417	16	822	1.27	12.63	1356808	1.28	97.154	97.586	521.86
s38584	2	536	1.00	2.00	780796	1.00	71.267	71.351	1.00
s38584	4	749	1.40	3.66	1091739	1.40	71.360	73.947	30.94
b05	2	104	1.00	2.00	3778	1.00	76.344	76.445	1.00
b05	16	72	0.69	15.01	3563	0.94	76.546	87.063	320.90
b11	2	73	1.00	2.00	2366	1.00	81.585	81.639	1.00
b11	16	50	0.68	15.58	2309	0.98	81.967	92.350	212.05
b14	2	207	1.00	2.00	51790	1.00	72.043	72.043	1.00
b14	16	301	1.45	10.98	77899	1.50	72.357	81.106	495.68
b15	2	488	1.00	2.00	219559	1.00	81.115	81.149	1.00
b15	16	686	1.41	14.23	316848	1.44	83.267	89.535	545.81
b20	2	306	1.00	2.00	152270	1.00	79.651	79.651	1.00
b20	16	492	1.61	12.51	249695	1.64	80.519	89.136	459.39
aes_core	2	311	1.00	2.00	165982	1.00	96.177	96.177	1.00
aes_core	16	121	0.39	16.00	66596	0.40	96.177	96.340	252.46
i2c	2	70	1.00	2.00	9228	1.00	60.862	60.862	1.00
i2c	16	85	1.21	11.84	12014	1.30	67.995	71.142	405.70
simple_spi	2	78	1.00	2.00	10505	1.00	76.702	76.806	1.00
simple_spi	16	75	0.96	13.01	10932	1.04	77.330	80.236	398.83
spi	2	865	1.00	2.00	200044	1.00	82.587	84.375	1.00
spi	16	865	1.00	15.55	211768	1.06	83.322	86.080	403.85
systemcaes	2	202	1.00	2.00	136414	1.00	88.735	88.735	1.00
systemcaes	16	232	1.15	15.61	159732	1.17	88.735	95.237	372.41
systemcdes	2	91	1.00	2.00	17662	1.00	96.089	96.089	1.00
systemcdes	16	33	0.36	16.00	6988	0.40	96.089	96.355	195.01
tv80	2	658	1.00	2.00	237897	1.00	82.023	82.034	1.00
tv80	16	1060	1.61	12.23	393866	1.66	83.025	93.509	446.46
wb_dma	2	175	1.00	2.00	92398	1.00	75.042	75.048	1.00
wb_dma	16	210	1.20	10.62	112583	1.22	75.381	76.093	421.43

normalized run time of the procedure, where the cumulative run time is divided by the run time for fault simulation of T_2.

From Table I it can be observed that, as L is increased, the increased number of functional clock cycles provides more opportunities for optimistic unspecified transition faults to be activated and detected. As a result, the coverage of optimistic unspecified transition faults increases. This translates into an increase in the combined transition fault coverage.

In general, the results demonstrate that it is not necessary to leave uncovered fault sites when target faults cannot be detected. Instead, a related fault model allows tests to be generated for these fault sites.

REFERENCES

[1] K.-T. Cheng, "Transition Fault Testing for Sequential Circuits", IEEE Trans. on Computer-Aided Design, Dec. 1993, pp. 1971-1983.
[2] I. Pomeranz and S. M. Reddy, "Unspecified Transition Faults: A Transition Fault Model for At-Speed Fault Simulation and Test Generation", IEEE Trans. on Computer-Aided Design, Jan. 2008, pp. 137-146.
[3] S. Y. Lee and K. K. Saluja, "Test Application Time Reduction for Sequential Circuits with Scan", IEEE Trans. on Computer-Aided Design, Sept. 1995, pp. 1128-1140.
[4] I. Pomeranz, "A Multi-Cycle Test Set Based on a Two-Cycle Test Set with Constant Primary Input Vectors", IEEE Trans. on Computer-Aided Design, July 2015, pp. 1124-1132.