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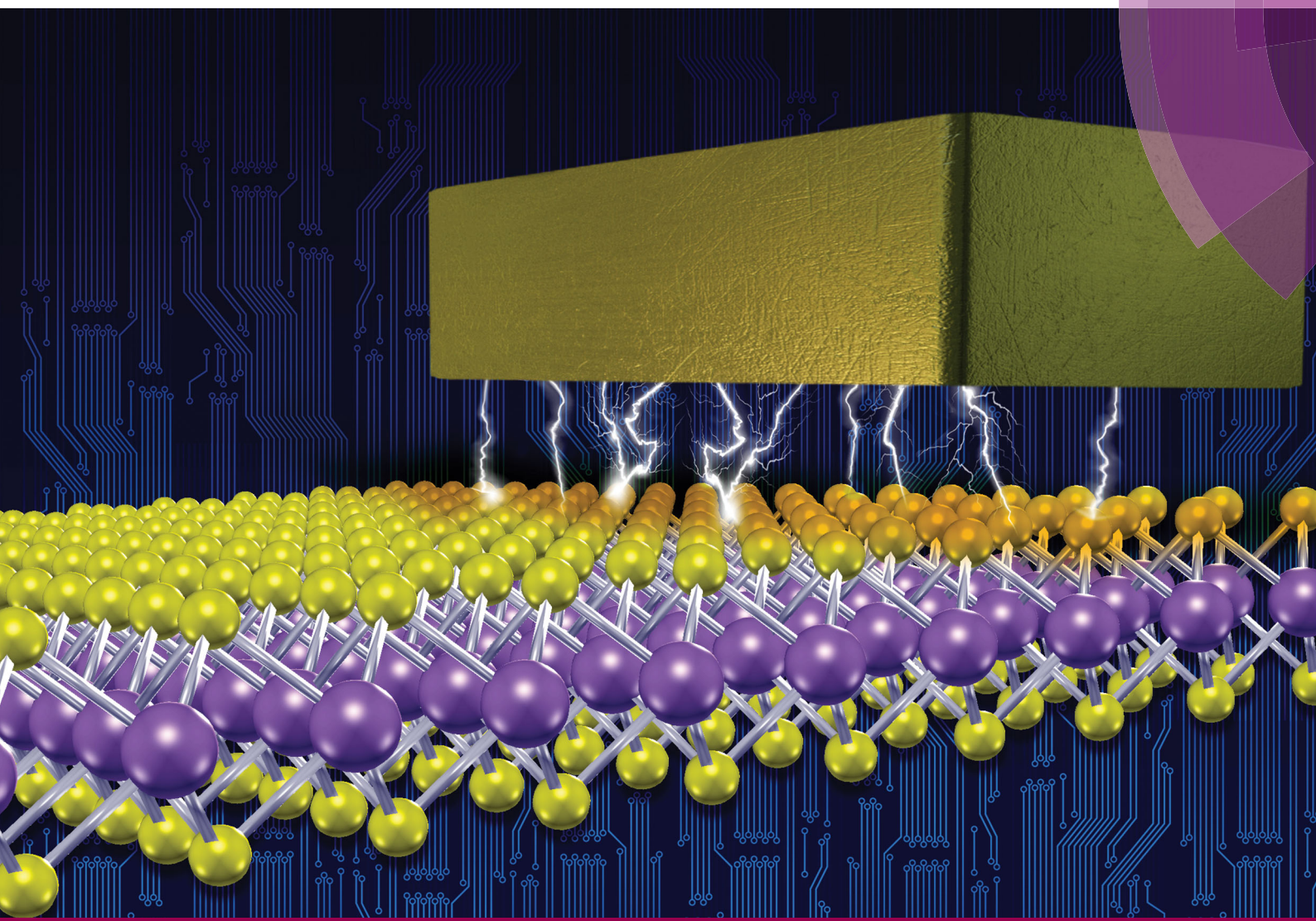

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Contact engineering for 2D materials and devices

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Over the past decade, the field of two-dimensional (2D) layered materials has surged, promising a new platform for studying diverse physical phenomena that are scientifically intriguing and technologically relevant. Contacts are the communication links between these 2D materials and the three-dimensional world for probing and harnessing their exquisite electronic properties. However, fundamental challenges related to contacts often limit the ultimate performance and potential of 2D materials and devices. This article provides a comprehensive overview of the basic understanding and importance of contacts to 2D materials and various strategies for engineering and improving them. In particular, we elucidate the phenomenon of Fermi level pinning at the metal/2D contact interface, the Schottky *versus* Ohmic nature of the contacts and various contact engineering approaches including interlayer contacts, phase engineered contacts, and basal *versus* edge plane contacts, among others. Finally, we also discuss some of the relatively under-addressed and unresolved issues, such as contact scaling, and conclude with a future outlook.

Introduction

The unprecedented technological success of the semiconductor industry over the last half-century has primarily been driven by silicon (Si) based technologies, at the center of which resides the complementary metal oxide semiconductor (CMOS) field effect transistor (FET) devices. During the golden era of CMOS evolution, relentless miniaturization of the device dimensions, more popularly known as the Moore's law of scaling, enabled

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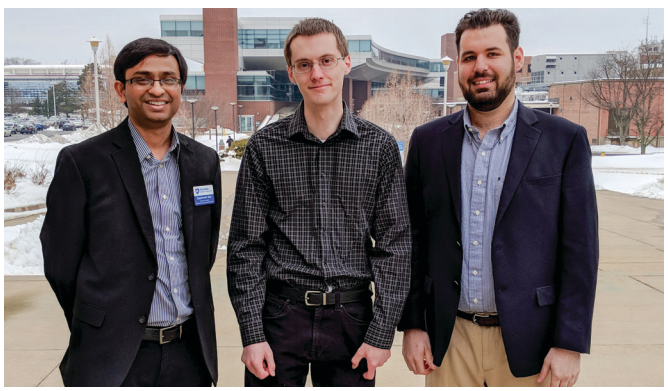

From left to right: Saptarshi Das, Andrew J. Arnold and Daniel S. Schulman

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faster and cheaper computing since exponentially more transistors could be placed into the same chip area, whereas scaling of the supply voltage ensured that the power density requirements for the integrated circuits (ICs) remained relatively constant.[1,2] However, in recent times the Si CMOS technology has encountered significant hardships in order to continue on its revolutionary trajectory. First, voltage scaling essentially stagnated around the year 2005 owing to fundamental thermodynamic limitations at the device physics level, which is governed by Boltzmann statistics. Now, the dimension scaling, which continued for another decade, albeit with multiple challenges, is nearing its end owing to fundamental quantum mechanical limitations at the material level.[3] Revival of the CMOS technology necessitates discovery of novel materials which can reinstate scaling and at the same time provide a solid foundation for innovative ultra-low power device concepts. In this context, two dimensional (2D) layered semiconductors have received significant attention owing to their atomically thin body nature, which enables aggressive length scaling without invoking detrimental short channel effects.[4,5] Furthermore, these 2D materials provide a unique platform for exquisite valley physics, exceptional excitonic effects, superior strain induced phase transition effects, and efficient quantum mechanical tunneling phenomena, which enable the development of beyond Boltzmann and non von-Neumann computational frameworks capable of delivering ultra-low power operation.[6–9] In fact, experimental results backed by theoretical calculations from the first generation of prototype 2D-devices show compelling evidence for their use as high performance and low power solutions for field effect transistors (FETs), radio frequency (RF) transistors, thin film transistor (TFTs), neuromorphic components, light emitting diodes (LEDs), solar cells, mechanical resonators, waveguides, and sensors of various types: chemical, biological, mechanical, optical, and thermal.[10–15]

However, as the field of 2D materials matures and the aforementioned ubiquitous 2D devices start to shrink in dimensions in order to further increase the performance and reduce the cost and power consumption, fundamental problems arise due to ''contacts''. Contacts are the communication links between these 2D materials and the three-dimensional world and are often overlooked by the scientific community. In this review article we will, therefore, emphasize the overwhelming importance of making good quality contacts to a wide variety of 2D layered materials for their implementation in future low power electronics, straintronics, flextronics, piezotronics, optoelectronics, valleytronics, neurotronics, and energy harvesting devices. We will begin with a general discussion of the 2D materials and their potential advantages over Si when implemented in a FET geometry. Next, we will discuss the fundamentals of metal/2D contacts, including the phenomenon of Fermi level pinning, which determines the Ohmic *versus* Schottky nature of the metal/2D contacts. We will also explain the characteristic features of carrier injection in a Schottky barrier (SB) 2D-FET and its impact in limiting both the ON state as well as OFF state performance of the device, and eventually elucidate on possible routes for improving the carrier injection through the SB. We will then move on to discuss the recently developed and material specific strategies for engineering low resistance contacts to various 2D materials, which include Fermi level depinning, hybridization and phase engineering, dimensional scaling (flake thickness and oxide thickness scaling), and even contact placement engineering (basal *versus* edge plane contacts). Finally, we will conclude with some of the unresolved and relatively under-explored aspects of metal/2D contacts.

Emergence of 2D semiconductors

The early era of 2D-electronics was primarily dominated by graphene due to its fascinating properties, such as electron–hole symmetry, high carrier mobility, optical transparency, and mechanical flexibility.[16–19] However, in recent years the field has rapidly expanded beyond graphene following the upsurge of semiconducting 2D materials with finite bandgaps (E_G). This includes compound semiconductors such as the transition metal dichalcogenides (TMDCs) with the general formula of MX_2 (where M represents the transition metal: Mo, W, Hf, Zr, Sn Re, *etc.* and X represents the chalcogen: S, Se, Te) and elemental semiconductors such as black phosphorus (BP) among others.[10,20] The trigonal prismatic 2H hexagonal structure common for the Mo and W based dichalcogenides is shown from the top view in Fig. 1a and from the side view in Fig. 1b where the layers are held together by weak van der Waals (vdW) interactions. Planes of metal atoms, *i.e.* Mo, are sandwiched between and bonded to six chalcogen atoms, *i.e.* S. In most electronic applications, charge transport occurs in-plane and the vdW gap can be considered a tunnel barrier acting as a resistance for free carriers moving between layers.[21] In bulk form, TMDCs have indirect bandgaps in the range of 0.9–1.6 eV.[22] However, when these TMDCs are scaled down to a single monolayer, an indirect to direct bandgap transition takes place due to quantum confinement effects increasing the bandgap range to 1.6–2.0 eV.[22] As the layer number decreases, the interaction between the d orbital of the transition metal and antibonding p_z orbital of the chalcogen atom decreases, increasing the conduction band minimum at the Γ point of the Brillouin zone and hence increasing the bandgap, *e.g.* in the case of MoS_2, from 1.2 eV in bulk to 1.85 eV in a monolayer.[23,24] Note that, in spite of several attempts to open up a bandgap, either through size quantization in graphene nanoribbons or electric fields in bi-layer graphene, the absence of a sizable bandgap at room temperature has limited the use of graphene in many electronic applications. A thorough review of graphene and its applications can be found elsewhere.[16–19,25–29] Semiconducting TMDCs, in contrast, offer natural and engineerable bandgaps, which was the central rationale behind these materials being integrated with mainstream semiconductor research.

2D field effect transistors (2D-FETs)

The 2D-FET structure most commonly used is shown in Fig. 1c. The back gated structure consists of a dielectric on a conductive substrate, usually 20–300 nm of thermally oxidized SiO_2 on

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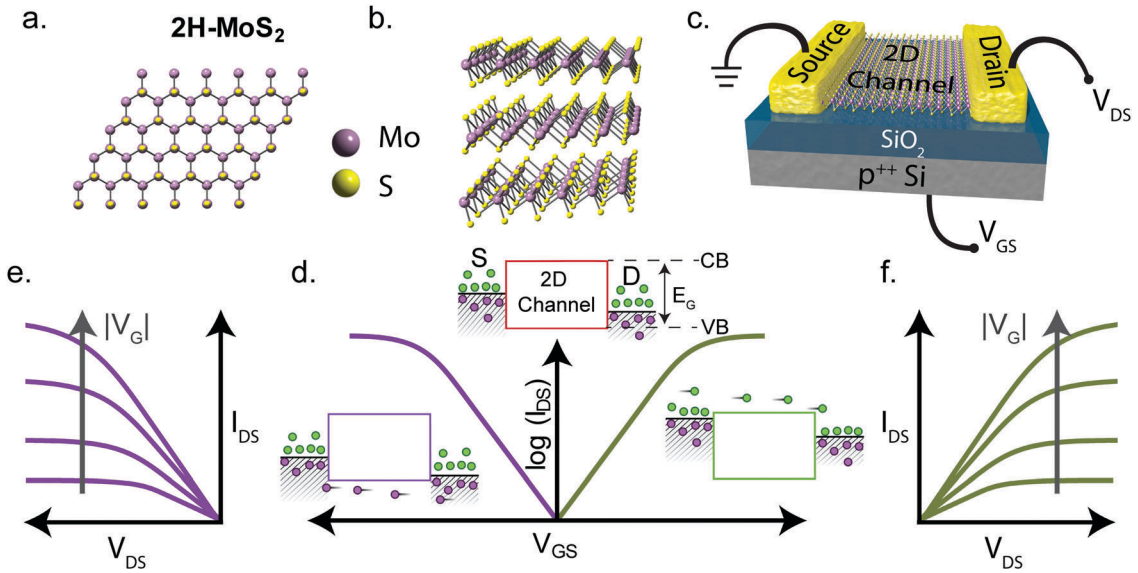

Fig. 1 2D field effect transistors (2D-FETs). (a) Top view and (b) side view of a representative transition metal dichalcogenide (TMDC), *e.g.* MoS_2, 2H crystal structure. The top view shows the hexagonal structure and the side view shows the van der Waals (vdW) layered structure. Planes of transition metal atoms (Mo) are sandwiched between and are bonded to 6 chalcogen (S) atoms. (c) Schematic of a typical back gated FET with a 2D semiconducting channel, *e.g.* MoS_2. The 2D material sits on a dielectric, frequently thermally grown SiO_2, which serves as a back-gate dielectric. Usually, highly doped p^{++} Si serves as the global back gate electrode. The source and drain contacts sit on top of the 2D material. (d) Ideal transfer characteristics (I_{DS} *versus* V_{GS}) of a 2D-FET with the inset showing the modulation of the conduction band (CB) and valence band (VB) *via* the applied gate voltage (V_{GS}) resulting in a band movement equal to the surface potential $q\Psi_S$. In the OFF state, the large barrier prevents thermal injection of carriers into the channel which is governed by the Fermi–Dirac distribution. In the ON state, the barrier is lowered, and carriers flow from the source to the drain. (e) p-Type, and (f) n-type output characteristics (I_{DS} *versus* V_{DS}) of a 2D-FET for different V_{GS} values. Ideal output characteristics, as expected, show typical linear and saturation regions.

heavily doped Si. The 2D material is either mechanically exfoliated, transferred onto, or directly grown on the dielectric and the contact metal is usually on top of the 2D material. The transistor is operated by grounding the source contact and applying a drain voltage, V_{DS}. The current in the device is modulated by applying a gate voltage, V_{GS}, to the global back gate. The ideal 2D-FET transfer characteristics (I_{DS} *versus* V_{GS}) are shown in Fig. 1d.[30] With no gate bias, *i.e.* $V_{GS} = 0$, the device is in the OFF state since large thermal barriers, governed by the Fermi-Dirac distribution, exist for the injection of both electrons into the conduction band (CB) and holes into the valence band (VB) as shown schematically using the middle band diagram in the inset of Fig. 1d. As such, the 2D channel remains highly resistive, preventing any current flow. When a positive voltage is applied to the gate, *i.e.* for $V_{GS} > 0$, the energy bands in the 2D channel are displaced downwards by an amount equal to the surface potential $q\Psi_S$, where q is the electronic charge. This allows the injection of electrons from the source into the conduction band of the 2D channel and as such current starts to flow as shown schematically using the right-hand band diagram in the inset of Fig. 1d. This thermionic electronic current initially increases exponentially with increasing magnitude of V_{GS} until the ON state, *i.e.* threshold condition ($V_{GS} = V_{TH}$), is reached where the so-called band movement nearly stops. Similarly, when a negative voltage is applied to the gate, *i.e.* for $V_{GS} < 0$, the energy bands in the 2D channel are displaced upwards allowing the injection of holes from the drain into the valence band of the 2D channel as shown schematically using the left-hand band diagram in the inset of Fig. 1d. The hole current also increases exponentially with increasing magnitude of V_{GS} until the ON state is reached. A transistor which shows both electron and hole branches in the transfer characteristics is conventionally referred to as an ambipolar FET. Fig. 1e and f show the output characteristics (I_{DS} *versus* V_{DS}) for the electron branch (n-type) and hole branch (p-type), respectively. As expected, one observes a linear Ohmic region as well as a current saturation region in the output characteristics of 2D-FETs. The reader should note that for high performance CMOS circuitry, both n-type and p-type transport are essential alongside Ohmic contacts. In the case of 2D materials, achieving n-type FETs and p-type FETs using a single material has been rather challenging. Furthermore, the contacts are most often Schottky in nature which limits carrier injection and ultimately the device performance.

Table 1 summarizes the performance of various state-of-the-art 2D-FETs. Of these, semiconducting MoS_2, referred to as 2H in a multilayer form and 1H in a monolayer form, is the most extensively studied since it produces n-type FETs with relatively low contact resistances (R_C), high ON currents (I_{ON}) and high ON/OFF ratios. MoS_2 is also air stable and naturally available in a single crystalline form, and can be seamlessly synthesized using chemical vapor deposition (CVD) techniques on various insulating substrates. Multilayered 2H-MoS_2 devices have demonstrated ON currents of up to 830 μA μm^{-1} and R_C down to 200 Ω μm while retaining ON/OFF ratios $>10^6$.[31,101] When benchmarking I_{ON} for various 2D-FETs, it is important to

Table 1 Summary of the state-of-the-art FETs based on various 2D materials with relevant parameters which include bandgap (E_G), polarity of transport (*i.e.* n-type, or p-type, or ambipolar), contact metal, contact resistance (R_C), thickness of the 2D material (t_{2D}), the channel length (L_{CH}), applied drain voltage (V_D), and calculated inversion charge density (Q_{inv}) corresponding to the maximum ON current (I_{ON})

Material	Polarity	E_g[a] (eV)	Contact metal	R_C (kΩ μm)	t_{2D}[h]	L_{CH} (μm)	V_D (V)	Q_{inv}[b] (cm^{-2})	I_{ON} (μA μm^{-1})	Ref.
2H-MoS_2	n	(B) 1.23[23]	Graphene/Ni[c]	0.54	10L	0.08	2	3×10^{13}	830	31
1H-MoS_2	n	(M) 1.85[24]	Au	0.48	1L	0.4	5	2×10^{14}	700	122
			1T/Au[d]	0.2		2	5	3×10^{12}	110	102
2H-$MoSe_2$	Ambipolar	(B) 1.09[23]	Ni	—	10L	2	5	5×10^{12}	n 26	123
2H-$MoTe_2$	p/ambipolar	(B) 0.93[124]	Pd/Ti/Au	—	15L	0.6	−4	1×10^{13}	p 100	125
2H-WS_2	n	(B) 1.35[23]	Cr/Au[e]	0.9	8L	0.5	2	6×10^{12}	65	126
2H-WSe_2	Ambipolar	(B) 1.35[127]	$Nb_{1-x}W_xSe_2$[f]	0.3	11L	0.27	−1.5	7×10^{12}	p 320	32
			Au	—	8L	2	5	8×10^{12}	n 300	33
1T-HfS_2	n	(B) 1.95[22]	Ti/Au	<2.7k	6L	1	2	1×10^{14}	750	128
1T-$HfSe_2$	n	(B) 0.9	Cr (MIS)[g]	50k–100k	8L	0.14	2.5	8×10^{12}	25	36
1T-$ZrSe_2$	n	(B) 1.1	Cr (MIS)[g]	—	6L	0.32	2.5	1×10^{13}	20	36
1T-SnS_2	n	(M) 2.0[129]	Ti/Au	—	1L	3.7	12	2×10^{13}	96	130
1T-ReS_2	n	(B) 1.5	Cr/Au	5k–175k	4L	7	1	5×10^{12}	0.35	131
1T-$ReSe_2$	Ambipolar	(B) 1.0[132]	Au	—	—	1.2	—	—	—	37
BP	p/ambipolar	(B) 0.36[39]	Sc/Au	—	19L	1	−3	8×10^{12}	p 580	40
		(M) 1.51[39]	Ti/Au	1.1k	20L	0.17	−2	3×10^{13}	p 300	41

[a] B: bulk/multilayer, M: monolayer. [b] $Q_{inv} = C_{OX}(V_{GS} - V_{TH})$. [c] Contact has a monolayer of graphene between the semiconductor and the metal. [d] Metal deposited on phase engineered metallic 1T MoS_2. [e] Channel n-doped with LiF. [f] $Nb_{0.005}W_{0.995}Se_2$ contacted h-BN encapsulated WSe_2 forms a 2D/2D low-resistance contact. [g] Metal insulator semiconductor (MIS) contact has 25 Å alumina between the Cr metal and 2D material. [h] Thickness given in number of layers.

indicate the inversion charge (Q_{inv}) in the semiconducting channel which is induced by the gate voltage, since $I_{ON} \propto \mu Q_{inv}$, where, μ is the carrier mobility. The mobility values are not listed in Table 1 as the reported values are usually SB limited and do not reflect the intrinsic value. A device gated to a higher Q_{inv} will have a higher I_{ON}, but this does not necessarily mean that the material and/or the contacts are superior. Other commonly studied 2H TMDCs are $MoSe_2$, $MoTe_2$, WS_2, and WSe_2. WS_2 typically produces n-type FETs similar to MoS_2, whereas $MoSe_2$, $MoTe_2$, and WSe_2 FETs show ambipolar characteristics with both electron and hole conduction. In the case of WSe_2 FETs, the ambipolar behavior is due to contacts pinning closer to the middle of the bandgap rather than near the conduction band as with MoS_2 as is discussed in later sections. On the other hand, the ambipolar behavior of $MoSe_2$ FETs is largely a result of its relatively smaller bandgap which is also discussed in later sections. Of these, WSe_2 FETs show the highest performance with R_C as low as 300 Ω μm and $I_{ON} >$ 300 μA μm^{-1} for both electron and hole conduction with Au and doped 2D contacts for n-type and p-type devices respectively.[32,33] WTe_2 is omitted because it has only been isolated in the semi-metallic distorted 1T′ polytype; although due to its high current densities it is promising for interconnect applications.[34]

While Mo and W TMDCs are stable in the semiconducting trigonal prismatic 2H polytype and semi-metallic octahedral 1T polytype,[35] most others, *e.g.* HfS_2, $HfSe_2$, $ZrSe_2$, SnS_2, ReS_2, and $ReSe_2$, exist in the semiconducting 1T polytype and are listed in Table 1. These materials are relatively unexplored compared to the 2H TMDCs, yet they possess unique physical and optoelectronic properties. Both $ZrSe_2$ and $HfSe_2$ form stable native oxides allowing natural integration of ultra-thin high-*k* dielectrics for efficient electrostatic gating which has previously been difficult for 2D materials through atomic layer deposition (ALD) techniques owing to the inert basal planes inhibiting uniform nucleation.[36] $ReSe_2$ FETs show ambipolar behavior and because of its distorted 1T structure that reduces the in-plane symmetry, it offers optoelectronic anisotropy.[37,38] The only dominantly p-type material listed in Table 1 is black phosphorus, an elemental 2D material with an anisotropic puckered structure. While the bandgap is always direct, it varies from 0.36 eV for bulk to 1.51 eV for monolayer.[39] High I_{ON} values of 300 μA μm^{-1} and 580 μA μm^{-1} for ∼20 layer devices with Ti and Sc contacts, respectively, have been achieved in BP-FETs. The predominant p-type transport with high ON current is primarily attributed to a much higher hole mobility (∼1000 cm^2 V^{-1} s^{-1}), in contrast to most 2D TMDCs, which exhibit n-type characteristics with typical mobility values in the range of several hundred cm^2 V^{-1} s^{-1}.[20,40,41]

Origin of metal/2D Schottky contacts

In conventional Si FETs, Ohmic contacts are realized through $n^+/p/n^+$ or $p^+/n/p^+$ substitutional/impurity doping profiles for electron (n-type) and hole (p-type) injection, respectively.[30] However, in the absence of such controllable and sustainable doping schemes, early demonstrations of 2D-FETs relied on the use of elemental metals with different work functions for carrier injection into the respective bands of the 2D channel. There has been some progress in doping 2D materials; however, these techniques are mostly surface electrostatic doping where a charged species on the surface results in the accumulation of electrons or holes in the semiconductor.[42] For example, potassium,[43] 1,2-dicholorethane,[44] benzyl viologen,[45,46] non-stoichiometric AlO_x,[47] and some self-assembled monolayers[48] have proven to be n-type dopants. Likewise, absorbed NO_2[49] and $AuCl_3$[45] act as p-type dopants. There have also been a few demonstrations of plasma doping to create diodes and p–n junctions using 2D semiconductors.[50–52] While some of these

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plasma doping methods can be limited to selected areas, such as contact regions, through conventional lithography processes, they also damage the 2D material through ion impacts. It is important to note that none of these doping methods have been applied experimentally to degenerately dope the 2D material underneath the contact regions in order to reduce the contact resistance. It is also possible to degenerately dope 2D TMDCs *via* direct substitutional doping through the introduction of a small amount of another material during the growth process.[32,53,54] However, because this doping occurs during the initial growth of the material, it is not possible to selectively dope only the contact areas.

Fig. 2a and b show calculated band alignments using density functional theory (DFT) for a variety of 2D materials in their multilayer/bulk and monolayer form respectively along with the work function, Φ_M, of commonly used contact metals. The energy of the conduction band, E_c, *versus* the vacuum level, E_{vac}, is given by the semiconductor electron affinity, χ_S. A low work function metal with the Fermi level aligned close to the conduction band of the 2D material will facilitate electron injection, whereas, a high work function metal with the Fermi level aligned close to the valence band of the 2D material will allow easier hole injection. Such metal–2D contacts are characterized by Schottky barriers (SBs) given by

$$\Phi_{SB\text{-}n} = \Phi_M - \chi_S, \quad \Phi_{SB\text{-}p} = E_G + \chi_S - \Phi_M \qquad (1)$$

In eqn (1), $\Phi_{SB\text{-}n}$ and $\Phi_{SB\text{-}p}$ are, respectively, SB heights for electron and hole injection and E_G is the bandgap of the semiconductor. However, in reality, semiconductors rarely form a SB at the Schottky limit given by eqn (1). Instead, the actual SB height lies between the Schottky and Bardeen limit. At the Bardeen limit, the metal Fermi level is pinned at the semiconductor interface state energy, Φ_{IS}. If these states arise from metal induced gap states (MIGS), they form at the charge neutrality level (E_{CNL}) which is calculated for various 2D materials in Fig. 2. For a given material, the actual SB height can be approximated by eqn (2), where S is the Schottky pinning factor. $S = 0$, indicates strong pinning, *i.e.* SB height is independent of the work function of the metal, while, as S approaches unity, the Bardeen limit converges to the Schottky limit.[55]

$$\Phi_{SB\text{-}n} = (S \times \Phi_{M\ -}\ \chi_S) + (1 - S)\Phi_{IS}, \quad S = \partial\Phi_{SB\text{-}n}/\partial\Phi_M \qquad (2)$$

Fig. 3a shows that regardless of the contact metal used, the transfer characteristics are primarily n-type for MoS_2 based 2D-FETs. Arrhenius type temperature dependent measurements show that the Fermi level of Sc, Ti, Ni, and Pt all pin near the conduction band as shown schematically in Fig. 3b. Sc and Pt at the Schottky limit should have a negative SB height of $\Phi_{SB\text{-}n} = -0.7$ eV and a positive SB height of $\Phi_{SB\text{-}n} = 1.4$ eV, respectively, but instead are only ~30 meV and ~230 meV, respectively. Fig. 3c plots the measured SB height for electron injection, *i.e.* $\Phi_{SB\text{-}n}$ for a variety of metals *versus* their work function where the best fit slope corresponds to a pinning factor of $S \sim 0.1$.[56–61] It should be noted that metals pin much closer to the conduction band than is predicted by the CNL in Fig. 2. In the case of WSe_2, metals pin much closer to the middle of the bandgap and ambipolar behavior is observed as seen in Fig. 3d.[62] Ni and Pd have similar average work function values of ~5.2 eV although the exact value depends on the crystal orientation and interface.[63] Based on eqn (1), both would be expected to form p-type contacts but are ambipolar, with $\Phi_{SB\text{-}n}$ of ~540 meV and ~820 meV for Ni and Pd, respectively.

A consensus on the origin of the Fermi level pinning has not yet arrived. Detailed surface studies of micromechanically exfoliated natural or geological MoS_2 flakes by R. Addou *et al.*, and S. McDonnell *et al.*, using scanning tunneling microscopy (STM), inductively coupled plasma mass spectrometry (ICPMS), and X-ray photoelectron spectroscopy (XPS) point towards high concentrations (~0.1–10%) of structural and metallic like defects, stoichiometric variations, chalcogen vacancies, and other elemental impurities to be responsible for the Fermi level pinning.[64,65] P. Bampoulis *et al.* used conductive AFM to directly measure the SBH of low concentration (~10^{11} cm^{-2}) subsurface metal-like defects (*i.e.* Mo-vacancies and antisite defects) and found that they had a much lower SBH and pinned more strongly, which decreased the pinning factor from $S \sim 0.3$ in the pristine region to $S \sim 0.1$ in the defect regions.[66] Work using Raman spectroscopy and DFT has also shown that the formation of nanoscale metal grains causes inhomogeneity and local strain between 1 and 2% which could dramatically affect the interface properties and electrical transport.[67–69] DFT calculations which assume ideal and defect free interfaces, point to different origins of Fermi level pinning. J. Kang *et al.* investigated contacts to monolayer MoS_2 and WSe_2 looking at the effect of the contact metal and geometry.[70] They identified three criteria for efficient electron injection: strong orbital overlap between the metal and the TMDC, a low SB height, and a narrow tunnel barrier. Mo and W were identified as good contact metals for MoS_2 and WSe_2, respectively. Since, these are the constituent transition metal elements in the corresponding TMDCs, the metal–TMDC separations are small leading to strong orbital overlap as well as thinner tunnel barriers, which ultimately benefit carrier injection. The Mo–MoS_2 and W–WSe_2 separations are 1.25 and 1.42 Å respectively, compared to 1.51–2.87 Å for other metals. Because the Mo and W work functions are not particularly low, with values of 4.5 eV and 4.6 eV respectively, it would appear that they should form relatively large SBs. However, the region underneath the contact is perturbed by the covalent bond formation, creating overlapped states, and in effect, an entirely new low work function Mo–MoS_2 or W–WSe_2 alloy. Hence, the $\Phi_{SB\text{-}n}$ for Mo–MoS_2 and W–WSe_2 is predicted to be much smaller than expected, with values of 0.13 and 0.35 eV respectively. Therefore, they fulfill all three criteria for low resistance n-type contacts.

C. Gong *et al.*, claimed two mechanisms are at play for the experimentally observed Fermi level pinning. First, charge redistribution at the interface between MoS_2 and the contact metal forms interface dipoles which modify the metal work function.[71] Their calculations show that for metals such as Al, the effective metal work function would increase, whereas for Ag, Au, Pd, and Pt, the effective metal work functions would decrease by 100's of meV. W. Saidi studied group I–IV metal

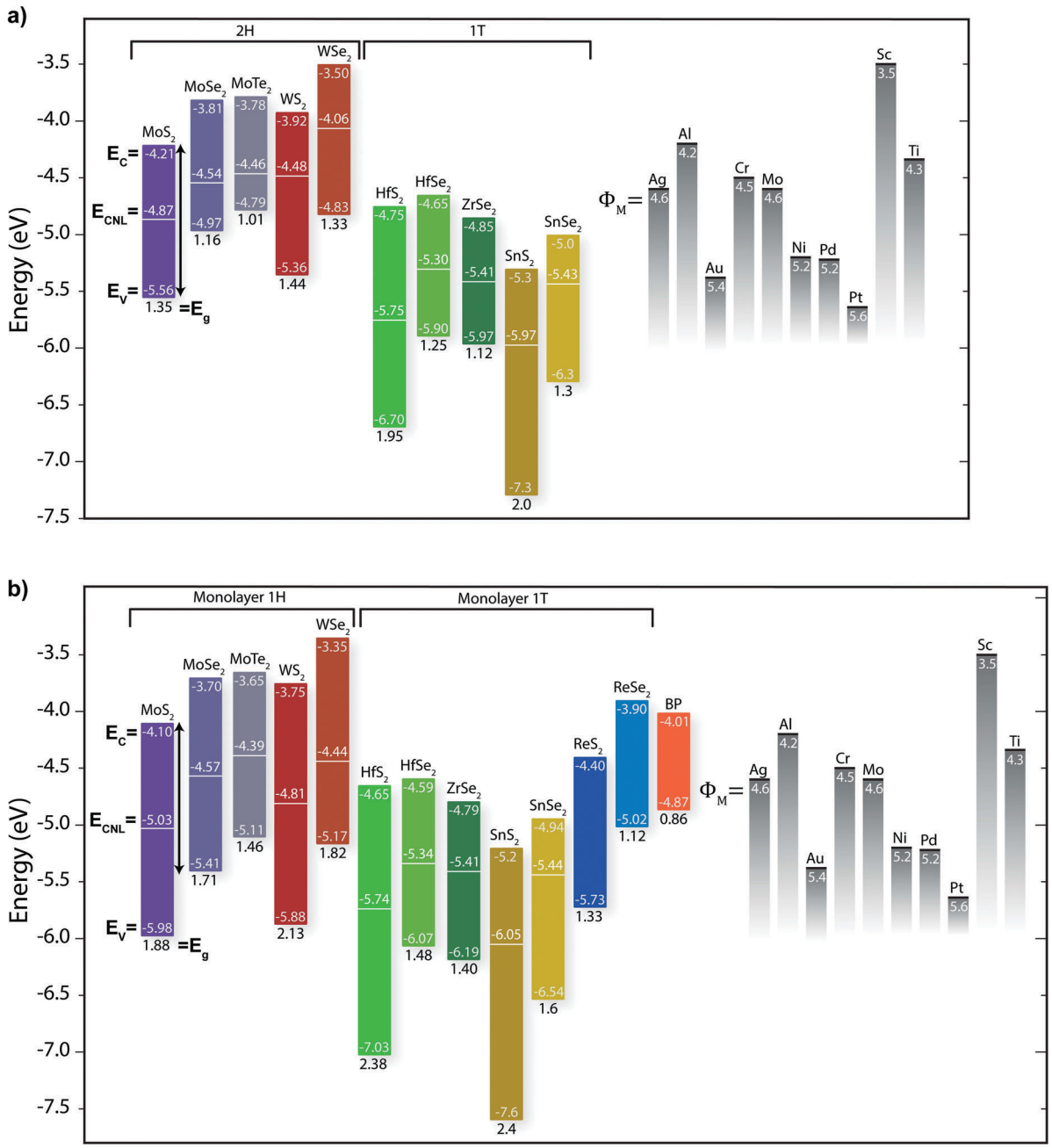

Fig. 2 Band alignment of various 2D materials and elemental contact metals. Schematic of bandgap, electron affinity, ionization potential, and charge neutrality level (CNL) values for (a) multilayer and (b) monolayer 2D materials along with the work functions Φ_M of common contact metals.[63] The electron affinity and ionization potentials are given by the energy of the conduction band minima, E_C, and valence band maxima, E_V, respectively *versus* the vacuum level. The charge neutrality level, E_{CNL}, is the energy at which metal induced gap states (MIGS) are predicted to form. In the case of MoS_2, this energy is further from the conduction band than experimentally shown by S. Das *et al.*[56] The Mo, W, Hf, Zr, and Sn based dichalcogenide values were computed using hybrid DFT [Perdew–Burke–Ernzerhof exchange model (PBE) + screened exchange (sX)] with dispersion corrections by Y. Z. Guo *et al.*[22] The electron affinity and ionization potentials for monolayer ReS_2, $ReSe_2$, and puckered black phosphorous are computed using semi-local (PBE) DFT with dispersion corrections by V. O. Ozcelik *et al.*[115] without any bandgap correction, hence underestimating the real bandgap. Note that BP and most TMDCs increase in bandgap when approaching the monolayer limit compared to bulk.[22,85] The band alignment between the metals and 2D materials does not take into account any Fermi level pinning. The metal work functions are either polycrystalline or averaged values for different crystal planes.[63]

adsorption on MoS_2 finding in all cases except for Au that the charge transfer resulted in net n-type doping of the MoS_2 and a work function reduction of the adatom/MoS_2 system.[72] However, the direction of charge transfer and hence dipole direction depends on the interface configuration as was shown in the case of Pt on MoS_2.[73] In the second mechanism proposed by

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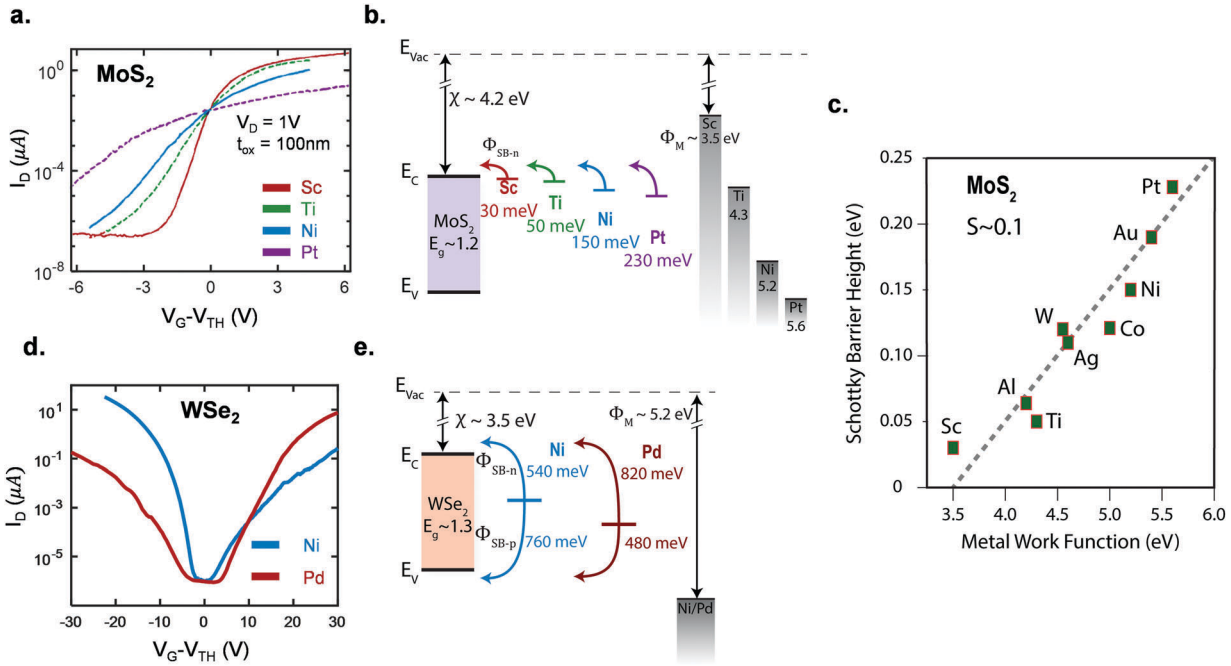

Fig. 3 Fermi level pinning at the metal/2D contact interface. (a) Transfer characteristics of exfoliated MoS_2 FETs using a 100 nm SiO_2 back gate dielectric with Sc, Ti, Ni, and Pt contact metals all showing unipolar n-type behavior. Adapted with permission from ref. 56. Copyright 2013 American Chemical Society. (b) The expected and actual metal MoS_2 band alignment showing Fermi level pinning near the conduction band.[56] (c) Experimentally extracted SB height, $\Phi_{SB\text{-}n}$, *versus* metal work function, Φ_M, for Sc,[56] Ti,[56] Ni,[56] Pt,[56] Ag,[57] W,[58] Co,[59] Au,[60] and Al[61] contact metals. The dotted line to guide the eye corresponds to a pinning factor, $S \sim 0.1$. (d) Transfer characteristics of exfoliated WSe_2 FETs using a 100 nm SiO_2 back gate dielectric with Ni and Pd contact metals both showing ambipolar behavior. Reprinted with permission from ref. 62. Copyright 2013, American Institute of Physics. (e) The expected and actual band alignment for Ni and Pd with WSe_2 showing mid-bandgap Fermi level pinning.[62]

C. Gong *et al.*, the interaction between the contact metal and the chalcogen component, *i.e.* S in the case of MoS_2, weakens the intra-layer Mo–S bonding, causing Mo d-states at the band edge to spread into the gap near the conduction band and thereby pinning the Fermi level. These states are distinctly different from MIGS which are independent of the metal. Using STM measurements, A. Kerelsky *et al.*, however, showed a significant local density of states which, near the interface, completely close the bandgap and penetrate up to 2 nm from the surface.[37] These states are relatively independent of the contact metal and therefore consistent with the MIGS theory. This is in conflict with the previous DFT study by C. Gong *et al.*, where the gap states depend on the metal's distance from and degree of interaction with the TMDC.[71] W. Chen *et al.* studied the electronic properties of monolayer MoS_2 adsorbed on Ir, Pd, and Ru substrates using first principles calculations and found partial Fermi level pinning and electron charge transfer to the MoS_2 resulting in n-type doping.[74] The pinning is consistent with the MIGS theory, but is less severe than what was extracted from the experimental results in Fig. 3c. This was attributed to the monolayer thickness, which limits the density of interface states formed and hence the degree of pinning.

I. Popov *et al.* looked closely at the impact of interface geometry and bonding, density of states (DOS), and potential barrier on the electronic transparencies of Ti and Au contacts to MoS_2.[75] They found that, in contrast to chemically unsaturated sulfur which forms favorable thiol bonds to Au, the sulfur in MoS_2 is fully saturated and does not bond strongly to Au. Consequently, Au forms a van der Waals type interface with the separation between the Au and MoS_2 calculated to be 2.62 Å, 0.2 Å longer than the sum of the Au and S covalent radii. Hence, charge injection occurs primarily *via* tunneling through a barrier that is relatively high (1.03 eV). The barrier is also considerably wide (1.59 Å) since charge is transferred from the Au to Mo states, and not from Au to S states as no significant S DOS exist at the Fermi level (E_F) at the Au–MoS_2 interface. The overall DOS is also very low and is primarily of Mo-4d_{z^2} character. Conversely, the separation between the Ti and MoS_2 was found to be 2.0 Å, 0.38 Å shorter than the sum of the Ti and S covalent radii. This strong S–Ti interaction results in a significantly larger DOS at E_F with additional states consisting of S-3sp and Mo-3d_{xy} character and theoretically, a metallic interface allowing direct charge injection. It should be noted, and is further discussed in later sections, that the ease of charge injection is only one component of the ultimate contact resistance. Experimental work shows that Ti contacts still exhibit tunneling limited injection, and although Au may appear to be a poor contact choice, Au contacted FETs have exhibited some of the lowest contact resistance values reported to date.[56,76] Regardless of the origin of Fermi level pinning, the effect is detrimental towards the realization of high performance FETs since it invariably results in poor carrier injection at the metal/2D contacts, irrespective of the metal or the TMDC material used.

Distinguishing features of SB-FETs

Fig. 4a shows the typical transfer characteristics of a Schottky contact FET. In SB-FETs, I_{DS} has two components: thermionic emission current ($I_{THERMAL}$) over the 'top' of the SB and thermally assisted tunneling current (I_{TUNNEL}) 'through' the SB. Both of these current components depend on the applied gate bias (V_{GS}), which modulates the band movement in the semiconducting channel through the aforementioned surface potential, $q\Psi_S$, as shown through the band diagrams in Fig. 4b–e. The readers should note that throughout the discussions in this review, it will be assumed that a large drain bias (V_{DS}) is applied to eliminate the effect of the SB at the drain contact. The thermionic current, $I_{THERMAL}$, is given by eqn (3a), where A is the Richardson's constant, T is the temperature, q is the electronic charge, k_B is Boltzmann's constant, and Φ_B is the effective thermal injection barrier, which is the sum of the true SB, $\Phi_{SB\text{-}n}$, and the surface potential, $q\Psi_S$. The surface potential, $q\Psi_S$, is given by eqn (3b), where V_{FB} is the flat band voltage, γ is the inverse band movement factor and C_S, C_{IT}, and C_{OX} are, respectively, the semiconductor capacitance, the interface trap capacitance, and the oxide capacitance. For an ultra-thin body fully depleted semiconducting channel, it is reasonable to assume $C_S = 0$ in the OFF state of the device operation.

$$I_{THERMAL} \approx AT^2 \exp\left(\frac{q\Phi_B}{k_B T}\right); \quad \Phi_B = \Phi_{SB\text{-}n} + q\Psi_S \tag{3a}$$

$$q\Psi_S \approx \left|\frac{V_{GS} - V_{FB}}{\gamma}\right|, \quad \gamma \approx 1 + \frac{C_S + C_{IT}}{C_{OX}} \tag{3b}$$

$$\begin{aligned} SS &= \left[\frac{d\log(I_D)}{dV_{GS}}\right]^{-1} = \left[\frac{d\log(I_D)}{d\Psi_S}\frac{d\Psi_S}{dV_{GS}}\right]^{-1} \\ &= \left[\frac{d\Psi_S}{dV_{GS}}\right]^{-1}\left(\frac{k_B T}{q}\ln 10\right) = \gamma \cdot \frac{60\text{ mV}}{\text{decade}} \end{aligned} \tag{4}$$

In the thermionic regime, $I_{DS} = I_{THERMAL}$ and as such, we see an exponential dependence of I_{DS} on V_{GS} in Fig. 4a with an inverse subthreshold slope (SS) of 60 mV decade^{-1} assuming one to one correspondence between the surface potential, $q\Psi_S$, and the applied gate bias, V_{GS}, *i.e.* $\gamma = 1$ as described through eqn (4). In all practical cases, a finite value of the interface trap capacitance C_{IT}, slows down the band movement and increases the SS by a factor, γ. The exponential dependence of I_{DS} on V_{GS} continues until the flat band voltage is reached, beyond which $I_{THERMAL}$ becomes practically constant and

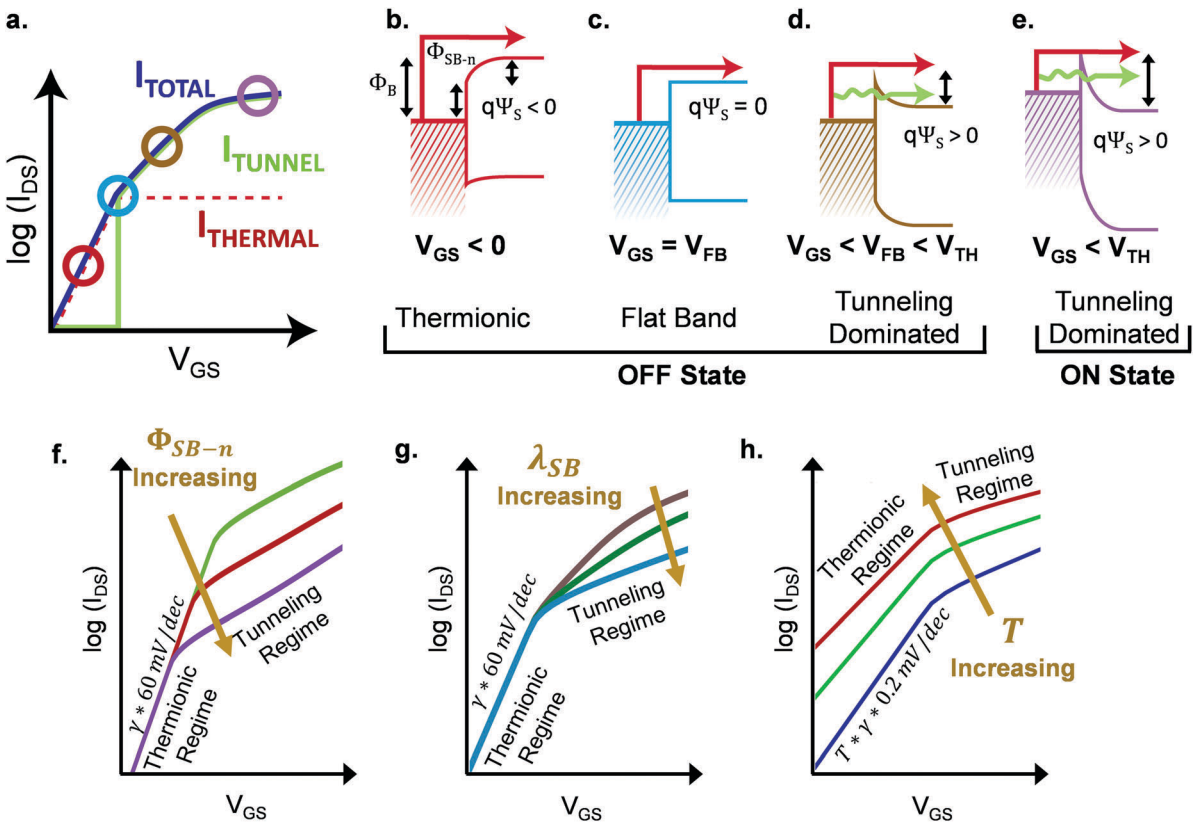

Fig. 4 Characteristics of Schottky barrier field effect transistors (SB-FETs). (a) Transfer characteristic of a typical SB-FET. The colored circles correspond to the thermionic regime (red), flat band condition (blue), OFF state tunneling dominated region (brown), and ON state tunneling dominated region (purple) with the corresponding band diagrams shown in (b)–(e) respectively. (f) Increasing the SB height, $\Phi_{SB\text{-}n}$, reduces the ON state current and lowers V_{GS} at which $V_{GS} = V_{FB}$. (g) Increasing the tunnel barrier width, λ_{SB}, reduces the slope of the tunneling regime and thereby reduces the ON current. (h) Increasing the temperature, T, reduces the thermionic subthreshold slope (SS) and increases both the thermionic and tunneling currents exponentially while increasing the OFF current.

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independent of V_{GS} as indicated by the red dashed line in Fig. 4a. For $V_{GS} > V_{FB}$, the band profile in the semiconducting channel changes as shown in Fig. 4d and e, enabling a thermally assisted tunneling current, I_{TUNNEL}. I_{TUNNEL} can be computed using eqn (5), where h is Planck's constant, m^* is the electron tunneling effective mass, $f(E)$ is the Fermi–Dirac distribution of the contact metal, $M_{2D}(E)$ is the number of 2D conducting modes in the semiconducting channel, and $T_{WKB}(E)$ is the SB transmission probability computed assuming a triangular potential barrier using the Wentzel–Kramers–Brillouin (WKB) approximation. Finally, λ_{SB} is the SB tunneling width which will be discussed in detail later. In this regime of carrier transport, the device current is the sum of the constant thermionic current and the tunneling current *i.e.* $I_{DS} = I_{THERMAL} + I_{TUNNEL}$. Here, the SS is tunneling limited, is no longer given by the expression in eqn (4), and is worse than the thermal limit of $\gamma \times 60$ mV decade^{-1}. In a SB-FET the current in the ON state, *i.e.* beyond the threshold voltage, V_{TH}, is completely dominated by I_{TUNNEL}. V_{TH} is defined as the gate voltage V_{GS} beyond which the band movement in the semiconducting channel ceases, or in other words the point where the surface potential becomes nearly constant.

$$I_{TUNNEL} = \frac{2q}{h}\int_{q\Psi_S}^{\Phi_{SB\text{-}n}} f(E)M_{2D}(E)T_{WKB}(E)\mathrm{d}E \quad (5a)$$

$$M_{2D}(E) = \frac{2\sqrt{2m^*(E - q\Psi_S)}}{h} \quad (5b)$$

$$T_{WKB}(E) = \exp\left(-\frac{8\pi}{3h}\sqrt{2m^*(\Phi_{SB\text{-}n} - E)^3}\frac{\lambda_{SB}}{q\Psi_S}\right) \quad (5c)$$

Fig. 4f, 4g and 4h, respectively, show the effect of SB height, $\Phi_{SB\text{-}n}$, SB width, λ_{SB}, and temperature, T, schematically on the transfer characteristics of an SB-FET. Reducing $\Phi_{SB\text{-}n}$, as expected, allows higher thermionic currents to be reached before the tunneling current dominates as shown in Fig. 4f. Reducing λ_{SB} on the other hand does not affect the thermionic regime but increases the tunneling probability and hence, improves the effective SS and ON current that can be reached for the same applied gate bias V_{GS} as shown in Fig. 4g. Since 2D materials are atomically thin, $\sim$0.65 nm at the monolayer limit, relatively thick oxides can still exhibit steep subthreshold slopes in the tunneling regime, which often confuses researchers into believing that Ohmic contacts have been achieved. In fact, as demonstrated by S. Das *et al.*, for relatively small SB heights, this culminates in linear output characteristics (I_{DS} *versus* V_{DS}), which is a trademark of Ohmic contact devices.[77] Linear "Ohmic type" I_{DS} *versus* V_{DS} characteristics are a necessary but, by no means, sufficient condition to claim Ohmic contacts.[56] This confusion can be readily eliminated once the temperature dependence of the transfer characteristics of an SB-FET, shown schematically in Fig. 4h, is acknowledged. Clearly, the SS in the thermionic regime has a linear temperature dependence following eqn (4), whereas the slope of the tunneling regime has a much weaker, nonlinear temperature dependence. It should be noted that, while the transmission probability through the SB is nearly temperature independent, the carrier distribution inside the metal is still given by the Fermi–Dirac distribution, which ultimately results in a relatively weak and non-linear temperature dependence of the SS in the tunneling assisted regime. In other words, tunneling current through a metal/semiconductor SB is always thermally assisted. It is to be emphasized that the extraction of the true SB height, no matter how small, is extremely important for benchmarking the ultimate performance of scaled 2D-FETs. A more detailed discussion on the extraction of SB height for different types of 2D-FETs can be found elsewhere.[78] Finally, the reader should also note that in order to mimic the true Ohmic contact scenario in a SB metal–semiconductor interface, one must realize a negative SB height, *i.e.* the metal Fermi level should align above the conduction band for electron injection and below the valence band for hole injection, respectively. For example, extensive research on carbon nanotubes (CNTs) demonstrated that a negative SB of $\Phi_{SB\text{-}n} \approx -0.25$ eV is required to achieve ON current levels in ballistic SB-CNTFETs which are on par with ballistic Ohmic-CNTFETs.[79] Negative SB heights have yet to be demonstrated for metal–TMDC contacts.

Enabling ambipolar transport in SB-FETs

As introduced earlier, ambipolar transport refers to the presence of both electron and hole branches in the transfer characteristics of a FET. While ambipolar FETs are not used in integrated circuits, they demonstrate the possibility of both n-type and p-type carrier transport in the semiconducting channel material, which is essential for a complementary logic design.[30] For Si, n-type (boron, aluminum, *etc.*) and p-type (arsenic, phosphorus, *etc.*) substitutional doping schemes are adopted in order to enable electron and hole transport, respectively. In the absence of substitutional doping, metal work function engineering can also achieve the same at the Schottky limit. In fact, even in light of strong Fermi level pinning at the metal/2D contact interface, work function engineering can be used to tune the ambipolar transport in 2D-FETs. For example, as shown in Fig. 5a, MoS_2 FETs with low work function Sc contacts ($\Phi_{Sc} \approx 3.5$ eV) show entirely n-type behavior owing to the small electron SB ($\Phi_{SB\text{-}n} \approx 30$ meV), and hence a naturally large hole SB ($\Phi_{SB\text{-}p} \approx 1.2$ eV). Note that the sum of the electron and hole Schottky barrier heights corresponds to the bandgap of the material *i.e.* $\Phi_{SB\text{-}n} + \Phi_{SB\text{-}n} = E_G$. However, by using an extremely high work function contact material such as MoO_x ($\Phi_{MoO_x} \approx 6.6$ eV) with the Fermi level aligned close to the valence band edge, predominantly p-type MoS_2-FETs were realized as shown in Fig. 5b. The effect of SB height on the ambipolar nature of the device characteristics is shown in Fig. 5c and d. Clearly, a small $\Phi_{SB\text{-}n}$ results in strong electron conduction and weak hole conduction (green curve), whereas, a large $\Phi_{SB\text{-}n}$ and hence a small $\Phi_{SB\text{-}p}$ results in strong hole conduction and weak electron conduction (purple curve). Symmetric electron and hole conduction are observed when the metal Fermi level pins close to the middle of the bandgap such that $\Phi_{SB\text{-}n} \approx \Phi_{SB\text{-}p}$ (red curve) at the cost of

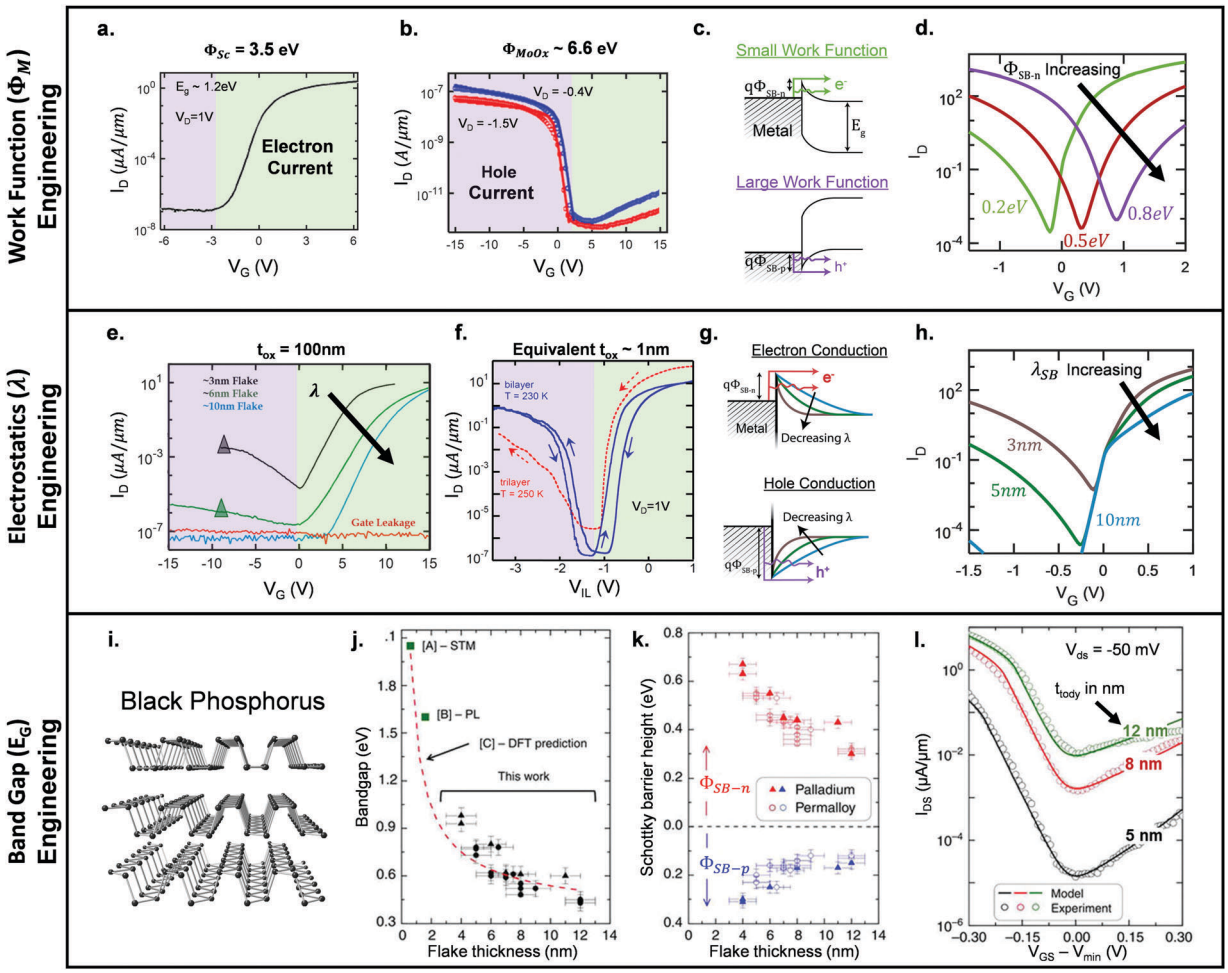

Fig. 5 Effect of metal work function, electrostatics and bandgap engineering on the ambipolar behavior of SB-FETs. (a) Transfer characteristics of an MoS_2 FET on a 100 nm SiO_2 back gate dielectric with low work function Sc contacts (Φ_{Sc} = 3.5 eV), which facilitate electron injection and restrict hole conduction since the electron SB height is much less than the hole SB ($\Phi_{SB\text{-}n} \ll \Phi_{SB\text{-}p}$). Adapted with permission from ref. 56. Copyright 2013 American Chemical Society. (b) Transfer characteristics of an MoS_2 FET on a 260 nm SiO_2 back gate dielectric with large work function MoO_x contacts (Φ_{Sc} = 6.6 eV), which, in contrast, allow hole injection and restrict electron conduction since $\Phi_{SB\text{-}p} \ll \Phi_{SB\text{-}n}$. Reprinted with permission from ref. 116. Copyright 2014 American Chemical Society. The effect of metal work function engineering is shown schematically in (c) and (d). Given a fixed bandgap, E_g, as $\Phi_{SB\text{-}n}$ increases, $\Phi_{SB\text{-}p}$ decreases resulting in an increase in hole current. (e) Scaling the MoS_2 flake thickness from 10 nm to 3 nm on a 100 nm SiO_2 back gate oxide thins the Schottky barrier tunneling width, λ_{SB}. As λ_{SB} decreases, an increase in electron, hole, and OFF state current is observed due to the increased tunneling probability of carriers through the Schottky barrier. Reprinted with permission from ref. 117. Copyright 2014 American Chemical Society. (f) Ionic liquid gated MoS_2 with an effective oxide thickness of ~1 nm shows a significantly better SS due to an improved λ_{SB} value. Reprinted with permission from ref. 81. Copyright 2013 American Chemical Society. (g and h) Show schematically the effect of λ_{SB}. (i) Puckered orthorhombic layered structure of black phosphorus. The non-planar structure gives rise to its anisotropic properties. (j) The bandgap has a strong layer number dependence with $E_G \sim 2$ eV at the monolayer limit and 0.36 eV in the bulk form as predicted from DFT and experimentally confirmed.[84,85,118,119] (k) The decreasing E_G results in layer thickness dependent electron and hole Schottky barrier heights for palladium and permalloy contact metals.[85] (l) Transfer characteristics of BP-FETs, where decreasing the flake thickness from 12 nm to 5 nm reduces the electron and hole injection barriers resulting in increasing electron, hole, and OFF state currents.[85] (j–l) Reprinted with permission from ref. 85.

reduced ON current for both the branches. As discussed in the next section, improved electrostatics can mitigate low ON currents of SB-FETs.

For ultra-thin body devices, the electrostatically determined SB tunneling width, λ_{SB}, is given by eqn (6), where t_{ox} and t_{body} are the thicknesses and ε_{ox} and ε_{body} are the dielectric constants of the gate oxide and the semiconducting channel respectively.[80]

$$\lambda_{SB} = \sqrt{\frac{\varepsilon_{body}}{\varepsilon_{ox}} t_{body} t_{ox}} \quad (6)$$

Given the exponential dependence of the tunneling probability in eqn (5c) on λ_{SB}, scaling of λ_{SB} can significantly improve the carrier injection into the respective bands of the semiconductor from the metal in a metal/2D SB contact. In fact, in the limiting case, *i.e.* when $\lambda_{SB} \rightarrow 0$, the SB can become completely transparent with perfect transmission (T_{WKB} = 1), irrespective of the height of the SB. Use of high-k and/or ultra-thin gate dielectrics in conjunction with atomically thin channel materials is critical for achieving ultra-scaled λ_{SB} values. Fig. 5e shows the evolution of MoS_2 SB-FETs from unipolar n-type devices to asymmetric ambipolar

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devices as a consequence of scaling λ_{SB}. Additionally, both the electron and hole ON currents increase significantly. This clearly shows that for Ni contacted MoS_2 SB-FETs, even though the SB height for hole injection is large ($\Phi_{SB\text{-}p} \approx 1.05$ eV), body thickness scaling improves the gate electrostatics and at the same time thins down the SB width, λ_{SB}, which ultimately increases the hole tunneling probability and hence the p-branch current. The minimum OFF state current, I_{min}, also increases as the SB no longer blocks hole tunneling from the drain contact. In Fig. 5f, λ_{SB} is scaled further, enabling near symmetric ambipolar MoS_2 SB-FETs by using ionic liquid gating, which offers an effective oxide thickness (EOT) of only $\sim$1 nm.[81] These effects are shown schematically in Fig. 5g and h.

Lastly, the bandgap of the semiconducting channel material also plays an equally important role in enabling ambipolar transport in SB-FETs. Black phosphorus, with a puckered orthorhombic structure as shown in Fig. 5i, is a classic system demonstrating such effects. Note that BP is the only other naturally occurring elemental 2D material beyond graphene. BP has recently been popular due to its anisotropic in plane properties owing to its non-planar structure, which enables implementation of artificial synapses, spintronic spin valves, and topologically insulating states.[9,82,83] The thickness induced bandgap change owing to quantum confinement is much more pronounced in BP: 0.36 eV in bulk and 1.51 eV in a monolayer as shown experimentally and from theoretical calculations in Fig. 5j.[39,84,85] Unlike TMDCs, where the bandgap transitions from indirect to direct only at the monolayer limit, the bandgap changes monotonically in BP with thickness and also remains direct for all thicknesses. With a bulk bandgap of $\sim$0.36 eV, BP bridges the gap between graphene, with no bandgap, and the TMDCs with bandgaps $>$1 eV. Because of the small bandgap, ambipolar transport is much more dominant than that in larger bandgap 2D semiconductors. Fig. 5k shows the layer number dependent SB height for electron and hole injection for Pd and Permalloy contacts. Similar to what was observed for MoS_2 in Fig. 5e, Fig. 5l shows how the electron, hole, and OFF current strongly depend on the flake thickness due to a combined reduction in λ_{SB} but primarily from the change in bandgap and reduction in both $\Phi_{SB\text{-}n}$ and $\Phi_{SB\text{-}p}$. Compared to larger bandgap materials, both $\Phi_{SB\text{-}n}$ and $\Phi_{SB\text{-}p}$ are relatively small, only a few 100 meV once the BP thickness gets to be a few nm. For FETs, this has a dramatic effect. At small drain biases of $V_{DS} = -0.1$ V, the BP FET has a reasonable ON/OFF ratio of $\sim 10^3$. However as V_{DS} increases up to -2 V, the ON/OFF ratio decreases to 8.4 as both electrons and holes are easily injected from the drain and source contacts, respectively.[41] Without the ability to effectively block charge injection, applications for BP in digital logic requiring ON/OFF ratios of $>10^4$ are limited unless the contacts can be properly engineered.

Benchmarking contact engineering strategies

As was discussed earlier, one of the primary factors limiting device performance and scalability of 2D-FETs is the large contact resistance resulting from the presence of Schottky barriers at the contacts. Various techniques have been investigated and are reviewed here to lower the contact resistance in 2D-FETs.

Fermi-level depinning

The simplest contact engineering strategy is to change the contact metal and thereby modulate the SB height. For example, low work function metal contacts such as scandium (Sc) have been shown to lower the SB height to $\sim$30 meV and significantly reduce the contact resistance in MoS_2 SB-FETs to values of 0.65 kΩ μm.[21,56] However, due to the phenomenon of strong Fermi level pinning, the range over which the barrier can be adjusted is relatively small and the technique is only effective if the pinning location is near one of the band edges. The influence of the metal work function can be improved by depinning the Fermi level. If the depinning is complete, *i.e.* if the Schottky limit is reached, Ohmic contacts can be seamlessly realized for most of the 2D TMDCs by selecting a metal from Fig. 2 with the Fermi level lying above the conduction band or below the valence band for n-type or p type 2D-FETs, respectively.

While the origin of Fermi level pinning is still contested within the academic community as was mentioned earlier, DFT simulations show that Fermi level pinning is at least partially dependent on metal–semiconductor interactions which induce states within the bandgap near the interface in a manner consistent with the MIGS theory.[37,71] Therefore, if the two materials are spatially separated, the density of the MIGS and hence the extent of the pinning will be reduced. This is most easily accomplished by inserting an ultra-thin insulating layer between the metal and the 2D TMDC as shown schematically in Fig. 6a. The insulating layer attenuates the metal electron wave function before it penetrates the 2D semiconductor, reducing the density of MIGS and as such prevents the intrinsic Fermi level from moving towards the charge neutrality level (E_{CNL}).[86] Furthermore, dipole formation at the insulator–semiconductor interface can also reduce the effective SB height. However, an insulating interlayer also introduces an additional tunnel barrier for the carrier injection. Consequently, as the interlayer thickness is increased, there is a tradeoff between a reduction in SB height that improves the contact resistance and a decrease in the transmission probability though the tunnel barrier which increases the contact resistance. This leads to an optimal intermediate value of the interlayer thickness as shown in Fig. 6b.

The band alignment and the dielectric constant of the interlayer also play an equally important role in determining the desired interlayer thickness as they determine the exponential electron wave function decay in the interlayer and therefore the MIGS density, as well as the carrier tunneling probability. For example, S. Lee *et al.* demonstrated that inserting a 1.5 nm thick Ta_2O_5 layer between the Ti contact and the CVD grown MoS_2 channel resulted in 2–3 orders of magnitude reduction in the specific contact resistivity (ρ_C) owing to a reduction in the SB height from $\sim$95 meV to $\sim$30 meV.[87] However, as the Ta_2O_5 thickness is increased beyond 1.5 nm, ρ_C starts to increase

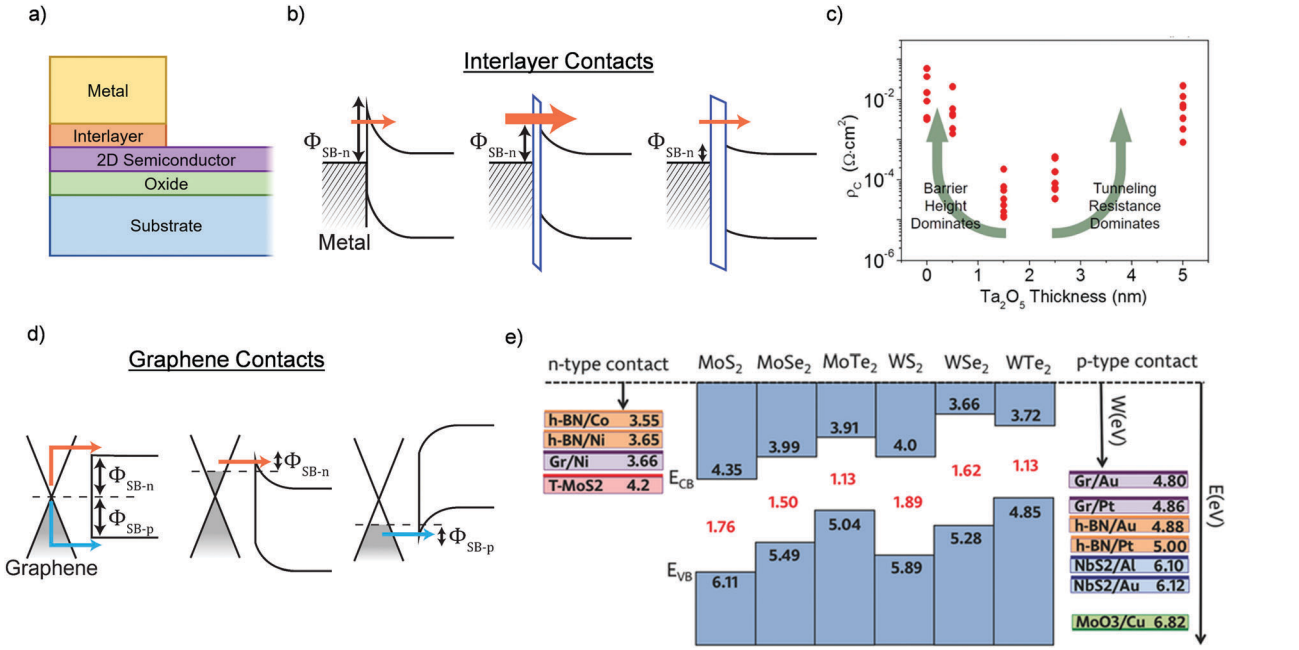

Fig. 6 Contact engineering strategies for Fermi level depinning: (a) schematic of a top contact to a 2D semiconductor with a thin interlayer between the metal and semiconductor. (b) Band diagrams showing the effect of interlayer tunnel barrier thickness on the Fermi level pinning and current injection. With no interlayer, there is a large SB and therefore low current. As the barrier thickness is increased, the SB height is lowered owing to Fermi level depinning, resulting in better current injection despite the presence of an interlayer tunnel barrier.[86] As the barrier continues to increase, the interlayer tunneling resistance begins to dominate and counter any improvement in current injection due to the reduction in SB height. Hence, there exists an optimum intermediate interlayer thickness to maximize the current injection. (c) Experimental data showing the specific contact resistivity *versus* Ta_2O_5 interlayer thickness. At low thicknesses, the SB height dominates the resistivity, while at higher thicknesses, the tunneling resistance dominates with an optimum value occurring at approximately 1.5 nm. Reprinted with permission from ref. 87. Copyright 2016 American Chemical Society. (d) Band diagrams of graphene contacts to 2D semiconductors. The Fermi level in the graphene can be adjusted by the applied gate voltage which reduces the SB height and the contact resistance.[92,94,96,120] (e) DFT calculations showing the modified work functions of various metal-interlayer combinations and their alignment with the bandgaps of common TMDCs. Graphene and h-BN interlayers lower the effective work function while NbS_2 and MoO_3 interlayers increase the same for various elemental metals. Reprinted with permission from ref. 92.

monotonically as shown in Fig. 6c. A. Dankert *et al.* demonstrated 2 orders of magnitude increase in ON current, 6 fold increase in field-effect mobility and improved spin injection efficiency in a MoS_2 FET by introducing a TiO_2 tunnel barrier between the ferromagnetic cobalt (Co) contact and the 10 nm thick exfoliated MoS_2.[59] Their findings suggest a reduction in SB height from ~120 meV for Co/MoS_2 contacts to ~27 meV for Co/TiO_2/MoS_2 contacts. Similarly, J. Chen *et al.* also reported an 84% reduction in the SB height for Co contacts to single layer MoS_2 FETs by inserting a 2 nm MgO tunnel barrier.[88] Finally, J. Wang *et al.* showed that 1–2 layers of a CVD grown h-BN interlayer can reduce the SB height from ~158 meV to ~31 meV for Ni contacts to MoS_2.[89] The above reports clearly point towards the successful depinning of the Fermi level using metal–insulator–semiconductor (MIS) contacts for MoS_2, leading to SB heights that are comparable to room temperature thermal broadening of the Fermi function ($2k_BT/q$ ~ 50 meV). However, barrier free Ohmic contacts at low carrier densities have only been achieved, very recently, by X. Cui *et al.* in Co/h-BN/MoS_2 MIS contacts enabling observation of intriguing quantum phenomena.[90] Their XPS measurements showed a reduction in the work function of Co/h-BN contacts to 3.3 eV compared to the 5.0 eV for pure Co. This is consistent with DFT calculations by M. Farmanbar *et al.*, suggesting that the insertion of monolayer h-BN can eliminate the interaction between the metal and MoS_2 and restore the unperturbed electronic structure of MoS_2.[91] In addition, an h-BN layer decreases the metal work function by ~2 eV for large work function metals, particularly for Co and Ni(111) owing to lattice matching with h-BN.[91]

While many recent experimental and theoretical studies have focused on making n-type Ohmic or low-SB contacts to TMDCs, the readers should note that a similar strategy can be used to fabricate low resistance p-type contacts. DFT calculations by M. Farmanbar *et al.* claim that metal/h-BN interlayer contacts can enable p-type transport in TMDCs if the metal work function is sufficiently high, and/or the TMDC ionization potential is sufficiently low.[92] For example Pt/h-BN, and Au/h-BN contacts to $MoTe_2$ result in a negative SB height for hole injection. Alternatively, one can use a graphene interlayer which is qualitatively similar to that of an h-BN monolayer. For example, Y. Liu *et al.* fabricated n-type FETs with Ni/graphene contacts which produced ON currents as high as 830 μA μm^{-1}, contact resistances down to 540 Ω μm, and SB heights as low as 7 meV.[31] The reader should note that, because graphene is a Dirac semi-metal, there is a nonzero density of states above and

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below the equilibrium Fermi level position. This allows the fermi level position to shift up and down with an applied gate voltage and can facilitate either electron or hole conduction depending on the gate bias as shown in Fig. 6d. This effect results in a dynamic reduction of the SB height for 2D transistors with graphene contacts if the device is configured so the graphene contact regions are also modulated by the gate. It has been experimentally demonstrated that graphene electrodes can be used to fabricate both n-type and p-type FETs.[93–96] X. Liao *et al.* used selective hydrogen plasma etching of graphene grain boundaries to fabricate ultra-short channel monolayer MoS_2 transistors with graphene contacts and channel lengths as short as 4 nm.[95] They measured contact resistances as low as 4.8 kΩ μm which is significantly higher than some of the other results discussed in this review. The limited improvement is likely due to the finite gate tunability of the graphene fermi level. H. Chuang *et al.* were able to improve the graphene tunability by reducing the EOT through the use of ionic liquid gating in order to produce high quality n-type and p-type WSe_2 FETs.[96]

M. Farmanbar *et al.* showed that a generic strategy for universally applicable p-type interlayer contacts would necessitate the use of an interlayer material that effectively increases the metal work function such as NbS_2, MoO_3 *etc.* as shown in Fig. 6e.[92] NbS_2 has a similar structure to that of semiconducting MX_2, but is metallic with a high work function close to 6 eV. Monolayer NbS_2 interlayers result in negative SB heights for contacts to all MX_2 materials irrespective of the work function of the metal, *i.e.* Au/NbS_2 and Al/NbS_2 are essentially the same contact. Similarly, MoO_3 interlayer contacts enable p-type transport, as demonstrated in Fig. 5b, owing to its sufficiently high electron affinity. In spite of being an oxide, it allows transport through its conduction band and hence does not present a tunnel barrier to MX_2. Because the interlayer material has such a large impact on the combined metal-interlayer effective work function, alternate interlayer materials can be used to make both n-type and p-type FETs for a given channel material without changing the contact metal. For example, Y. Sata *et al.* fabricated both n-type and p-type WSe_2 FETs with Ti/Au contacts by varying the interlayer material.[97] A multilayer graphene interlayer produced n-type FETs with $\Phi_{SB\text{-}n} \approx 63$ meV while multilayer $NbSe_2$ resulted in p-type FETs with $\Phi_{SB\text{-}p} \approx 40$ meV. Alternatively, a degenerately doped layer of the 2D channel material can be used as an interlayer to fabricate both n-type and p-type FETs for a given material. H.-J. Chuang *et al.* demonstrated high performance WSe_2 devices using substitutionally Nb doped WSe_2 as the interlayer material.[32] They measured contact resistances as low as 300 Ω μm, drive currents as high as 320 μA μm^{-1} and mobilities of up to 200 $cm^2\ V^{-1}\ s^{-1}$. By adjusting the dopant, Nb for p-type and Re for n-type doping, they were able to fabricate both n-type and p-type FETs for WSe_2 and MoS_2 while maintaining low contact resistances and high mobilities.

Hybridization and phase engineering

An alternative improvement method involves the hybridization of the 2D semiconductor underneath the metal contacts. This can be accomplished by using a metal which strongly interacts with the semiconductor through covalent bonding as shown schematically in Fig. 7a. It should be noted that the bonding only occurs on the top layer of the 2D material so any benefits are lessened as the semiconductor thickness increases. J. Kang *et al.* reported molybdenum contacts to monolayer MoS_2 where

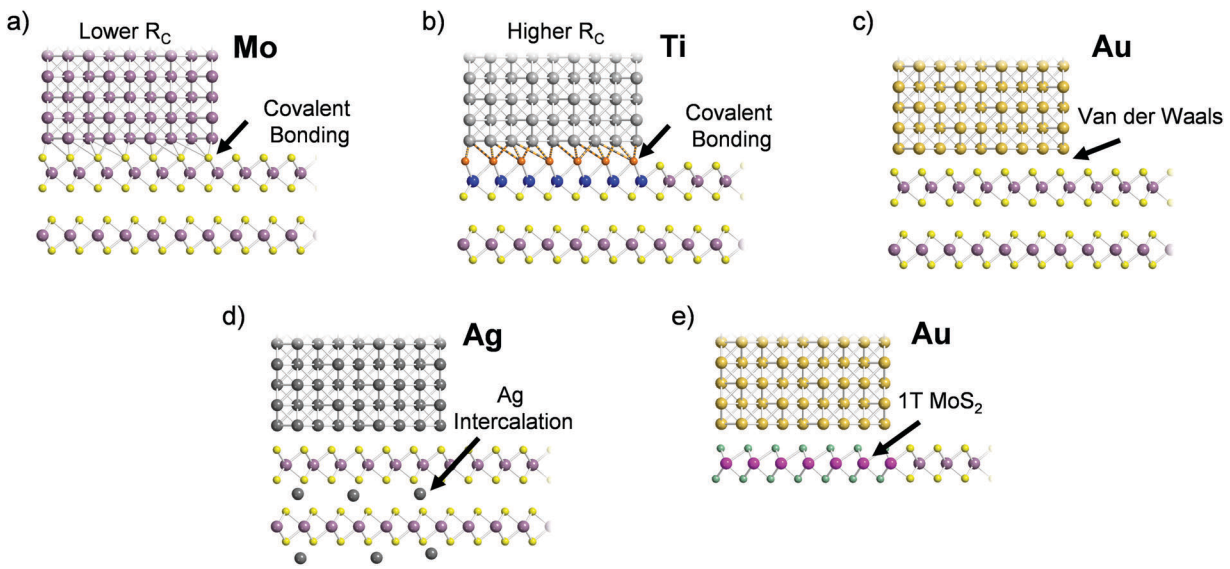

Fig. 7 Contact metal and phase engineered contacts: (a) Mo contacts form covalent bonds with the underlying MoS_2 reducing the SB height.[98] (b) Ti contacts also form covalent bonds with MoS_2, but perturb the underlying layers increasing the contact resistance.[76] (c) Au contacts form van der Waals type interactions with MoS_2 which do not perturb the carrier mobility under the contact.[76] (d) The annealing of Ag contacts at 250 or 300 °C results in the intercalation of Ag between the MoS_2 layers which decreases the contact resistance.[57] (e) Treatment with *n*-butyl lithium in the patterned contact areas before metal deposition converts the monolayer MoS_2 from the semiconducting 2H phase to the metallic 1T phase, greatly reducing the contact resistance.[101,102]

strong covalent bonding between Mo and the MoS_2 significantly reduced the SB height and improved the contact resistance.[98] However, covalent bonding between the semiconductor and the contact metal is not always beneficial as shown schematically in Fig. 7b.[99] This was experimentally demonstrated by C. English *et al.* These authors found that the covalent bonding between MoS_2 and metals like Ti, Ni *etc.* increases the sheet resistivity of MoS_2 owing to carrier mobility degradation underneath the contact which ultimately results in higher contact resistance in spite of a lower SB height.[76] This finding is contrary to theoretical studies which state that a strong interaction with Ti should metallize the interface and the underlying layer, and hence lower the contact resistance.[70,75] Experimentally, the interface interaction has been shown to be strongly affected by the vacuum pressure during deposition. Ti contacts only interact strongly with MoS_2 if they are evaporated under ultra-high vacuum (UHV) conditions of $\sim 10^{-9}$ Torr.[99] If they are evaporated at a higher pressure ($\sim 10^{-6}$ Torr), they oxidize and largely form TiO_2 which perturbs the MoS_2 less and results in lower contact resistance values. However, this is not a general trend for all strongly oxidizing, low work function metals as exemplified by the high performance UHV deposited Sc contacted devices discussed in the previous section.[56] Metals like Au, in contrast, exhibit vdW type interactions with MoS_2 as shown schematically in Fig. 7c, and therefore maintain an unperturbed carrier mobility underneath the contact which aids in achieving lower contact resistance values.[76] Recently, M. Abraham *et al.* reported annealed Ag contacts to few layer MoS_2. They found that annealing at 250 or 300 °C reduced the contact resistance from 800 Ω μm to 200 Ω μm, without any detrimental effect on the FET characteristics. They attributed the reduced contact resistance to diffusion of Ag into the MoS_2 and subsequent doping of the contact area as shown schematically in Fig. 7d.[57] L. Wei *et al.* found Ag contacts to multilayer WSe_2 to have a contact resistance of 6.5 kΩ μm, two orders of magnitude lower than for Ti contacts.[100] Their calculations show that significant Ag-d orbital mixing dopes the WSe_2 and therefore leads to lower contact resistances compared to other metals with less orbital mixing such as Al.

Finally, an elegant approach of transforming the 2D semiconductor underneath the contacts into a metal or metal like state is phase engineering as shown schematically in Fig. 7e. R. Kappera *et al.* demonstrated that immersing monolayer MoS_2 in *n*-butyl lithium can convert ~60–70% of the treated region from the semiconducting 2H phase to the metallic 1T phase.[101,102] The *n*-butyl lithium donates charge to the MoS_2 converting it to the metastable 1T phase which remains even after the removal of the *n*-butyl lithium. The 1T MoS_2 under the contacts has an atomically sharp phase boundary with the 2H channel and eliminates the Schottky barrier under the contacts, drastically improving the contact resistance to values as low as 200 Ω μm.[102] S. Cho *et al.* demonstrated a similar process which used a 26 mW laser to locally induce a phase change under the contact regions in $MoTe_2$ FETs from the 2H semiconducting phase to the distorted 1T′ metallic phase.[103] They found that this process reduced the SB height from ~200 meV to ~10 meV and increased the mobility from ~1 $cm^2\ V^{-1}\ s^{-1}$ to ~50 $cm^2\ V^{-1}\ s^{-1}$.

Edge contacts

Edge contacts to 2D materials show numerous benefits over top contacts. The top basal planes of TMDCs are contacted through unfavorable out-of-plane carrier transport with charge injected through a wide tunnel barrier and across an interface with a low degree of covalency. However, contacts to edge sites are characterized by more favorable in-plane carrier injection with a higher degree of covalency and smaller tunnel barrier widths.[70,104] Y. Matsuda *et al.* studied edge contacted graphene and found that the contact resistance directly relates to the transmission probability, $T(E)$ and hence the cohesive coupling between the metal d orbitals and the graphene p orbitals.[105] With the traditional top contacts to graphene, the cohesive coupling occurs with the carbon pπ orbitals, whereas for the edge contacted graphene, carbon pσ orbitals also contribute, increasing the cohesive coupling and improving the transmission. The effect is compounded for multi-layered 2D materials as edge contacts can form for each layer, efficiently injecting charge deep into the 2D material. Edge contacts are also beneficial for scaling purposes since there is no longer any need for an overlap region between the metal and the semiconductor. However, because close proximity is required, it is difficult, but not impossible, to fabricate edge contacts, especially to thicker 2D layers using conventional deposition techniques. One method relies on the presence of an insulating capping layer which is etched away underneath the contact regions before the metal is deposited as shown in Fig. 8a. The capping layer prevents the deposited metal from coming in direct contact with the top of the channel material, resulting in the formation of edge contacts. L. Wang *et al.* used this method for h-BN encapsulated monolayer graphene and achieved contact resistance values as low as 100 Ω μm and room temperature mobilities near the theoretical phonon scattering limit.[104] Similarly, Y. Chai *et al.* used ALD deposited Al_2O_3 to demonstrate edge contacts to multilayer MoS_2.[106] B. Karpiak *et al.* were also able to use this method to fabricate ferromagnetic 1D edge contacts to h-BN capped graphene.[107] Ferromagnetic 1D edge contacts to graphene are promising for spintronic devices where traditional top ferromagnetic metal/tunnel barrier contacts limit device performance due to defects in the oxide tunnel barrier. 1D edge contacts are advantageous, offering improved spin injection and detection homogeneity as well as reduced interface-induced spin dephasing.

Recently, M. Guimaraes *et al.* developed a bottom up technique where a highly controllable metal–organic CVD (MOCVD) method[108] was used to grow single layer TMDCs (MoS_2 and WS_2) from the edges of lithographically patterned monolayer graphene as shown in Fig. 8b, providing seamless edge contacts with a contact resistance of 30 kΩ μm.[109] This is several orders of magnitude higher than the state-of-the-art contact resistance values which are in the range of 200 Ω μm. The cause of the increased contact resistance is that, while edge contacts provide better carrier injection than top contacts, the

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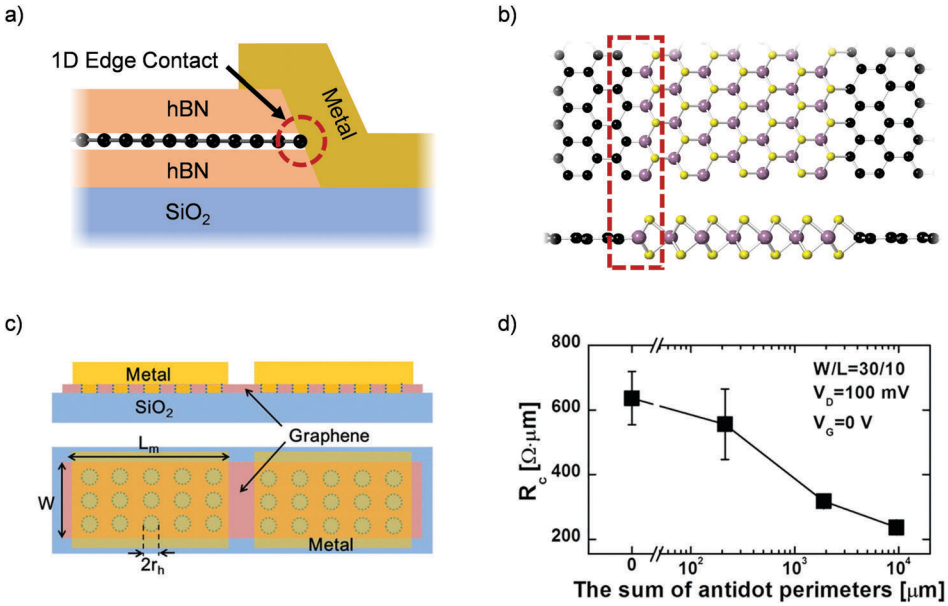

Fig. 8 Edge contacts: (a) edge contact to h-BN encapsulated monolayer graphene fabricated by etching through the edge of the stack before the metal deposition. The top h-BN layer prevents any contact between the metal and the top of the graphene layer. (b) Monolayer MoS_2 grown in etched regions of CVD monolayer graphene to form pure edge contacts.[109] While edge contacts provide better carrier injection and are highly scalable, the miniscule contact area may limit performance. (c) Schematic of etched antidots in graphene FETs underneath the metal contacts. These antidots increase the total effective edge contact length and hence improve the device performance.[112] (d) Increasing the total perimeter of the etched antidots reduces the contact resistance by a factor of three. (c and d) Reprinted with permission from ref. 112, with the permission of AIP Publishing.

carriers are transported though a significantly reduced contact area defined by the channel thickness. W. Leong *et al.* used a different strategy where they created multiple nano-sized pits with zigzag edges in graphene underneath the contact through metal-catalyzed etching in hydrogen in order to facilitate strong chemical bonds with the deposited Ni.[110] They were able to demonstrate a contact resistance as low as 100 Ω μm in single-layer graphene FETs and 11 Ω μm in bilayer graphene FETs. H. Park *et al.*, S. Song *et al.*, and J. Smith *et al.* adopted more engineerable approaches for optimizing the contact resistance for graphene FETs by increasing the effective edge contact length through patterned etching.[111–113] Fig. 8c shows a schematic of antidots etched underneath the contacts of a graphene FET. As the total perimeter of the antidots is increased, the contact resistance improves by a factor of three due to the increased edge contact length as shown in Fig. 8d.[112]

Where is the Schottky barrier?

The conventional Schottky barrier model presented up until this point works relatively well for small SB heights and is useful for understanding the effects of metal work function engineering and gate electrostatics on ambipolar transport.[85] This is the simplest case which assumes that the SB exists where the contact metal meets the semiconducting channel or in the case of phase engineered or hybridized contacts, at the junction between the metallic/metal-like and semiconducting TMDC as shown in Fig. 9a.[101] However, this simple picture fails to address some subtle issues like the impact of contact gating in multilayer TMDCs with relatively large SB heights such as in the case of WSe_2. A more comprehensive "two path" model was, recently, proposed by A. Prakash *et al.*[114] They identified two SB current injection paths as shown in Fig. 9b and c in addition to the thermionic injection path. The total current is given by the sum of these 3 paths, $I_{\text{path-1}} + I_{\text{path-2}} + I_{\text{THERMAL}} = I_{\text{TOTAL}}$. Their experimental data backed by simulation results shown in Fig. 9d suggest that path 1, which represents the traditional SB injection, cannot be the dominant current injection path for the WSe_2 devices, owing to large SB height ($\Phi_{\text{SB-n}} \sim 0.4$ eV) and wider SB width ($\lambda_{\text{SB}} \sim 40$ nm) limiting the transmission probability. Instead, path 2 is the primary current injection source and is also responsible for the contact gating effect. In Fig. 9b, the potential profile under the contact along the thickness of the flake, t_{body}, is shown where the body to source voltage drop (V_{BS}) is given by eqn (7), and γ_{C} is the band movement factor under the contact.

$$V_{\text{BS}} = \frac{V_{\text{GS}}}{\gamma_{\text{C}}}; \quad \gamma_{\text{C}} = \left(1 + \frac{C_{\text{S}}}{C_{\text{ox}}}\right); \quad C_{\text{S}} = \frac{\varepsilon_{\text{body}}}{t_{\text{body}}} \qquad (7)$$

Charge is injected deep into the flake *via* thermally assisted tunneling. As seen in Fig. 9c, the path 2 tunnel barrier width is determined by t_{body}, and not by λ_{SB}. Even though the band movement underneath the contact is slower than the band movement in the channel region, more charge is injected due to the narrower tunneling width. In the case of the WSe_2 device shown in Fig. 6d, I_{TOTAL} is dominated by I_{THERMAL} in the thermionic regime, whereas the ON state current is entirely given by $I_{\text{path-2}}$. BP FETs on the other hand are dominated by path-1 where the traditional SB model works well.[85] The path-2

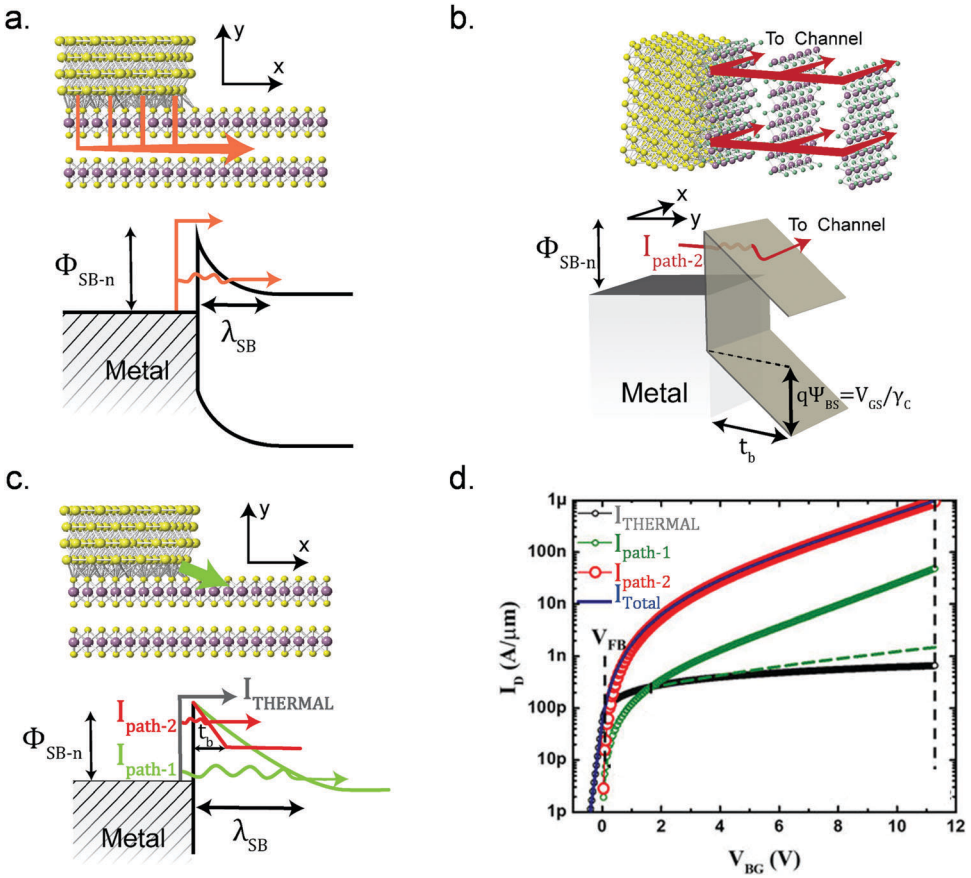

Fig. 9 Current injection in SB-FETs. (a) Simplified SB contact model which does not take into account effects such as contact gating. The electron SB height, $\Phi_{SB\text{-}n}$, is determined by the Fermi level pinning at the metal/2D interface and the tunnel barrier width, λ_{SB}, is given by the geometric screening length. (b) Schematic showing an alternative injection path, $I_{path\text{-}2}$, which injects carriers deep into the 2D material *via* thermally assisted tunneling. The tunnel barrier width equals the semiconductor thickness, t_b ($t_b = t_{body}$), instead of λ_{SB}. The potential drop through the flake depends on the band movement factor underneath the contact, γ_C. (c) The traditional injection path ($I_{path\text{-}1}$), $I_{path\text{-}2}$, and the thermal injection path ($I_{THERMAL}$) are schematically shown. (d) The current contributions, $I_{path\text{-}1} + I_{path\text{-}2} + I_{THERMAL} = I_{TOTAL}$, for a WSe_2 FET. The large $\Phi_{SB\text{-}n}$ and λ_{SB} mean the I_{TOTAL} is dominated by $I_{THERMAL}$ in the thermionic regime and entire $I_{path\text{-}2}$ in the ON state. Reprinted with permission from ref. 114.

charge injection mechanism also explains the strong temperature and gate voltage dependence of the interfacial resistivity. It should be noted that this model assumes uniform carrier injection for path-2 over the entire contact area neglecting any current crowding effects discussed in the next section.

Contact scaling

Contact scaling is one of the most important but least addressed issues in the context of making high quality contacts to 2D materials. Contact scaling challenges primarily arise from the very simple fact that in an aggressively scaled device, both the channel length (L_{CH}) and the contact length (L_C) have to be reduced by a similar factor. While channel length scaling reduces the channel resistance (R_{CH}), contact length scaling increases the contact resistance (R_C). Since the total resistance of the device (R_{TOTAL}), given by eqn (8a), is the sum of these two resistances, device performance is ultimately limited by contact resistance for aggressively scaled devices. In fact, a recent study by C. English *et al.* demonstrated that even for high quality Au contacts deposited under ultra-high vacuum ($\sim 10^{-9}$ Torr) with R_C = 740 Ω μm, the device becomes contact dominated *i.e.* $R_{CH} \approx 2R_C$ when the channel length approaches 90 nm, far from the current "10 nm" node technology.[5,76] Contact scaling and associated effects are schematically depicted in Fig. 10a–c. The quantitative description of contact resistance (R_C) as a function of the contact length is given by eqn (8b) and is derived based on a distributed resistive network model as shown in Fig. 10b, where, ρ_{SH} (in Ω) is the sheet resistance of the semiconducting channel material underneath the contact and ρ_C (in Ω cm^2) is the specific contact resistivity.[30] L_T is referred to as the transfer length, *i.e.* the effective length over which the charge carriers are transferred from the contact metal into the semiconducting channel. This effect is also known as current crowding and can be phenomenologically explained from the fact that carriers prefer to travel inside the more conductive metal contacts and get transferred into the more resistive semiconductor only near the metal–semiconductor contact edges. As evident from eqn (8c) and Fig. 10b, the contact

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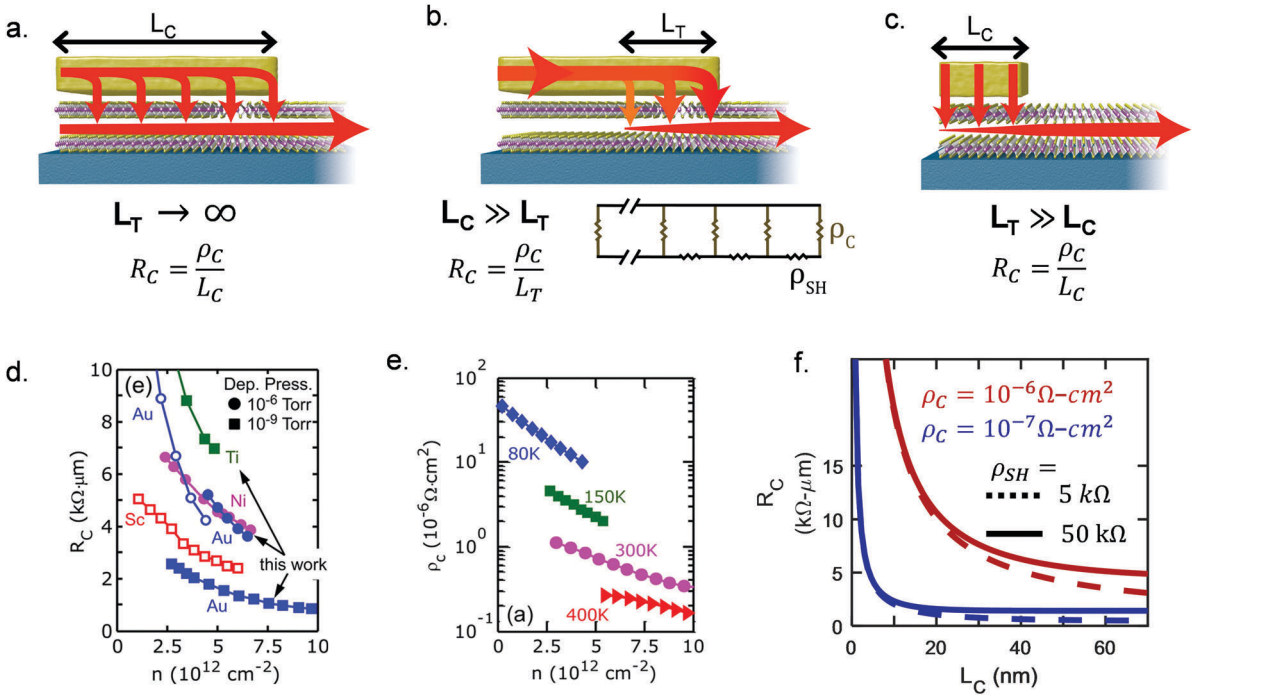

Fig. 10 Length scaling effect on contact resistance. (a) When the transfer length L_T is large, charge is uniformly injected from the metal into the 2D semiconductor and the contact resistance R_C is inversely proportional to the contact length, L_C. (b) When the contact length is larger than the transfer length ($L_C \gg L_T$), the current crowding effect results in the current being injected within a length, L_T, and R_C is independent of L_C. This is the so called current crowding effect described quantitatively using the distributed resistor network model shown schematically.[30] (c) When $L_C \ll L_T$, R_C is again inversely dependent on L_C. (d) Measured R_C *versus* carrier density, n, for various contact metals and deposition pressures in the literature.[56,76,121] (e) Specific contact resistivity, ρ_C, *versus* carrier density, n, and temperature for Au contacts deposited in an ultra-high vacuum (10^{-9} Torr).[76] (d and e) Reprinted with permission from ref. 76. Copyright 2016 American Chemical Society. (f) Effect of the contact length, L_C, on R_C. Decreasing ρ_C from 10^{-6} Ω cm^2 to 10^{-7} Ω cm^2 reduces R_C. Decreasing ρ_{SH} from 50 kΩ to 5 kΩ has relatively little effect on R_C when $L_C \approx L_T$. However, R_C decreases considerably when $L_C \gg L_T$.

resistance is independent of the contact length if $L_C \gg L_T$. However, the contact resistance increases monotonically as the contact length is reduced beyond L_T as shown in Fig. 10c; a fact which is not often addressed by the scientific community. Therefore, true optimization of the contact resistance for aggressively scaled devices requires L_T scaling which can only be accomplished by decreasing ρ_C. Note that increasing ρ_{SH} also scales L_T, but at the expense of increased R_{C0} which defies the ultimate objective of minimizing R_C. Numerous factors determine ρ_C including the height of the SB. Fig. 10d shows the contact resistance for MoS_2 FETs with different metal contacts as a function of the channel sheet carrier density (n_S) at the long contact length limit ($L_C \gg L_T$). Note that sheet carrier density of the semiconductor underneath the contact (n_C) is often wrongly interpreted to be equal to the channel carrier concentration (n_S) in the literature. It is interesting to note that in spite of having similar $\Phi_{SB\text{-}n} \sim 150$ meV and hence, similar ρ_C, Ni contacts are more resistive than Au contacts at the same MoS_2 channel sheet carrier density and therefore the same assumed n_C. This is accounted for by the large difference in the mobility of MoS_2 underneath the contact metal which is $\mu_C = 20$ cm^2 V^{-1} s^{-1} for Au contacts compared to $\mu_C = 0.25$ cm^2 V^{-1} s^{-1} for Ni contacts.[76] These experimental findings indicate that ρ_{SH} can be significantly different from the channel sheet resistance due to a variety of reasons such as hybridization of the 2D material with the contact metal, slowed band movement of the semiconductor under the contact, and a reduced carrier mobility under the contact.[76,114]

$$R_{TOTAL} = R_{CH} + 2R_C \tag{8a}$$

$$R_C = R_{C0}\coth\left(\frac{L_C}{L_T}\right); \quad R_{C0} = \sqrt{\rho_C\rho_{SH}}; \quad L_T = \sqrt{\frac{\rho_C}{\rho_{SH}}};$$

$$\rho_{SH} = \frac{1}{qn_C\mu_C} \tag{8b}$$

$$R_C = \begin{cases} \sqrt{\rho_C\rho_{SH}} & L_C \gg L_T \\ \dfrac{\rho_C}{L_C} & L_C \ll L_T \end{cases} \tag{8c}$$

Fig. 10e shows the specific contact resistivity ρ_C for Au contacts to MoS_2 at various temperatures and carrier concentrations. Fig. 10f shows the effect of the contact length on the contact resistance for various combinations of ρ_C, and ρ_{SH} based on eqn (8b). When the contact length is large, *i.e.* $L_C \rightarrow \infty$, minimizing ρ_{SH} significantly reduced R_C as shown by the dashed and solid lines in Fig. 7f for $\rho_{SH} = 5$ kΩ and 50 kΩ respectively.

For relatively short contact lengths as $L_C \rightarrow 0$, R_C is highly sensitive to ρ_C. For TMDCs, ρ_C is still about an order of magnitude larger than for heavily doped Si contacts where $\rho_C \sim 10^{-8}\ \Omega\ cm^2$.[5] This is a fundamental reason why the contact resistances in TMDC FETs are still far higher than in Si Fin-FET technologies where $R_C < 100\ \Omega\ \mu m$. In Fig. 10f, a device with $\rho_C = 10^{-7}\ \Omega\ cm^2$ (red) *verus* $\rho_C = 10^{-6}\ \Omega\ cm^2$ (blue) results in over an order of magnitude difference in R_C when $L_C < 20$ nm. As $L_C \rightarrow \infty$, R_C for $\rho_C = 10^{-7}\ \Omega\ cm^2$ (red) rapidly decreases with increasing L_C nearing the contact resistance for a device with $\rho_C = 10^{-6}\ \Omega\ cm^2$ (blue). For this reason, the effects of ρ_{SH} and ρ_C need to be kept in mind as certain contact engineering strategies which demonstrate low R_C values may not perform well in highly scaled devices.

Future outlooks

So far the extraordinary amount of research carried out on 2D materials and devices has primarily been driven by scientific inquisitiveness and curiosity. Therefore, it will be premature to comment on their technology readiness level. In fact, the ultimate ''killer'' applications, that will harness one or more exquisite properties of these materials, have yet to be agreed upon. It is also too soon to tell if and when these 2D materials will become a significant segment of the semiconductor industry. From a fundamental standpoint, it is true that these 2D semiconductors are promising alternatives to bulk semiconductors such as Si in FET structures owing to their atomically thin nature that allows aggressive scaling and novel electronic properties conducive to energy efficiency. However, significant progress still must be made in wafer scale manufacturability of TMDCs at temperatures compatible with back end of the line (BEOL) processing, without compromising their high quality and at the same time ensuring low defect densities. Current silicon doping levels are in the parts-per-billion (ppb) range while most of the TMDC materials have defect concentrations measured in percentage. By traditional semiconductor standards, these materials are highly defective, causing a disconnect between experimental findings and theoretical studies. The emerging era of Internet of Things (IoT), which is one of the fastest growing technologies with a projected strength of 50 billion smart devices by the year 2020, may pave a relatively easier way for commercialization of 2D materials in the form of electronic sensors used in all aspects of human life including healthcare, communication, entertainment, home automation, wearables, telemetry, security, infrastructure, and so on and so forth.[133] IoT devices might allow some compromise on material quality as long as the devices are multi-functional, energy efficient, low cost, and mass manufacturable.

Regardless of the ultimate application of the 2D materials in either high performance or low-power consumer or defense related electronic devices, ''Contacts'' will play a pivotal role since these are the inevitable communication links required to harness the fascinating electronic properties of the 2D materials for the three-dimensional (3D) world. Unfortunately, in the absence of any reliable and controllable doping schemes, it is difficult to create low-resistance Ohmic contacts to these materials. The conventional approach of using elemental metals to contact these 2D semiconductors results in Fermi level pinning due to the formation of gap states and dipoles at the metal/2D contact interface and often gives rise to Schottky barrier type contacts. Such Schottky contacts invariably increase the contact resistance and limit overall device performance. Fermi level pinning also restricts ambipolar transport, a requisite for CMOS logic. Therefore, understanding and engineering efficient contacts will have far reaching benefits. In this context, further experimental and theoretical studies are needed in order to fully decipher the impact of Fermi level pinning, Schottky barrier injection, contact gating, current-crowding, and fabrication/processing, *etc.* A comprehensive picture is yet to emerge answering the most fundamental question of how charge is injected from metal contacts into the 2D materials.

In light of these outstanding questions, remarkable progress has been made in reducing the contact resistance of 2D-FETs, as well as fabricating highly scaled devices with sub 10 nm gate lengths.[134] The question now is which of these contact strategies can be transferred to a highly scaled device in a manufacturable way. Issues such as contact length scaling need to be overcome, in particular, improving the interfacial resistivity and the sheet resistance underneath the contacts. Other important factors such as the parasitic capacitance resulting from the structure and geometry need to be considered as well. One major issue not addressed in the literature so far is how to create low resistance contacts for top gated 2D-FETs. In a back gated structure, the global back gate modulates the carrier concentration underneath the contact and hence the lowest contact resistance is achieved in the ON state. However, for top gated FETs, degenerate doping of the 2D material underneath the contacts seems necessary due to the absence of the contact gating. Furthermore, CMOS implementation mandates low resistance NMOS and PMOS transistors, *i.e.* seamless injection of both electrons and holes into their respective bands of the 2D semiconductor from the contacts. Currently, WSe_2 is the most promising material demonstrating CMOS compatibility owing to its ambipolar conduction. However, WSe_2 devices are limited by large contact resistance values and hence the ON state performance cannot match MoS_2 devices. While it is possible to have different TMDCs for NMOS and PMOS, this would add significant complexity and is therefore undesirable.

Conclusions

In conclusion, in this review, we have provided a comprehensive discussion on various aspects related to contacts to 2D materials and devices including the phenomenon of Fermi level pinning and its possible origins and adverse consequences. We have also elucidated the characteristic features of a Schottky barrier FET and possible ways of mitigating its detrimental effects on the device performance. We also presented a review of several contact engineering strategies that have been adopted to improve the contact resistance including superior electrostatics

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through geometric dimension scaling, Fermi level depinning *via* the introduction of thin interlayer materials between the metal and semiconductor, graphene contacts with gate tunable work functions, metallic 1T phase MoS_2 contacts, and edge contacts among others. Finally, we emphasize some of the unresolved or relatively unexplored questions such as where does the SB lie, how is the current injected from the contact into the semiconductor, and how will contact scaling impact the contact performance *etc.* While a decent amount of experimental and theoretical work has been carried out in recent years, more rigorous and focused effort towards improving the contacts can increase the ultimate potential for 2D devices.

Author contributions

The manuscript was written through contributions of all authors. All authors have given approval to the final version of the manuscript.

Conflicts of interest

The authors declare no competing financial interest.

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