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Si Complies with GaN to Overcome Thermal Mismatches for the Heteroepitaxy of Thick GaN on Si

*Atsunori Tanaka, Woojin Choi, Renjie Chen, and Shadi A. Dayeh**

Heteroepitaxial growth of lattice mismatched materials has advanced through the epitaxy of thin coherently strained layers, the strain sharing in virtual and nanoscale substrates, and the growth of thick films with intermediate strain-relaxed buffer layers. However, the thermal mismatch is not completely resolved in highly mismatched systems such as in GaN-on-Si. Here, geometrical effects and surface faceting to dilate thermal stresses at the surface of selectively grown epitaxial GaN layers on Si are exploited. The growth of thick (19 µm), crack-free, and pure GaN layers on Si with the lowest threading dislocation density of 1.1×10^7 cm^{-2} achieved to date in GaN-on-Si is demonstrated. With these advances, the first vertical GaN metal–insulator–semiconductor field-effect transistors on Si substrates with low leakage currents and high on/off ratios paving the way for a cost-effective high power device paradigm on an Si CMOS platform are demonstrated

For nearly five decades,[1] the large mismatch in the thermal expansion coefficients between GaN and Si (55.7%) has limited the thickness of crack-free GaN film growth on Si to less than 5 µm. In planar layers, severe substrate bowing and GaN layer cracking appears at thicknesses exceeding 1 µm.[2] The selective area growth (SAG) emerged as an effective approach to minimize the detrimental wafer bowing effects by confining the area of grown GaN and enabled the successful increase for this thickness limitation to ≈1.5 µm.[3] But thicker layers are critical for electronic and optoelectronic devices where the density of dislocations and effects of Ga/Si inter-diffusion near the grown interface are thickness dependent.[4,5] Additionally, thicker GaN layers improve the current spreading, minimize heating effects, and reduce the efficiency droop in GaN light emitting diodes (LEDs). To the best of our knowledge, the thickest GaN layer achievable on Si was limited to 4.5 µm grown atop a low temperature aluminum nitride (AlN) interlayer sequence with a total thickness of 14.6 µm.[6] The AlN layers block vertical current flow, thus limiting the effective useful GaN layers for certain types of LEDs and power devices that require >10 µm thicknesses.

To enable the growth of thick and crack-free GaN layers on Si, the interfacial stresses at any point of the GaN/Si interface need to be reduced to avoid crack nucleation. Stresses within the layers themselves need also to be directed away from the crack planes. However, prior SAGs have extensively used rectangular growth patterns where the stresses peak at the pattern corners and it is at these corners where the crack in the GaN layers nucleates.[3,7–9] Therefore, we first embarked on reducing the interfacial stresses along the circumference of SAG patterns in 10 µm-thick GaN layers grown on Si. Our thermal stress simulations (see the Supporting Information) showed that upon cooling from the 1050 °C growth temperature to room temperature, the corner stress is significantly reduced when more corners were added to the pattern and is lowest—and evenly distributed—for a circular interface (**Figure 1**a). Our experiments in Figure 1b corroborated with the simulation results. For the 10 µm-thick SAG GaN-on-Si, the triangular and square GaN patterns were severely cracked while those with hexagonal and circular masks were not. We limited our growth time to three hours for which we could grow by SAG 18 µm-thick GaN-on-Si at the center of circular patterns with 350 µm diameter and the GaN thickness was over 35 µm at the disk edges. As discussed below, once the hexagonal facets are completely developed, thick and crack-free GaN layers exceeding 18 µm will be possible.

The facet development during SAG in circular structures is dictated by the differences in growth rates in the $\langle 11\bar{2}0 \rangle$ (fast) and $\langle 1\bar{1}00 \rangle$ (slow) directions leading to the evolution of $\{01\bar{1}1\}$ facets in the slowest growing interface and hexagonal vertices in the $\langle 11\bar{2}0 \rangle$ direction at the facet intercepts. The development of the hexagonal facets also accumulates stresses in the planar Si substrate. With the same growth disk morphology that was obtained during the growth, we repeated the thermal stress simulations of cooling from 1050 to 100 °C (Figure 1c). The simulation results indicated that the stress peaks at the hexagonal vertices (Figure 1a,d) lead to disk rotation by ≈4–5°. Because of the free surface of the GaN disk, the GaN is not cracked but the Si is cracked under this rotation. Optical and scanning electron microscopy (SEM) showed that the cracks in

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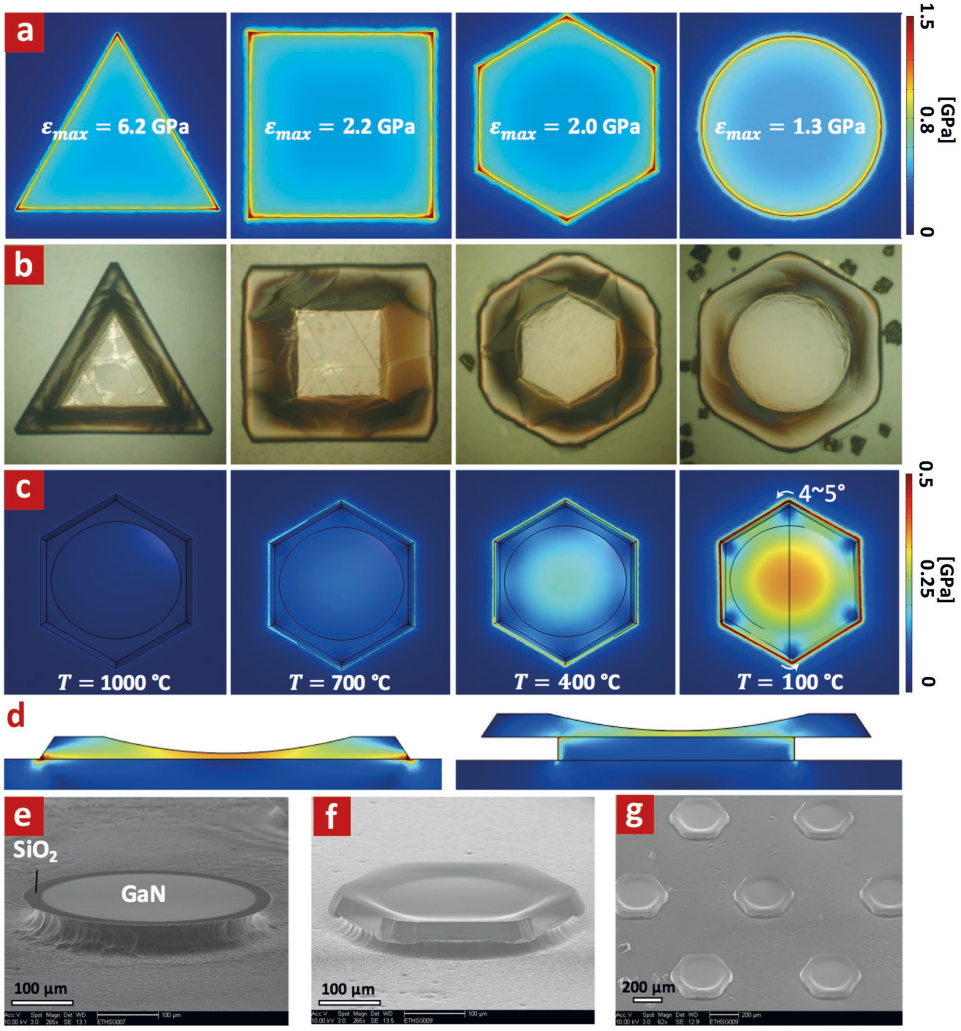

Figure 1. Growth mask influence on the stress in GaN and validation of Si substrate etching in crack-free SAG GaN disk. a) Thermal stress distribution at the GaN/Si interfaces with different mask designs showing the lowest stress maxima for the circular mask. b) Top-view optical microscopy images of the SAG GaN grown to have 10 µm at the center of the structure. The GaN with triangular and squared patterns severely cracked as predicted in (a). c) Evolution of thermal stress during cooling down from 1050 to 100 °C. The solid black lines are the original GaN disk location at the growth temperature. As the GaN disk is stressed during cooling down, it starts to rotate, and results in ≈4–5° rotation with respect to the Si substrate. d) Cross-sectional view of thermal stress simulation of SAG GaN with/without Si base etched. The stress peaks at the interface of hexagonal vertices were eliminated by removing Si under the SAG GaN. e–g) Angled-view SEM images of Si etched SAG GaN disk before (e) and after (f,g) growth.

the Si substrate now nucleate from the interface of the hexagonal vertices (Figure S2a,b, Supporting Information). Further, the cracks propagate tangentially around the GaN disk further suggesting the existence of this rotational stress. The in-plane rotational stress is also deduced from the simulations that accounted for the anisotropic elastic constants in both GaN and Si (Figure S3, Supporting Information). In experiment, the in-plane rotational stresses prevail due to growth inhomogeneities that further break the symmetry in the hexagonal structure. In the cross-section of the GaN/Si interface, we observed that the crack in the Si extended further to the center of the disk and its depth in Si t_{Si} was slightly thicker than the GaN top layer, t_{GaN} ($t_{Si} \propto c_{11-GaN}/c_{11-Si} \cdot t_{GaN} > t_{GaN}$, where c_{11} is an in-plane elastic constant; Figure S4, Supporting Information). Elevated levels of stress in the Si substrate that arise from high areal density GaN structures can lead to the eventual peel off from the Si substrate as shown in Figure S5 (Supporting Information).

In order to eliminate cracking in the Si substrate, we hypothesized that a free Si surface will also dilate the stresses in Si upon cooling down from the GaN growth temperature as supported by thermal stress simulations in Figure 1d. Therefore, we estimated the lateral overgrowth based on our earlier SAG studies[10] and fabricated structures for which the exposed 500 nm-thick GaN seed layer is surrounded by an SiO_2 growth mask on top of an isotropically etched Si structure (Figure 1e and the Experimental Section). This free surface structure (Figure 1e) resulted in crack-free GaN layers and Si substrate because the free surface of the Si substrate can accommodate the stress by rotation. In this context, Si deformation that is caused by thermal stresses in GaN resembles the lead (GaN) and the follower (Si) in a Tango setting. A larger

field of view angled SEM image of the grown array is shown in Figure 1g and top-view optical and SEM images in Figure S2c,d (Supporting Information) showing no tangential cracking in Si. The cross-sectional SEM image through the edge-to-center in the SAG GaN-on-Si disk shown in Figure S6 (Supporting Information) further validates that all cracks in both GaN and Si were exterminated. With this technique, we showed genuine crack-free GaN grown on Si with a thickness of 18 µm for the first time. This is advantageous because the enhanced growth rate by SAG epitaxy allows achieving high-quality GaN layers by metal–organic chemical vapor deposition (MOCVD) in short growth times and is extendable to millimeter-scale growth GaN islands (Figure S7, Supporting Information). Additionally, moving the voltage blocking layers to the vertical direction can increase the device density per unit area compared to the conventionally fabricated lateral devices on the substrate surface. Overall, these capabilities may contribute to a cost effective high power GaN device paradigm on Si.

The mechanism for GaN-on-Si stresses and crack elimination is directly related to the formation of the GaN facets. For a 30 min SAG growth time, a 5 µm-thick undoped GaN layer is grown without facets (**Figure 2**a) whereas a 3 h growth run resulted in 18 µm-thick undoped GaN layers with $\{1\bar{1}01\}$ hexagonal facets (Figure 2b). Although both images in Figure 2a,b show uncracked GaN disks, the yield of uncracked disks for the thinner sample was only 4% (1 out of 25 disks) whereas, counter-intuitively, the yield for the thicker and faceted hexagonal disks was 100% (25 out of 25 disks). To evaluate the difference in residual stress in GaN for the two different growths, we used areal Raman spectroscopy to estimate stress from the Raman peak shift $\Delta\omega$ (Figure S8, Supporting Information). For a σ_{xx} biaxial stress, the Raman shift $\Delta\omega = K\sigma_{xx}$ of GaN E_2(high) peak with respect to stress-free GaN E_2(high) peak, 568 cm^{-1}, was calculated using $K = 4.2$ cm^{-1} GPa^{-1}.[11] Figure 2c–f shows the 2D and 3D mapping of the stress in GaN disks with different thicknesses. These stress measurements identified that

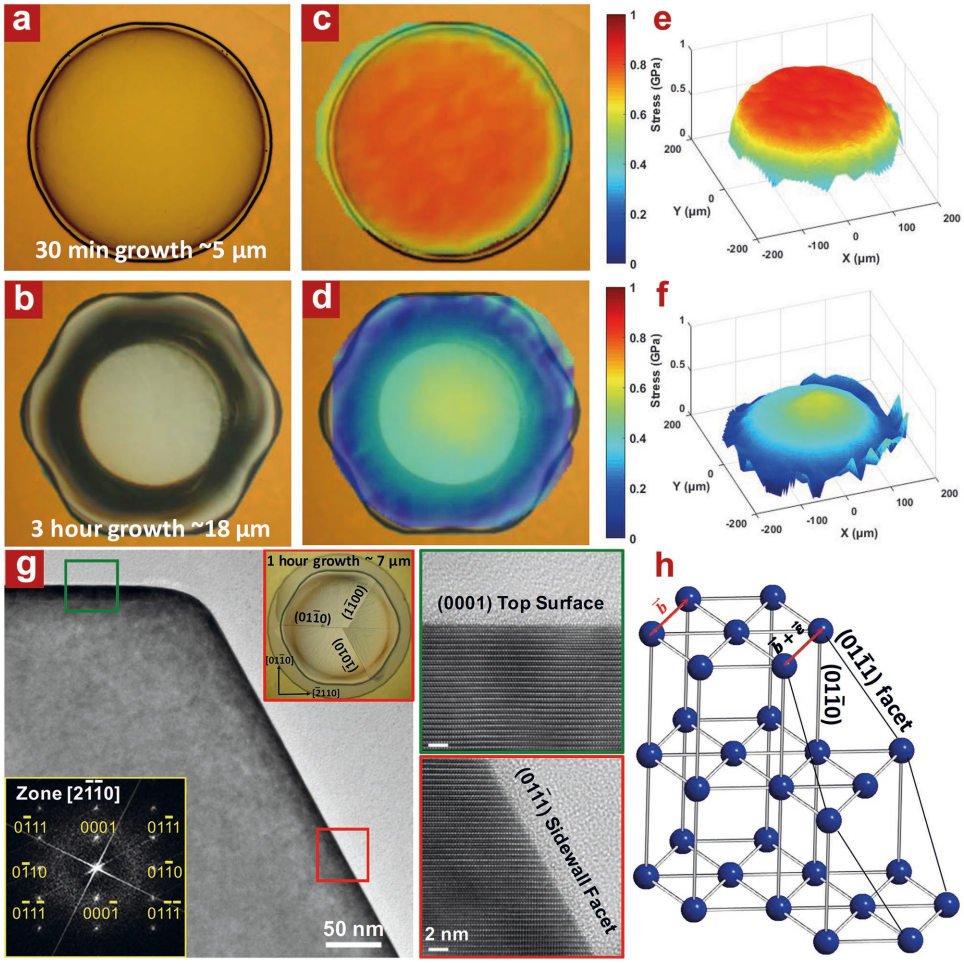

Figure 2. Stress relaxation mechanism in crack-free GaN-on-Si by facet formation. a,b) Top-view microscopy images of 30 min GaN with no facets and 3 h growth GaN with sharp hexagonal facets. c,d) 2D stress mapping measured by Raman spectroscopy on the two different GaN disks overlayed over the images of (a) and (b). e,f) 3D stress maps for disks in (a) and (b). The overall stress values in the thick GaN are almost half of that in the thin GaN due to effective stress reduction near the edge of the GaN disks, indicating stress relaxation by facet formation. g) Cross-sectional TEM and HRTEM images at the edge of hexagonal facets. The sidewall facet and top surface planes are identified by FFT patterns in the bottom-left inset. The top-right inset shows a top-view microscopy image of cracked GaN disk with the crack planes identified. h) Illustration of hexagonal crystal structure (not showing interlattice atoms) showing that the $(01\bar{1}0)$ crack plane and the $(01\bar{1}1)$ growth facet share the Burgers vector $\vec{b}$ and allow the stress in GaN disk to dilate.

the thick GaN encompassed a maximal stress that is nearly half of that for the thin GaN layers. Significantly, the stress reduction is mostly effective near the edge of the thick GaN disks. Therefore, the stress reduction is directly related to the formation of complete facets for the hexagonal disks.

In all our growth studies, we observed the cracks in GaN always occur on the $\{01\bar{1}0\}$ family planes and propagate in $\langle\bar{2}110\rangle$ type directions (inset of Figure 2g and Figure S9, Supporting Information). From the cross-sectional transmission electron microscopy (TEM) images of the faceted GaN disk in Figure 2g and its fast Fourier transform (FFT), we deduced that the thick GaN disk developed $\{01\bar{1}1\}$ facets on the sidewall. Cross-sectional TEM analysis also validated that the cracks occur on the $\{01\bar{1}0\}$ planes (Figure S10 and S11, Supporting Information) when the crystal was oriented in a $[2\bar{1}\bar{1}0]$ beam axis, i.e., along the line of propagation of the crack. The $\langle\bar{2}110\rangle$ crack propagation directions are common dislocation directions (Burgers vector $\vec{b}$) in hexagonal crystals and an avalanche of these dislocations under tensile stress will lead to cracking on the $\{01\bar{1}0\}$ planes. $\vec{b}$ is the line of intersection between the $\{01\bar{1}0\}$ and $\{01\bar{1}1\}$ facet planes as illustrated in Figure 2h. Therefore, if the stresses accumulated on the $\{01\bar{1}0\}$ planes in the $\vec{b}=[\bar{2}110]$ are shared with the surface $\{01\bar{1}1\}$ facets, stress accumulation on the $\{01\bar{1}0\}$ planes inside the GaN disk does not reach a threshold for an avalanche of dislocations in the $\langle\bar{2}110\rangle$ direction. As a result, crack formation on the $\{01\bar{1}0\}$ planes in thick and well-faceted SAG GaN-on-Si disks was eradicated.

This understanding of the cracking mechanism and geometrical effects on stress dilation enabled the growth of 18 µm-thick, crack-free GaN-on-Si with 350 µm diameter in circular SiO_2 mask patterns. For device applications, the threading dislocation density (TDD) is one of the critical parameters that significantly degrade device characteristics and reliability.[12] Dislocations of various types are generated at the GaN/Si interfaces because of lattice and thermal mismatches with dislocation densities approaching 10^9–10^{11} cm^{-2}. It is known that the growth of thick layers in lattice mismatched materials[5,13] can lead to annihilation and reduction of the dislocation densities, but in the context of GaN-on-Si, this approach has never been applied before because thicker GaN layers on Si were not possible before our work. With our thick, crack-free GaN-on-Si, the dislocations at the interface of GaN/Si annihilated as the material grew thicker, and the TDD reduced from $\approx 8.0\times10^7$ cm^{-2} for 10 µm-thick GaN-on-Si to 1.1×10^7 cm^{-2} for 18 µm GaN-on Si as observed with the cross-sectional high-resolution transmission electron microscopy (HRTEM) images in **Figure 3**. This TDD was also validated by dislocation enhanced wet etching and surface imaging as shown in Figure S12 (Supporting Information). To the best of our knowledge, this is about ten times lower than the state-of-the-art TDD of 9.7×10^7 cm^{-2} reported for GaN-on-Si.[14]

To highlight the potential of the thick and crack-free GaN-on-Si with low TDD, we fabricated vertical trench-gate normally off metal–insulator–semiconductor field-effect transistors (MISFETs) employing 19 µm-thick drift layers. **Figure 4**a shows a schematic cross-sectional view of the MISFET structure and Figure 4b shows a cross-sectional SEM image of the fabricated device. The vertical MISFET consisted of a 450 nm-thick intermediate p^+-GaN current blocking layer, and a 200 nm-thick

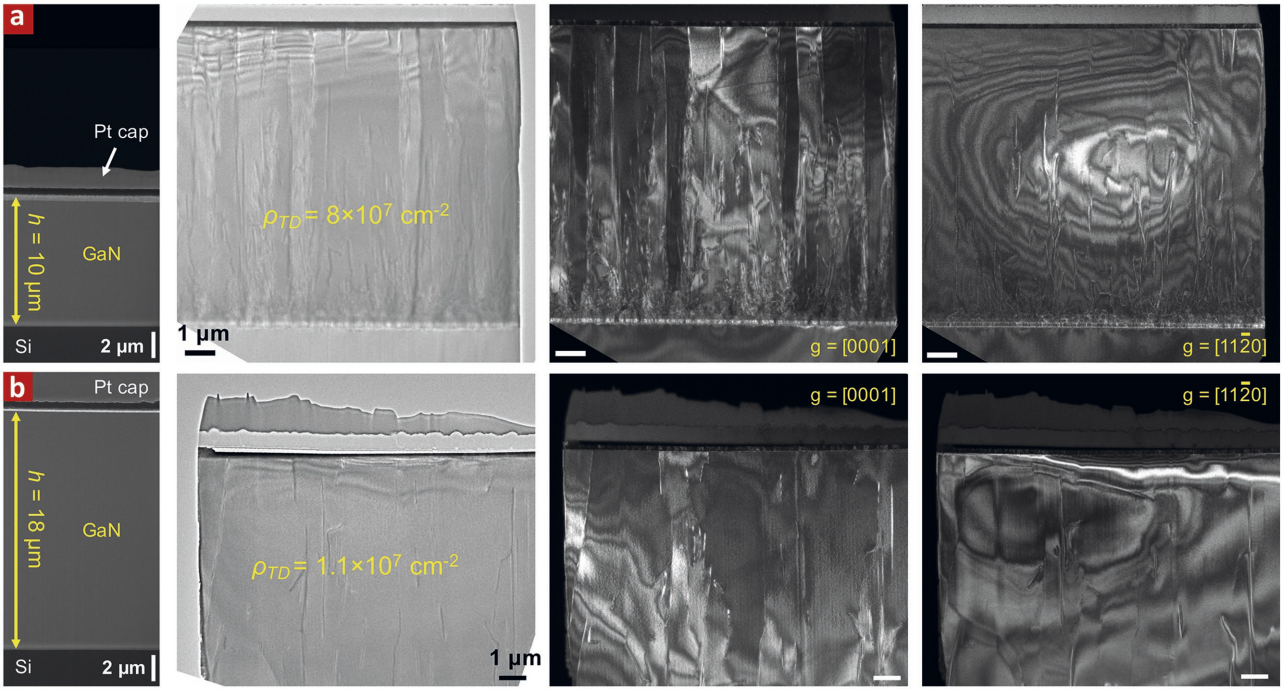

Figure 3. Threading dislocation density reduction in thick GaN disk. a,b) L-R cross-sectional images of GaN-on-Si by SEM, bright field TEM, dark field TEM at two-beam condition with $\vec{g}$ = [0001], and dark field TEM with $\vec{g}$ = [11$\bar{2}$0] for 10 µm-thick (a) and 18 µm-thick (b) GaN layers. The high-density dislocations at the interface with Si in both samples are reduced as the thickness of the GaN layer increased, reaching 1.1×10^7 cm^{-2} for 18 µm-thick GaN layer.

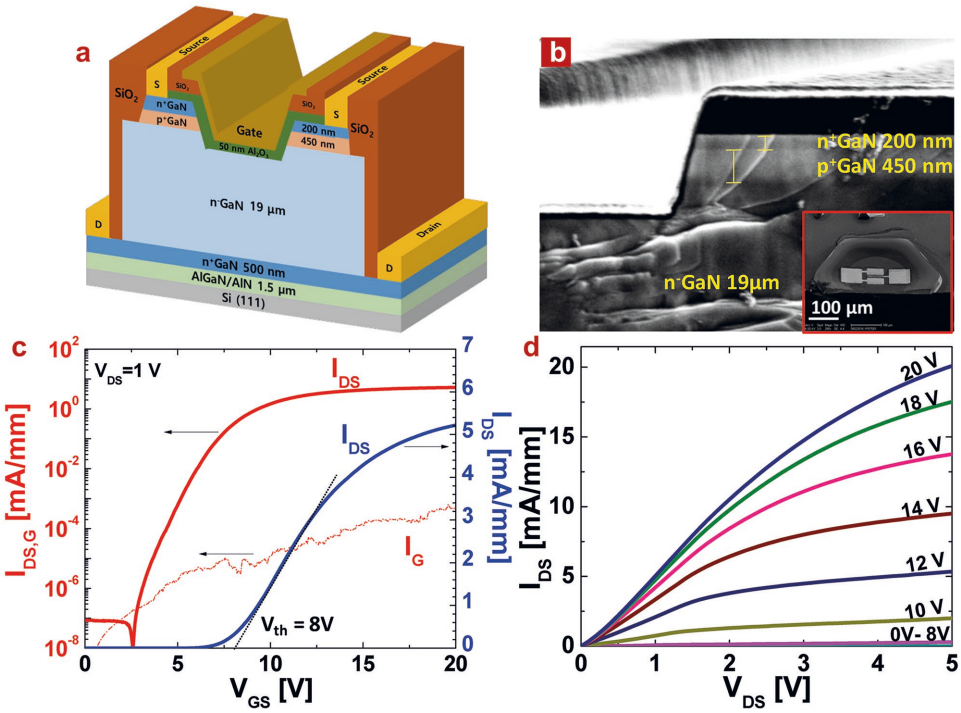

Figure 4. First demonstration of normally off trench-gate GaN vertical MISFET on Si. a) Schematic structure of GaN-on-Si vertical MISFET on 19 µm SAG GaN layer. b) Cross-sectional SEM image of the trench-gate region. Clear p-GaN and n-GaN contrast were observed and thicknesses were determined. The inset SEM image shows angled view device image. c) Linear (blue) and log (red) scale transfer *I–V* characteristics (I_{DS}–V_{GS}) and gate leakage (I_G–V_{GS}) at V_{DS} = 1 V. d) Output *I–V* characteristics (I_{DS}–V_{DS}) at different gate voltages in steps of 2 V.

n^+-GaN top current source layer, as labeled in Figure 4b. The gate recess utilized a sequential dry and wet etching in order to result in smooth and ≈80° slanted sidewalls and round corners at the bottom of the trench as shown in Figure 4b. The device transfer curves shown in linear and semi-log plots are shown in Figure 4c and exhibit a device threshold voltage of ≈8 V and an I_{on}/I_{off} ratio of 10^7 approaching that of recently developed GaN-on-GaN trench-gate MISFETs.[15–21] The device output curves are shown in Figure 4d exhibiting good saturation characteristics and R_{on} value of 31.5 mΩ cm^2 with a gate width of 100 µm (50 µm × 2; see the Supporting Information). The modest hysteresis observed in the transfer curves (Figure S13, Supporting Information) and the relatively high R_{on} observed for these first vertical GaN-on-Si trench MOSFETs can be further optimized with gate surface treatments[22] and regrowth,[20,21] and with engineering the doping profile in the drift layers.[23] Additional work is also required for device edge termination in order to achieve high breakdown voltages in these devices. Nonetheless, we demonstrate here that very low leakage currents and the successful formation of vertical *p–n* junctions are indeed feasible and led to the demonstration of the first vertical GaN-on-Si trench-gate MISFETs.

We demonstrated a new regime of epitaxy in thermal mismatched materials where the thick and crack-free GaN-on-Si is possible. With a systematic approach to understand the cracking behavior and lateral overgrowth to form faceted hexagonal disks on exposed underlying Si surfaces, we were able to grow over 18 µm-thick GaN on Si and lower the TDD density to 10^7 cm^{-2}. These results allowed us to demonstrate functional vertical trench-gate GaN MISFETs on Si and pave the way for integrated vertical GaN power and optoelectronic devices on an Si CMOS platform.

Experimental Section

For the growth of SAG GaN-on-Si, a 3 × 2″ Thomas Swan/Axitron close-coupled showerhead MOCVD system was utilized with trimethylgallium, bis(cyclopentadienyl)magnesium (Cp_2Mg), silane gas (SiH_4), ammonia gas (NH_3) as precursors and H_2 as a carrier gas. On top of a 500 nm GaN layer on AlGaN/AlN transition layers on Si, the SiO_2, SiN_x SAG mask layers were deposited by plasma enhanced chemical vapor deposition (PECVD). Photolithography then followed in order to pattern 350 µm diameter circular masks with dot-to-dot spacing of 450 µm. The masks were first etched in the dot region by reactive ion etching (RIE) (CHF_3, Ar, and O_2) and were then etched with a diluted buffered oxide etch. The exposed GaN surface was treated with concentrated hydrochloric acid (HCl) solution (36–38%) at 60 °C for 3 min in order to remove native gallium oxides (Ga_xO_y).[24] The SAG was carried out on these wafers at a temperature of 1050 °C, which was calibrated at the susceptor surface with a pyrometer, and at a chamber pressure of 100 mbar. For studying cracking in SAG GaN, a V/III ratio of 2250 was employed, which corresponded to a planar growth rate of 1 µm h^{-1} on 2″ c-Al_2O_3 wafer and the growth time was changed to tailor the GaN disk structures from 30 min to 3 h. The substrate engineering SAG template was prepared by controlled anisotropic dry etching of GaN and Si, followed by XeF_2 isotropic dry etching to make a floating GaN template. The vertical MISFET structure was grown on top of 3 h SAG undoped GaN with p^+GaN growth performed at 930 °C and n^+GaN at 1050 °C followed by p^+GaN activation in MOCVD chamber at 750 °C for 20 min under N_2 flow. The morphologies of the grown structures were characterized by SEM and high-resolution transmission electron

microscopy (HRTEM). The HRTEM characterization was performed in an FEI Tecnai F30 microscope at 300 kV to identify the crack planes, growth facets, and threading dislocation densities. The locations for the cross-sectional TEM images and the TEM images are shown in Figure S10 (Supporting Information).

To prepare the electron-beam transparent lamellae for cross-sectional TEM, the focused ion beam (FIB) equipped within SEM (FEI Nova 600) was utilized, followed by in situ lift-out of the sample lamellae to a Cu TEM grid. Prior to FIB milling, 400 nm SiO_2 and 50 nm Pt were deposited atop the sample to improve the surface contrast and to prevent damage of interested area under ion beams. These FIB lamellae were roughly milled under a 30 keV Ga beam and were finally finely milled at a reduced voltage (5 keV), until the thicknesses reached 60–80 nm.

For vertical trench-gate GaN MISFETs, after the SAG growth of $n^-/p^+/n^+$GaN (19/0.45/0.2 µm) epitaxial layers, the SAG mask layer (SiO_2 and SiN_x) was completely removed by 10% diluted hydrofluoric acid solution. A 600 nm SiO_2 isolation layer was redeposited by PECVD and then a mesa isolation etching was performed with the PECVD-SiO_2 layer as a hard mask for a BCl_3/Cl_2-based RIE low damage etching with a radio-frequency (RF) power of 50 W. After removing the SiO_2 hard mask, another SiO_2 layer was deposited as a gate recess etching hard mask as well as a passivation layer for the devices. A 600 nm SiO_2 layer was etched by RIE with a CHF_3/Ar gas mixture to obtain a vertical etching profile of the gate trench and then the gate recess of 1.15 µm with RIE using the mesa isolation conditions was etched. The etched GaN surface was cleaned by 5% tetramethylammonium hydroxide at 80 °C for 10 min and 29% NH_4OH solution for 10 min with sonication at room temperature, and the sample was immediately loaded to a Beneq TFS200 atomic layer deposition (ALD) system. The ALD process was initiated by 20 cycles of trimethyl aluminum (TMAl) prepulses and followed by a 50 nm-thick Al_2O_3 layer deposition as a gate insulator with a chuck temperature of 200 °C. No postdeposition annealing for the gate insulator was performed. A dry etching by RIE was performed for contact window opening, followed by an electron beam evaporation of a 30 nm/70 nm Ti/Al metal stack as Ohmic contacts on top of the n^+GaN layer. Finally, a 60 nm/120 nm Ti/Au was sputtered and dry etched by RIE for the gate metal and pads, in order to achieve a conformal profile at the gate trench sidewall.

Supporting Information

Supporting Information is available from the Wiley Online Library or from the author.

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Conflict of Interest

The authors declare no conflict of interest.

Keywords

GaN on Si, heteroepitaxy, MISFETs, MOCVD, selective area growth

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Supporting Information

Si Complies with GaN to Overcome Thermal Mismatches for the Heteroepitaxy of Thick and Crack-Free GaN on Si

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I. Selective Area Growth of GaN on Si

The focus of this work is to enable the growth of thick GaN layers on Si. Therefore, we acquired Si wafers with 500 nm-thick GaN layers grown on AlGaN/AlN/Si(111) substrate from Powdec (Tochigi, Japan). The SAG mask fabrication started with solvent cleaning by Acetone and Iso-propanol sonication. PECVD SiO_2 or SiNx were deposited and pattern by photolithography and dry/wet etching of dielectric layers then followed. The growth selectivity and mask removal significantly depend on the SAG mask material as shown in Figure S1d-f. After growth, SiNx mask was hardly removed while SiO_2 and SiO_2/SiNx were easy to be removed. For the vertical MISFET, we employed a SiO_2/SiNx SAG dielectric mask.

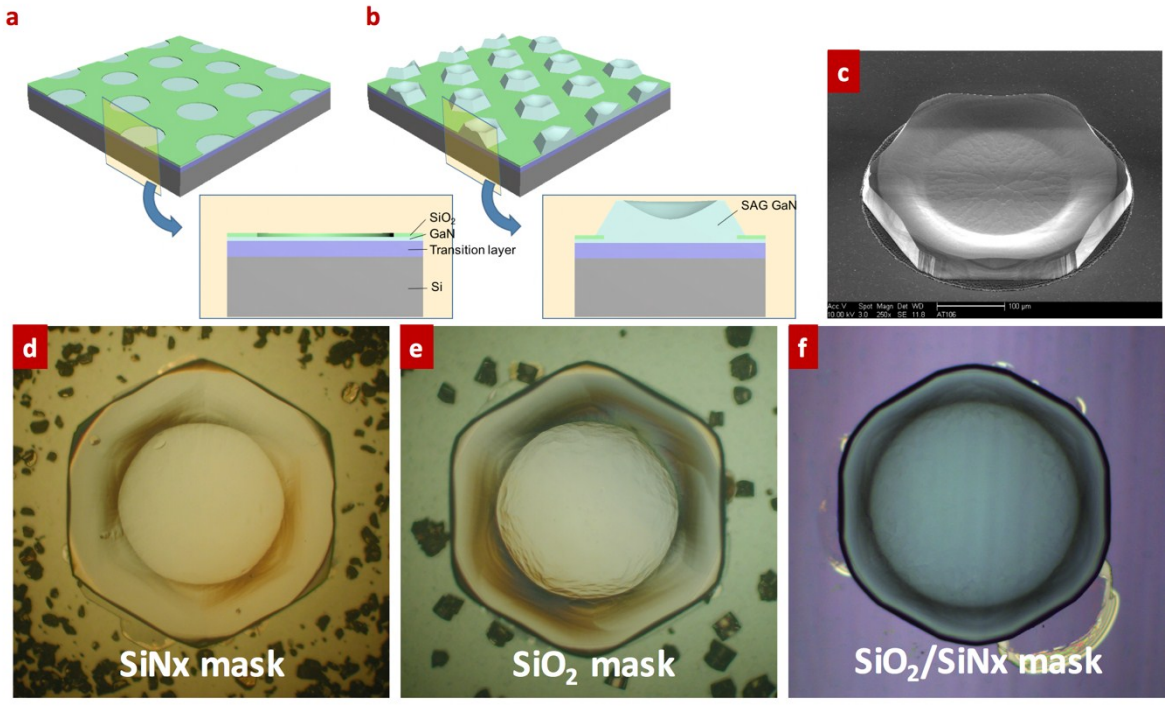

Figure S1. Selective area growth and selectivity. a,b. Schematic illustrations of the SAG GaN-on-Si before and after growth. The grown GaN forms hexagonal facets once the GaN starts to overgrow on the circular SAG mask pattern. **c.** Angled view SEM image of 10 µm thick GaN at the center of the disk and 20 µm at the edge. **d-f.** Top view microscope images of SAG GaN with different mask materials and sequences. SiO_2/SiNx mask shows the best selectivity and mask removal was the most feasible.

II. Thermal stress simulation by Comsol

The thermal stress simulations in this study were performed using Comsol Multiphysics. For the simulations presented in Figure 1, we assumed that the top GaN was fully relaxed at the growth temperature and stressed only by thermal expansion difference from 1mm thick Si substrate. For fair comparison, the interface areas of the different structures were set to be the same as a 350 μm diameter circle. The thermal stresses were calculated by structural mechanics module combined with heat transfer interface to couple the temperature field to structural expansion. The built-in material parameters in Comsol were used for all simulations in the manuscript, except for Figure S3 as described below.

III. Tangential cracking in Si substrate.

Figure S2a and S2b show severely cracked Si substrate. Different from cracking in GaN which always followed specific crystal directions, the crack in Si nucleated below the vertices of the GaN dot and propagated in a tangential fashion due to tangential strain/stress accumulation under the GaN disk that is caused by a rotation due to shear stresses at each of the GaN hexagonal vertices. This tangential cracking agreed with the inferred results from the Comsol simulations which indicated rotational principal stress directions at the interface. Etching of the Si substrate and creating GaN/Si islands eliminated the cracking in Si by dilation of stress with free Si surface. The thicknesses of each GaN layer were 15 μm at the center of GaN disks (Figure S2c and S2d).

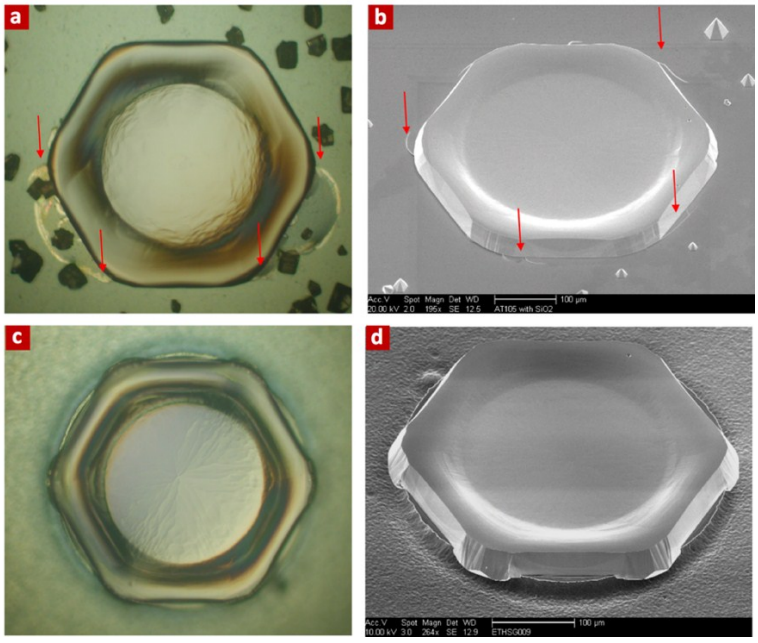

Figure S2. Elimination of tangential cracking in Si. a,b. Optical/SEM images of thick SAG GaN on Si with no Si etch. Cracking can be clearly observed in the base Si in a tangential

fashion. **c,d.** Optical/SEM images of Si-etched thick SAG GaN on Si with no cracking in either GaN or Si.

To clearify the rotational stress in the xy plane, we further simulated the rotational stress component, ∂_{xy}, induced by the thermal mismatch stress. In all simulations, we used the same volume as that of a GaN island which is 30 μm thick and 350 μm in diameter. Figure S3 a-h show tetrahedral mesh patterns for eash simulated structure. We used anisotropic linear elastic materials for both GaN and Si. The elasticity matrix of Si was defined as follows[1]:

$$\boldsymbol{D} = \begin{pmatrix} 1.66 & 0.64 & 0.64 & 0 & 0 & 0 \\ 0.64 & 1.66 & 0.64 & 0 & 0 & 0 \\ 0.64 & 0.64 & 1.66 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0.80 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0.80 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0.80 \end{pmatrix} \times 10^{11}\ \text{Pa}.$$

For wurzite GaN[2] , we used:

$$\boldsymbol{D} = \begin{pmatrix} 3.90 & 1.45 & 1.06 & 0 & 0 & 0 \\ 1.45 & 3.90 & 1.06 & 0 & 0 & 0 \\ 1.06 & 1.06 & 3.98 & 0 & 0 & 0 \\ 0 & 0 & 0 & 1.05 & 0 & 0 \\ 0 & 0 & 0 & 0 & 1.05 & 0 \\ 0 & 0 & 0 & 0 & 0 & 1.23 \end{pmatrix} \times 10^{11}\ \text{Pa}.$$

Figure S3 i-l show mapping of stress tensor, ∂_{xy}, at the interface of GaN/Si. The non-uniform shear stress components indicated the rotational stresses in GaN and Si exist at their interface.

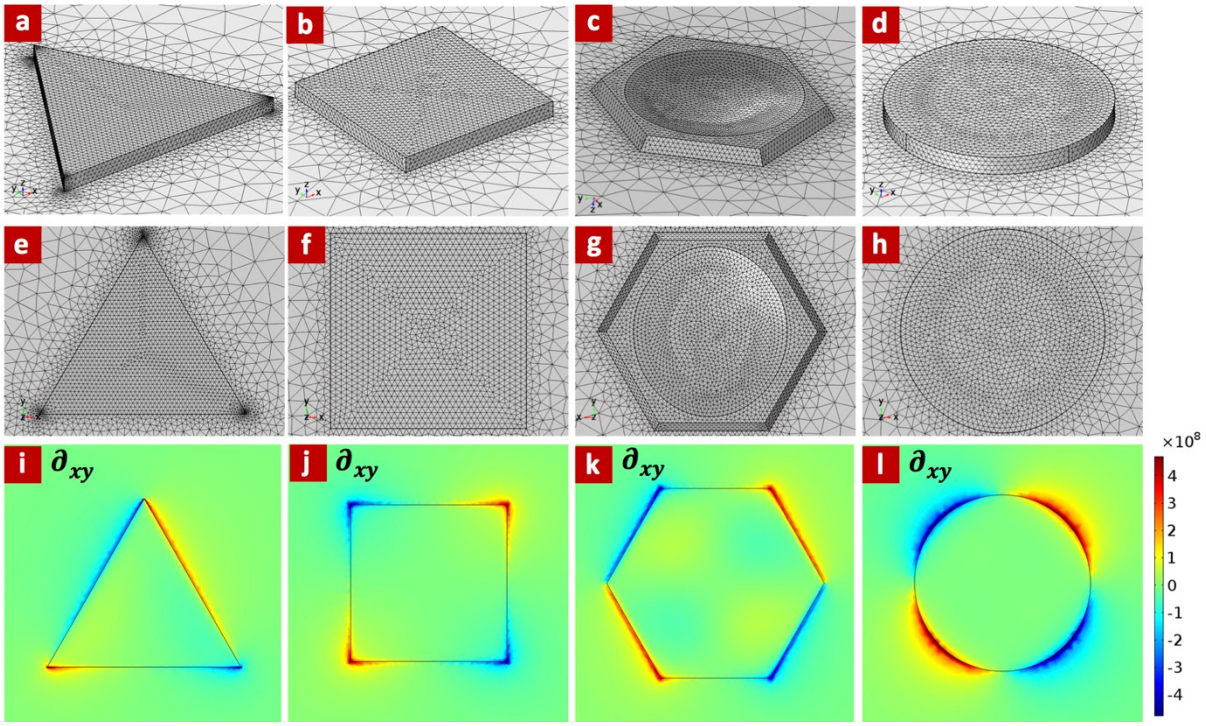

Figure S3. Mapping of rotational stress components, ∂_{xy} . Top view (**a-d**) and anlged view (**e-h**) of mesh pattern for different geometries used in all simulations. **i-l.** Mapping of stress tensors ∂_{xy} at the interface of

GaN/Si with anisotropic elastic matricies. The non-uniform stress distribution along the side of the GaN hexagonal disk together with existing non-uniformites in the grown GaN island lead to rotational stresses in the xy plane at the interface.

The cracking in Si propagates as deep as GaN thickness as shown in Figure S4. The cracking became more severe when GaN disk density increases (Figure S5) leading to eventual peel-off from the substrate and preventing further efforts for device fabrication. In order to eliminate the stress in Si, equal amount of Si under the SAG GaN needs to be removed. Therefore, we etched ~30 µm Si under GaN disk to eliminate cracking in both GaN and Si (Figure 1e-g).

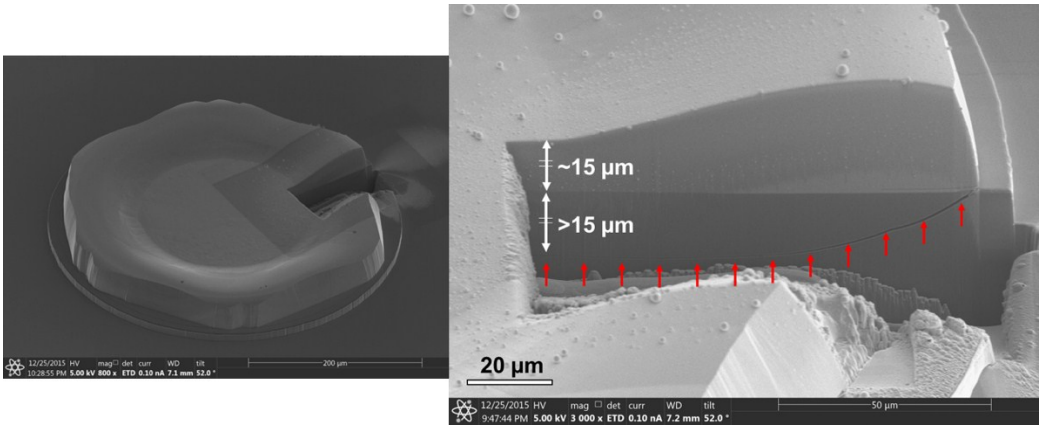

Figure S4. Depth of cracking in Si. Angled view SEM images of FIB cut GaN disk without isotropic etch. The cracking in Si nucleated at the corner of SAG GaN disk and propagated as deep as GaN total thickness. This highlights the need for etching Si base as deep as GaN thickness to relax the rotational stress.

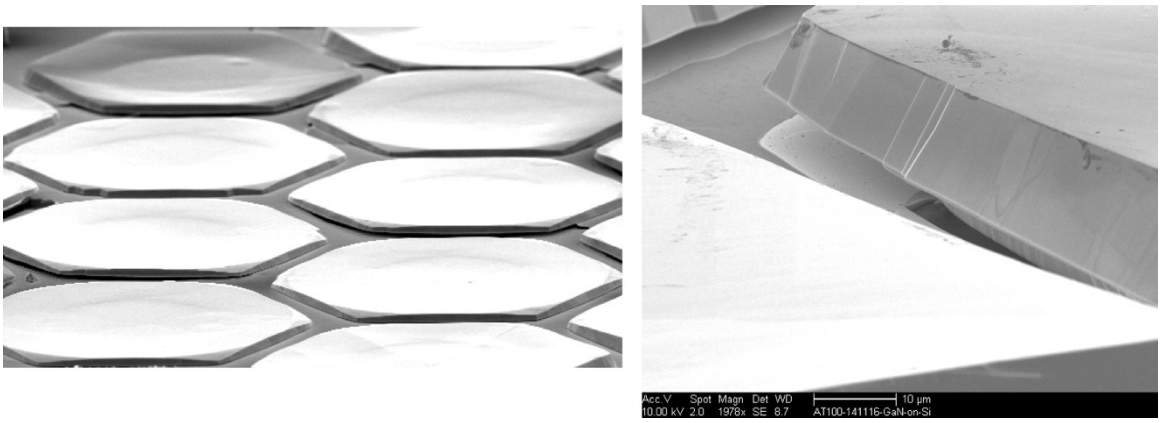

Figure S5. Peeling issue in dense SAG GaN on Si array. Angled view SEM images of highly packed SAG GaN disk arrays (dot-to-dot spacing 20 µm). The high packing desnity led to severe cracking and eventual peel off for the GaN disk from substrate.

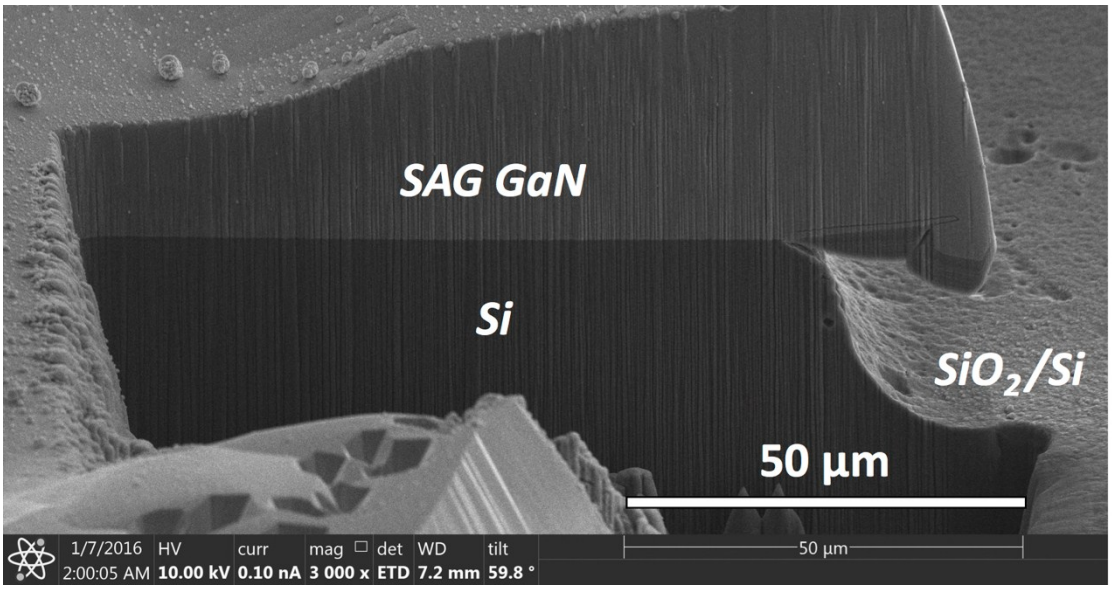

Figure S6. Substrate engineering for crack elimination in Si. Angled view SEM image of FIB cut GaN disk with proper base Si etching. The etching depth was nearly equivalent to the GaN thickness to accommodate all stress at the Si surface. There is no cracking found in GaN and Si.

IV. SAG GaN on Si with millimeter scale mask.

We have also performed large scale SAG GaN growth on Si. By using the circular mask, we were able to grow ~5µm thick crack free GaN on Si. The growth was performed under the same condition as the 350 µm dot reported in this paper with a growth time of 3 hours. The geometrical effects embodied in a limited Ga diffusion length (*Sci. Rep.* **2015**, *5*, 17314), led to a 4X reduced growth rate. It is feasible to grow thicker layers by increasing the time further.

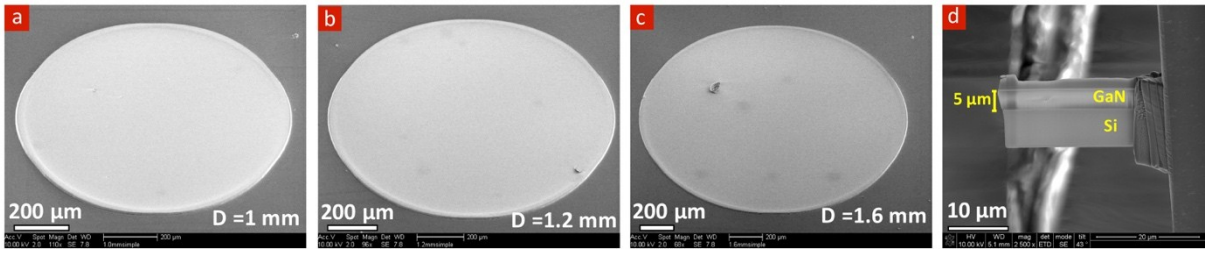

Figure S7. Millimeter scale SAG GaN growth on Si. a,b,c. Angled view SEM images of 1mm, 1.2mm, and 1.6mm diameter GaN disks showing no cracking in GaN-on-Si post 3

hours of GaN growth. **d.** Cross-sectionl SEM images from 1.4mm diameter GaN on Si showing a thickness of 5 μm.

V. Stress measurement on different GaN disk location

Figure S8a and S8b show the as-measured Raman peak (GaN E_2^H) as a function of X, distance from center of the disk. For the thin GaN disk, the GaN E_2^H is significantly lower than the unstressed reference sample GaN E_2^H peak. For all X, the Raman shift frequency remained relatively unchanged. In contrast, the peak shift with X for the thick GaN from the unstressed GaN E_2^H is largest near the center, and decreases toward that of the unstressed state near the disk edges (facets). This implies that the evolution of the hexagonal facets significantly reduced the stress in the GaN disk.

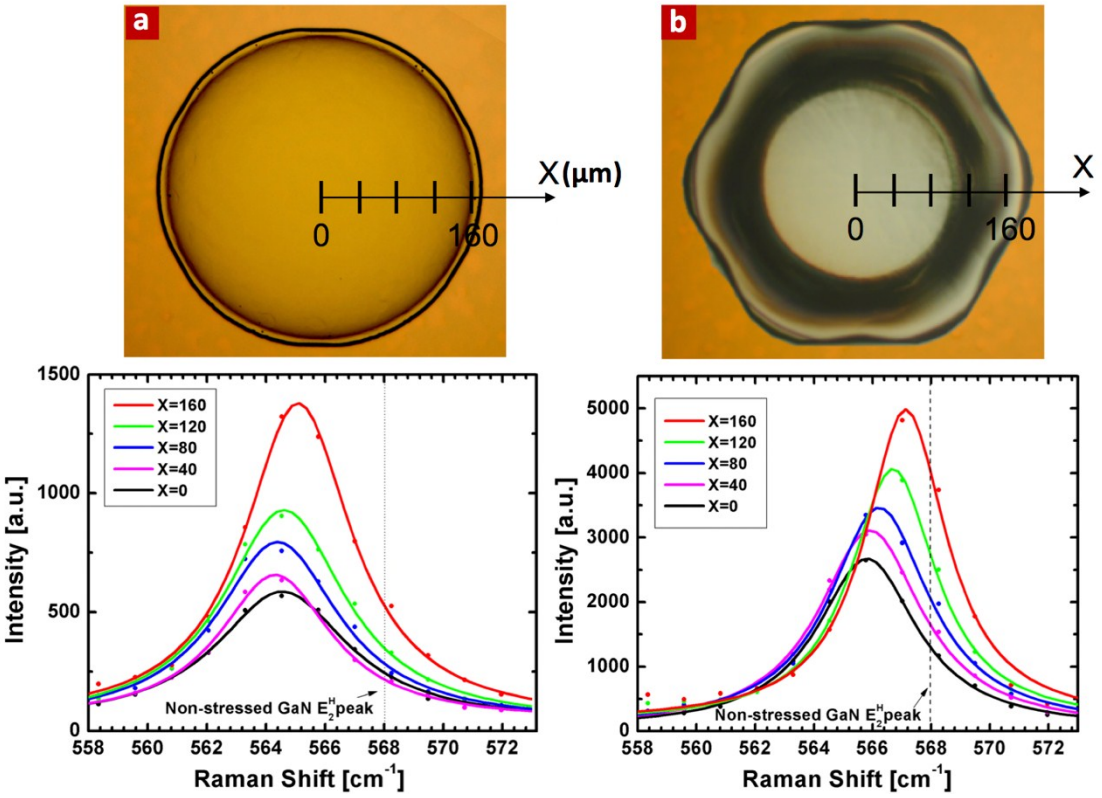

Figure S8. Stress relaxation due to hexagonal facets. Top view microscope images and Raman Shift of **a.** thin GaN disk and **b.** thick GaN disk as a function of X, distance from the disk center. The dashed line indicates the reference peak for non-stressed GaN E_2^H(568 cm^{-1}).

VI. Determination of cracking plane by TEM

From Figure S9, major cracks were observed on the planes of $\{01\bar{1}0\}$ and $\{0001\}$, which agrees with well-known hexagonal crystal slip planes under tensile stress. To determine the crack planes with TEM, we prepared thin TEM lamellas using focused-ion beam (FIB) and in-situ lift-out procedure illustrated in Figure S10. The TEM lamellas were oriented perpendicular to the facets (panel a, Figure S10) to determine the exact facet structure, and perpendicular to the crack (panel b, Figure S10) to determine the crack planes. Figure S11 shows the major crack plane is the $\{01\bar{1}0\}$ plane but the cracks also appear to glide on intermediate $\{01\bar{1}4\}$ planes. The crack propagation in the GaN dot is along the zone axis, following $< 2\bar{1}\bar{1}0>$ type of directions.

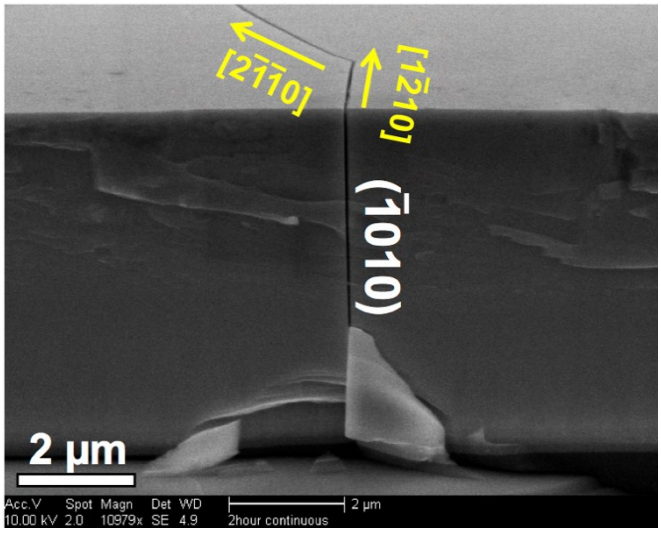

Figure S9. Major crack plane determination by SEM. Angled view SEM image of diced GaN disk in $< \bar{1}010 >$ direction. The crack propagates straight down to the substrate and ~60° intersections, indicating the crack plane is in $\{\bar{1}010\}$ and propagate in the $< 2\bar{1}\bar{1}0>$ directions.

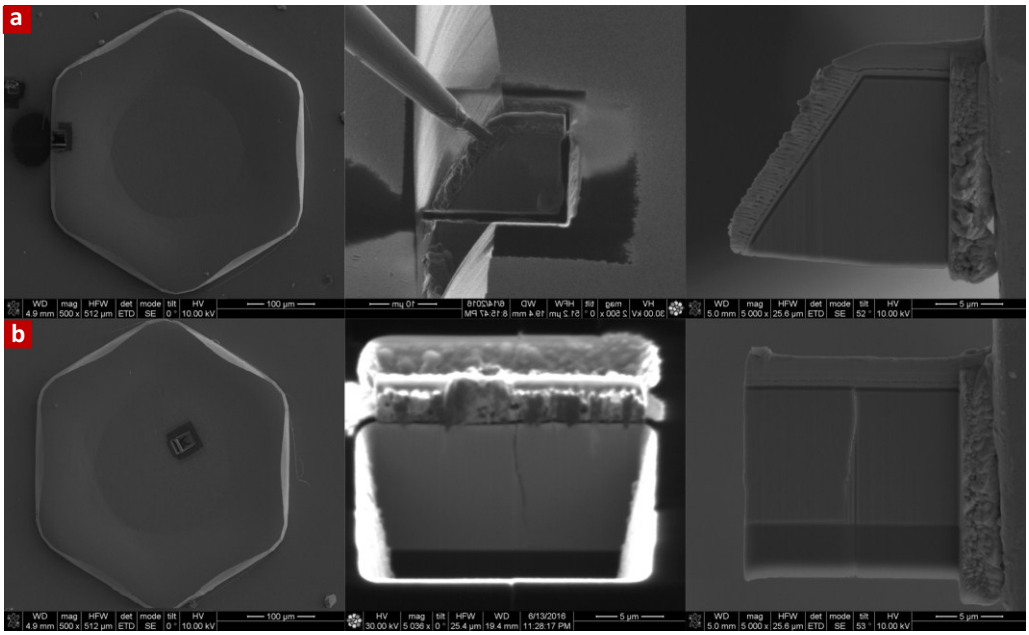

Figure S10. TEM sample preparation. SEM images of FIB cut and lifting of TEM slab by omniprobe. FIB cuts were perpendicular to the hexagonal facets $\{01\bar{1}1\}$ in (**a**) and to the major crack $\{01\bar{1}0\}$ planes in (**b**) to reveal the relationship between crack directions and facets.

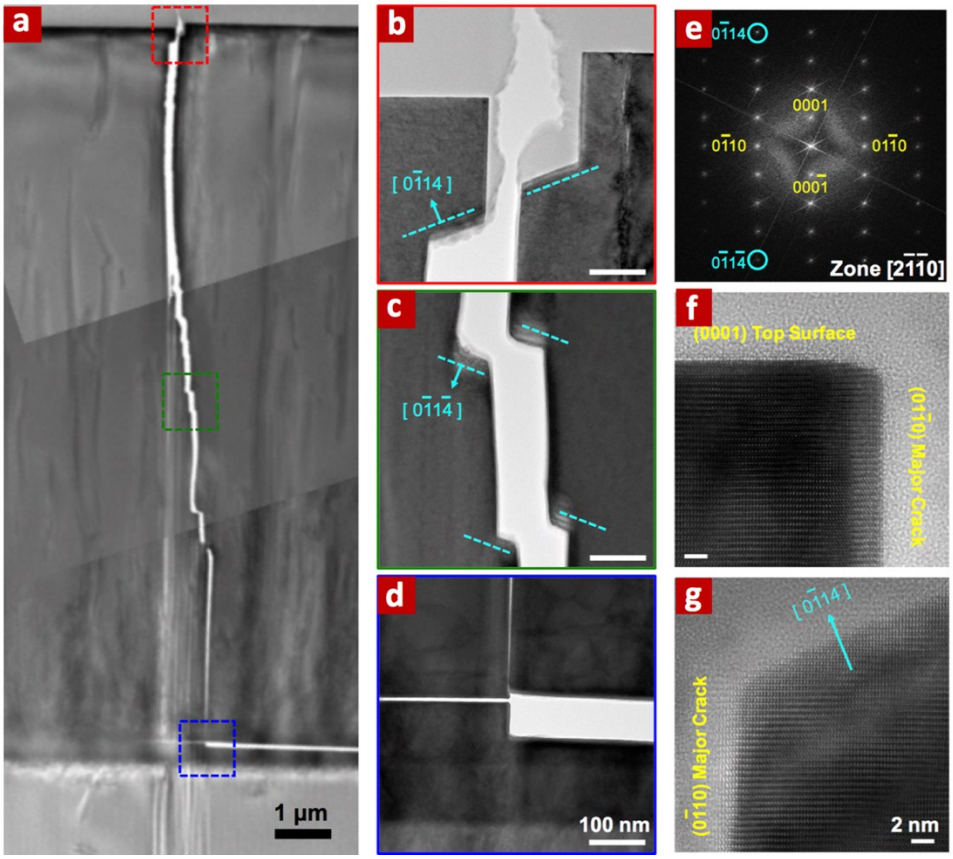

Figure S11. Crack plane determination by TEM. a-d. Cross-sectional TEM image showing cracking from the Si interface propagated to the top surface with cracks gliding on $\{01\bar{1}4\}$ planes and maintaining a dominant $\{01\bar{1}0\}$ crack plane. **e.** FFT pattern used to determine the

minor cracking planes and **f-g.** magnified HR-TEM image near the top surface of a small crack on the $\{01\bar{1}4\}$ plane.

VII. Determination of TDD by selective etching

The grown GaN-on-Si was immersed in H_2SO_4:H_3PO_4 (3:1) solution at 270 °C to selectively etch the the mixed and screw dislocations in GaN disk. The Figure S1a shows the top view microscope images showing a number of dark pits at the center. The dislocation density from the pit counting is 1.2×10^7 cm^{-2} (12 pits in 10μm^2) which agrees well with that deduced from the TEM analysis.

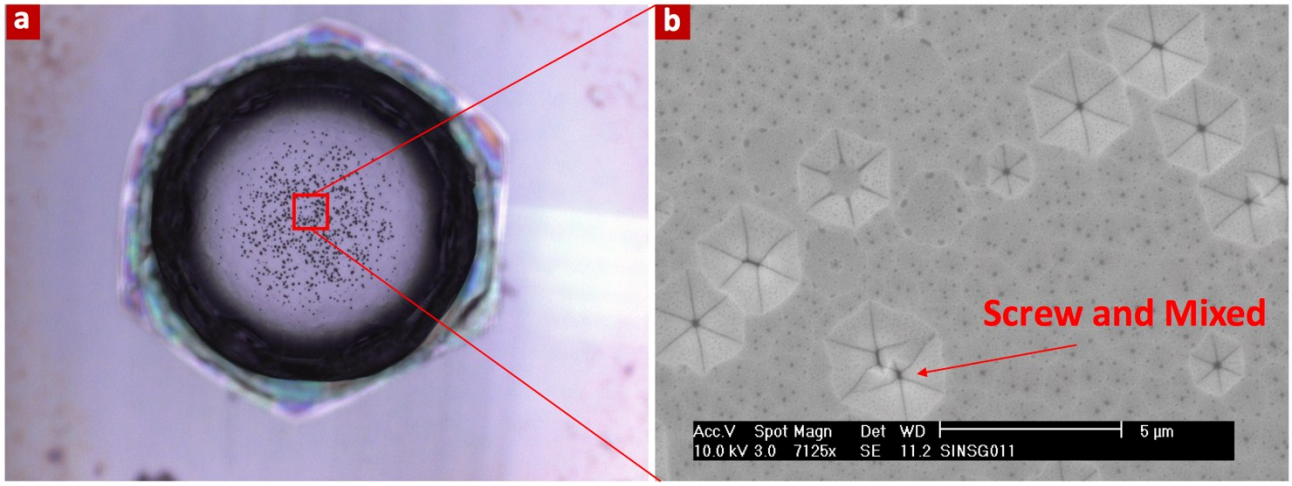

Figure S12. Dislocation selective etching. a. Top view microscope image after etching **b.** Top view SEM image near the center of the disk where most dislocations were found.

VIII. Calculation of *Ron*

The MISFET device R_{on} is calculated by considering the device active area.[3] The device trench width is 4 µm and gate width is 50 µm. The pitch of the device was calculated by adding the drift layer thickness 19 µm to the trench width in order to account for the current spreading in the drift region. Therefore, the active area of the device is 23 µm (pitch) × 69 µm (50 µm gate width + 19 µm drift region thickness)

$$R_{on} = \left[\frac{1V(V_{DS}=1V)}{5.03\times10^{-4}A\ (I_{DS}\ at\ V_{DS}=1V\ and\ V_{GS}=20V)}\right] \times 1.59 \times 10^{-5} cm^2 (Active\ Area) = 31.6\ m\Omega.cm^2$$

IX. MISFET hysteresis

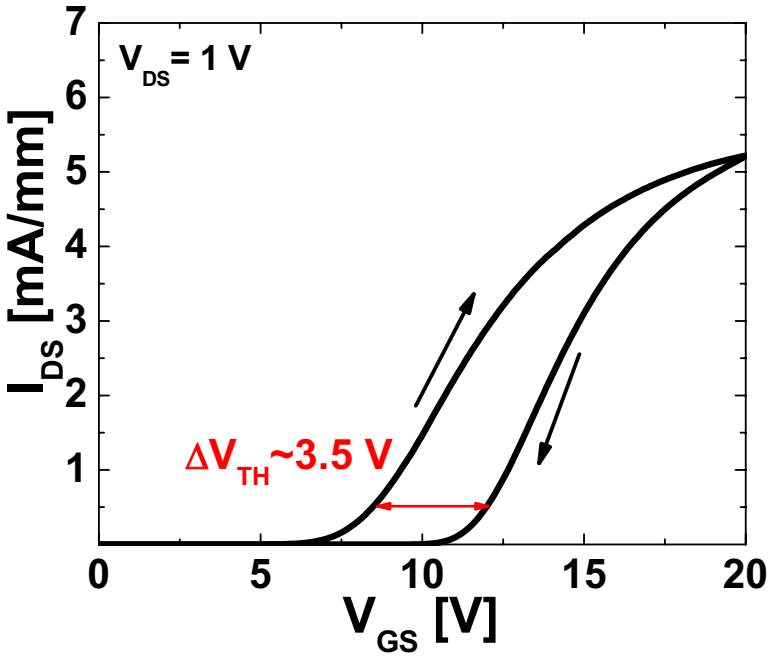

Figure S13. Threshold voltage shift. Linear transfer characteristics (I_{DS}-V_{GS}) at V_{DS} = 1V with different voltage sweep direction.

X. References

[1] W. A. Brantley, *J. Appl. Phys.* **1973**, *44*, 534.

[2] A. Polian, M. Grimsditch, I. Grzegory, *J. Appl. Phys.* **1996**, *79*, 3343.

[3] C. Gupta, C. Lund, S. H. Chan, A. Agarwal, J. Liu, Y. Enatsu, S. Keller, U. K. Mishra, *IEEE Electron Device Lett.* **2017**, *38*, 353.