Fluctuation and Noise Letters

Energy-dissipation Limits in Variance-based Computing

Sri Harsha Kondapalli, Xuan Zhang and Shantanu Chakrabartty

Electrical and Systems Engineering, Washington University in St Louis
One Brookings Drive, St Louis, MO 63130, USA
Email: {sriharshakondapalli, shantanu}@wustl.edu

Received 15 October 2017
Revised 30 November 2017

Variance-based logic (VBL) uses the fluctuations or the variance in the state of a particle or a physical quantity to represent different logic levels. In this letter we show that compared to the traditional bi-stable logic representation the variance-based representation can theoretically achieve a superior performance trade-off (in terms of energy dissipation and information capacity) when operating at fundamental limits imposed by thermal-noise. We show that, in addition to the universal KT $\ln(1/\epsilon)$ energy dissipation required for a single bit flip, a bi-stable logic device needs to dissipate at least 4.35KT/bit of energy, whereas under similar operating conditions, a VBL device reduces the additional energy dissipation requirements down to sub-KT/bit. These theoretical results are general enough to be applicable to different instantiations and variants of VBL ranging from digital processors based on energy-scavenging or to processors based on the emerging valleytronic devices.

1. Introduction

At a fundamental level any form of digital computation involves repeated and controlled transition between different logic states. Traditionally, these logic states are represented and implemented using potential wells that are separated from each other by an energy barrier. The potential wells are assumed to be stable configurations and any fluctuation or variance in these configurations is treated as noise. For example, in a standard CMOS logic the logic state is represented by the signal mean (average voltage or current) and the signal variance captures the effect of thermal fluctuations or environmental interference. For a spintronic device [1] the logic states are represented by the state of magnetic spin of the electrons; in a phase-change device like memristor [2] or FeRAM [3] the logic states are represented by the static alignment of the molecules. From a statistical point of view, the two logic states (denoted by '1' and '0') are represented by the means (0 and μ) of the two probability distributions that are separated from each other by an energy-barrier, as shown in Figure 1(a). Note that since the physics of the two configurations are assumed to be similar, the variances of the distributions can be assumed to be equal and the probability of error can be estimated by the overlap of the distributions (shown in Fig. 1(a)). In this paper, we investigate an alternate logic representation

where instead of the mean, the variances of the state configurations are used for representing logic levels 0 and 1. The statistical representation of the variance-based logic (VBL) [4] is shown in Fig. 1(b) where logic '0' is represented by a configuration with small fluctuations (or variance), and logic '1' is represented by a configuration with large fluctuations (or variance). Note that in Fig. 1(b), the two distributions have the same mean value which therefore does not carry any logic information. Also note that VBL representation is different from a noise based logic (NBL) [5] where the orthogonal patterns of noise carried the digital information, unlike the change in signal variance in the case of VBL.

VBL is applicable to devices and systems where the shape of the energy levels (or equivalently the momentum of the particles) can be changed. One such example is a system that is powered by scavenging energy from ambient sources. In this case, the asymmetry in the electrical impedance seen by the system ground and as seen by the energy transducer leads to different variances in voltage levels at the supply and at the ground potential. In [4] we have exploited the voltage variances to implement different forms of VBL logic gates and circuits. Another example where VBL could be applicable are processors based on valleytronic devices [6] where the curvature of the energy-levels (or equivalently the momentum of the particle trapped in the energy-level) could be changed to represent different logic levels. Our goal in this paper is to abstract out the physical level implementation of VBL and investigate the energy-efficiency limits of VBL as determined by thermal-noise.

In this regard, the energy-efficiency of VBL can be compared to the traditional mean-based logic (MBL) by visualizing the process of logic transition, as shown in Fig. 1(c) and (d). For a specific implementation of MBL the logic transition can be realized by transferring electrons from one potential well to another [7], [8], as shown in fig. 1(c). During the logic transition (0 to 1 for example), the energy barrier is lowered and the potential wells are reshaped in a way that the electrons move to the potential well corresponding to logic 1. The energy barrier E_1 is then restored and held until the next transition. Assuming irreversible computation and adiabatic transport of the electrons between the potential wells, the energy dissipated per logic transition or a bit for MBL, can be estimated to be twice the height of energy barrier ($E_{MBL} \approx 2 \times E_1$). The thermodynamic limits on E_1 is determined by the minimum energy required to enforce logic state transition and is atleast $KT\ln(2)$ Joules when the information content carried is close to zero. [9]. Note that this energy limit is independent of logic implementation or realization of the logic circuit. However, when the energy dissipated due the process of measurement is taken into account, a different lower-bound on the energy-dissipation per bit is obtained [10]. On the other hand, in a VBL device (as depicted in Fig. 1(d)) the electrons are either constrained in a narrow potential well (a low variance state '0') or the electrons are relatively free to move around in a broader potential well (a high variance state '1'). Transition between the logic states in VBL involves changing the shape of the potential well and hence involves adding or subtracting a fixed amount of energy E_2 ($= E_{VBL}$) from the system, as shown in Fig. 1(d). In this paper we derive the

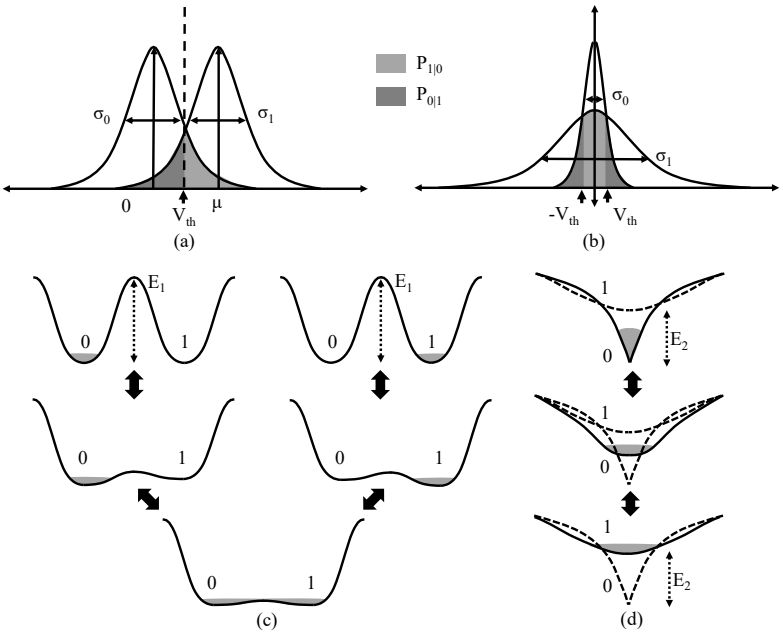

Fig. 1. Statistical representation of binary logic states '0' and '1' using (a) MBL and (b) VBL. The process of logic transition corresponding to (c) MBL and (d) VBL.

lower bounds on energy dissipation (E_{VBL}) for VBL and compare it with E_{MBL}.

2. Estimation of energy-dissipation per bit

Following an approach similar to what was presented in ref. [10], we first estimate the information capacity for MBL and VBL by estimating the average probability of error p_{avg} that is incurred in measuring the two logic levels. This can be estimated as

$$p_{avg} = p_0 p_{1|0} + p_1 p_{0|1} \tag{1}$$

where p_0, p_1 are apriori probability for logic state to be '0' or '1', and $p_{1|0}, p_{0|1}$ are conditional probability that captures incorrect measurement of the logic state. In an MBL representation as shown in Fig. 1(a), a threshold V_{th} could be used to distinguish between the logic levels in which case $p_{1|0}, p_{0|1}$ is given by the overlap between the distributions. Assuming equal apriori probability $p_0, p_1 = 0.5$ and the conditional distributions to be Gaussian with respective means 0 and μ and variances σ_0^2 and σ_1^2, the average probability of error [11] can be estimated as

$$p_{avg,MBL} = \frac{1}{4}[erfc(\frac{\mu - V_{th}}{\sqrt{2}\sigma_1}) + erfc(\frac{V_{th}}{\sqrt{2}\sigma_0})] \tag{2}$$

where,

$$erfc(x) = \frac{2}{\sqrt{\pi}} \int_x^{\infty} e^{-t^2} dt. \tag{3}$$

In case of VBL, the variances σ_0^2 and σ_1^2 corresponding to the two logic states could be measured by comparing the magnitude of the signal with respect to a threshold $\pm V_{th}$. The probability of error ($p_{err,VBL}$) is determined by the shaded region as shown in Fig. 1 (b). Following equation 1 and assuming equal apriori probabilities, the average probability of error $p_{err,VBL}$ can be estimated as

$$p_{avg,VBL} = \frac{1}{2}[1 - erfc(\frac{V_{th}}{\sqrt{2}\sigma_1}) + erfc(\frac{V_{th}}{\sqrt{2}\sigma_0})]. \tag{4}$$

The information transfer rate can be estimated by applying Shannon's capacity equation to an binary asymmetric channel with error probabilities $p_{0|1}$ and $p_{1|0}$ and is given by

$$\begin{aligned} C(p_{0|1}, p_{1|0}) = f_c[1 + p_1\{p_{0|1}\ln(p_{0|1}) + p_{1|1}\ln(p_{1|1})\} + \\ p_0\{p_{1|0}\ln(p_{1|0}) + p_{0|0}\ln(p_{0|0})\}] \end{aligned} \tag{5}$$

where f_c is the rate (or equivalently the speed) at which the logic state is measured.

The next step towards determining the energy efficiency of MBL and VBL is to estimate the energy dissipated during the process of logic transition. Similar to the approach presented in [10] we will realize both the logic by measuring an equivalent signal (mean or the variance) on an equivalent capacitance C_{meas}. For an MBL, the energy is dissipated during charging and discharging the sampling capacitor 'C_{meas}' to voltage μ at a rate of f_c is given by

$$P_{MBL} = f_c \times \frac{1}{2} C_{meas} \mu^2. \tag{6}$$

For a VBL, the power dissipation would be given by the difference in the signal variance corresponding to the two logic states and is given by

$$P_{VBL} = f_c \times C_{meas}(\sigma_1^2 - \sigma_0^2) \tag{7}$$

The power dissipated per bit (or the figure-or-merit for comparison) is then given by

$$FOM_{MBL,VBL} = \frac{P_{MBL,VBL}}{C(p_{0|1}, p_{1|0})}. \tag{8}$$

Note that the FOM is a function of probabilities $p_{1|0}$ and $p_{0|1}$ which in turn depend on the variances σ_0^2, σ_1^2 corresponding to the logic states 0 and 1 respectively. Since our objective is to determine the fundamental limits for MBL and VBL as constrained by thermal noise, we will assume $\sigma_0^2 = KT/C_{meas}$. Figure 2 (a) compares the FOM numerically estimated for MBL and VBL using equations 2- 8 and for different values of V_{th}, σ_1^2. The figure shows that for the FOM for MBL is bounded

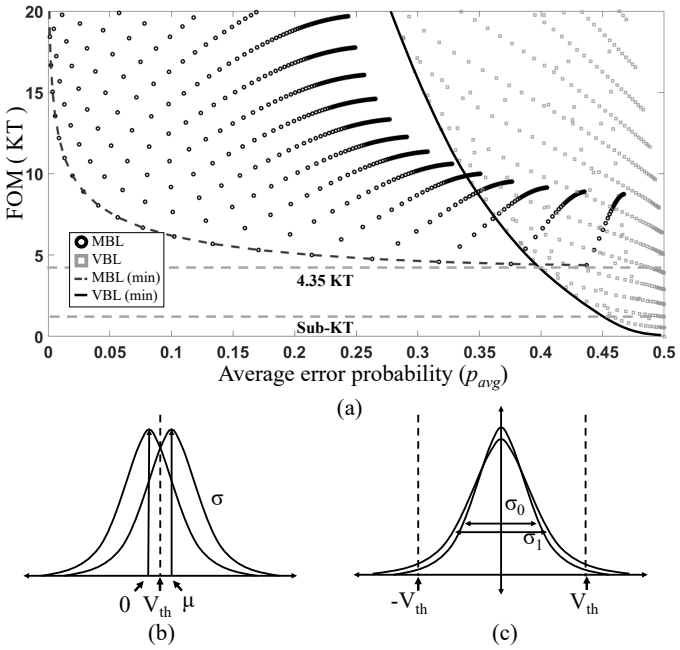

Fig. 2. (a) Numerical estimated FOM (energy dissipated per bit) corresponding to MBL and VBL for different values of V_{th} and σ_1. (b) Statistical distributions and thresholds corresponding to the (b) MBL operating at the 4.35KT per bit fundamental limit; and (c) VBL operating at sub-KT per bit fundamental limit.

from below and approaches a fundamental limit of 4.35 KT/bit. This limit is different from what was previously reported in [10] and therefore in this section we provide a brief derivation of this limit.

Revisiting the approximation provided in ref. [10] it can be seen that the capacity of MBL (C_{MBL}), when operating near the average probability of error $p_{avg} = p \approx 0.5$. Assuming a binary symmetric channel with $\sigma_1 = \sigma_0$, the Shannon capacity equation given by equation 5 can be rewritten as

$$C_{MBL}(p) = f_c[1 + p\log_2 p + (1-p)\log_2(1-p)]. \tag{9}$$

Defining Δp as $\Delta p = p_{avg} - 0.5$ and using a Taylor series expansion of C_{MBL} around $p_{avg} = p = 0.5$, equation 9 leads to,

$$\begin{aligned} C_{MBL}(\Delta p)|_{p\approx 0.5} &= C(p) + \frac{C'(p)}{1!}\Delta p + \frac{C''(p)}{2!}\Delta p^2 + ... \\ &= \frac{2}{\ln 2} f_c(\Delta p)^2 \end{aligned} \tag{10}$$

Assuming that the variance of measurement $\sigma_0^2 = \sigma_1^2 = \frac{KT}{C_{meas}}$ as determined by

thermal-noise and $V_{th} = \frac{\mu}{2}$, Δp is given by

$$\Delta p \approx \frac{g(0)\mu}{2} = \frac{\mu}{2\sqrt{2\pi}\sigma} = \frac{\mu}{2\sqrt{2\pi KT/C_{meas}}} \tag{11}$$

where g(.) is the Gaussian distribution function. Using Eq. (10), the capacity is given by

$$C_{MBL}|_{p\approx 0.5} = \frac{\mu^2}{(4\pi \ln 2)\frac{KT}{C_{meas}}} f_c \tag{12}$$

which leads to the fundamental FOM limit as

$$FOM_{MBL|min} = \frac{P_{MBL}}{C_{MBL}|_{p\approx 0.5}} \approx 4.35KT/bit. \tag{13}$$

This limit has been verified using numerical simulation and the results are summarized in Fig. 2(a). It can be also seen in Fig. 2(a) that the FOM limit for VBL could be lower than the MBL limit and in some cases the FOM approaches sub-KT per bit. For VBL sub-KT per bit limit is achieved when the respective variances σ_0 and σ_1 are approximately equal (implying $p_{avg} \approx 0.5$) and the threshold V_{th} samples only the tails of the distribution, as shown in Fig. 2(c). To understand why VBL can achieve sub-KT per bit limit, in Fig. 3 we compare the channel capacity $C(p_{0|1}, p_{1|0})$ for MBL and VBL, numerically estimated for different values of V_{th} and σ_1. Fig. 3 shows that while for MBL the information capacity approaches zero when the $p_{avg} \approx 0.5$, this is not the case for some instances of VBL when V_{th} is located around the tails of the distribution. In the above derivation, we have ignored the energy incurred by the switching circuit to convey the VBL levels, albeit the logic '0' and '1'. For VBL, the switch will effectively control the width of the potential well, shown in Fig. 1 (b), which in turn will change the noise-variance. Therefore, the energy dissipation to convey one bit of information is also determined by the minimum energy dissipated to trigger a switch, which is $KT\ln(1/\epsilon)$, ϵ being the probability of error in case of VBL. [9, 12]. In the limit of $\epsilon = 0.5$, this will result in the Brillouin limit of $KT\ln(2)$ which needs to be added to the lower bound of VBL.

3. Comparison of Signal-to-Noise Ratio for MBL and VBL

In [13] it was proposed that one of methods to approach the fundamental limit of energy-dissipation for MBL was to use error-correcting codes to compensate for high p_{avg}. A more practical approach would be to first boost the signal-to-noise ratio (SNR) of the measurement through repeated sampling and statistical averaging. Given N independent and identically distributed (iid) random samples x_1, x_2, ... x_N from a distribution with mean μ and variance σ^2, the sample mean ($\hat{x}$) is defined as $\hat{x} = \frac{\Sigma_{i=1}^{N} x_i}{N}$ and sample variance is given by $\hat{\sigma}^2 = \frac{\Sigma_{i=1}^{N}(x_i - \hat{x})^2}{N-1}$. The signal-to-noise ratio (SNR) for the measurement is given by

$$SNR = \frac{E[\hat{x}]^2}{E[\hat{\sigma}^2]} \tag{14}$$

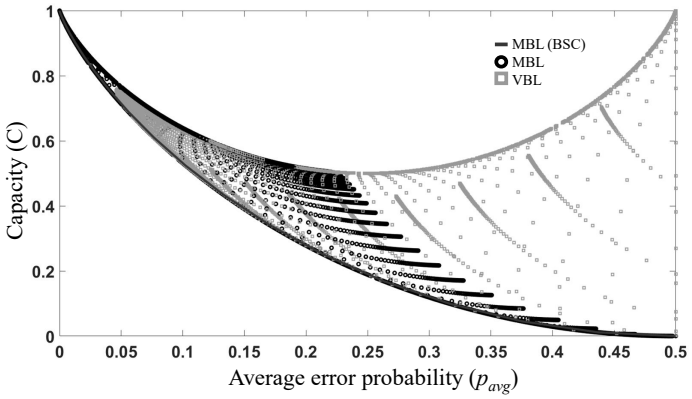

Fig. 3. Comparison of numerically estimated information capacity C as a function of the average probability of error p_{avg}, corresponding to MBL and VBL and for different values of V_{th} and σ_1.

In case of MBL, it is given by

$$SNR_{MBL} = \frac{N\mu^2}{\sigma^2} \tag{15}$$

Even if the samples are drawn from any given probability distribution the definition of SNR_{mean} holds. Where as the variance of the sample variance becomes a function of fourth order moment and is estimated to be [14]

$$E[(\hat{\sigma}^2 - \sigma^2)^2] = \sigma^4[\frac{2}{(N-1)} + \frac{\kappa}{N}] \tag{16}$$

were κ is the kurtosis of the probability distribution. A generalized expression for SNR_{var} is given as

$$SNR_{VBL} = \frac{1}{\frac{2}{(N-1)} + \frac{\kappa}{N}} \tag{17}$$

It can be seen that SNR_{MBL}, shown in equation. 15, increases with increase in μ and N and with the decrease in variance (σ^2). On the other hand SNR_{VBL}, shown in equation. 17, is independent of parameter σ and only increases with N. In Fig. 4(a) we show the regions where $SNR_{VBL} \geq SNR_{MBL}$ and $SNR_{VBL} \leq SNR_{MBL}$.

4. Hybrid Logic for energy scavenging processors

The result shown in Fig. 4(a) indicates that VBL and MBL techniques could be combined to form a hybrid logic topology where VBL is used when $\mu \leq \sqrt{2}\sigma$, and MBL is used when $\mu \geq \sqrt{2}\sigma$. The scenario occurs in energy scavenging processors [15] where the ambient energy (for example radio-frequency signals or vibrations) could serve as source of high-variance. In a traditional approach, the source of energy is harvested and rectified to create a stable voltage level μ which could then be

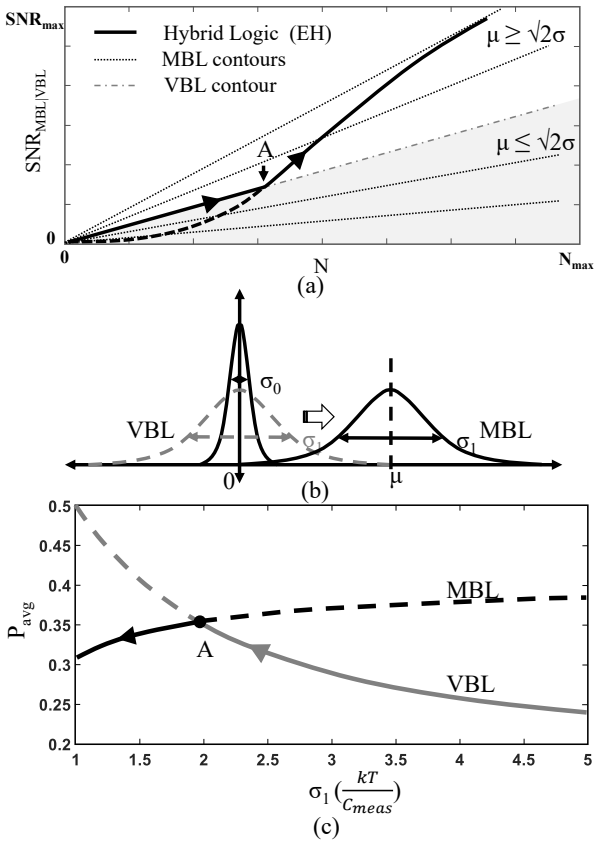

Fig. 4. Rationale for a hybrid logic that combines MBL and VBL - (a) plot showing regions where VBL (or MBL) yields a higher SNR compared to MBL (or VBL) with 'A' being the transition point between the two logic topologies; (b) Transition between VBL to MBL in an energy-scavenging system; and (c) plot showing the variation in the average probability of error p_{avg} for different values of σ_1 with 'A' being the transition point to switch between MBL and VBL.

used to implement MBL based processing. This process is illustrated in Fig. 4(b) where during the startup phase $\mu \leq \sqrt{2}\sigma$ is satisfied and therefore VBL would be more attractive. As more energy is harvested and rectified, $\mu \geq \sqrt{2}\sigma$ it is more attractive to use MBL for computing. The proposed hybrid logic should also provide improvements in reliability as the variance of the logic level σ_1 reduces in addition to the increase in μ. Fig. 4(c) shows the estimated p_{avg} corresponding to MBL and VBL when σ_1 is varied. The comparison shows an optimal transition point labeled as 'A' where switching the logic style from VBL to MBL yields a better reliability in terms of p_{avg}. Future work would entail practical implementation of the hybrid logic using topologies similar to that of [4] and comparing its performance with other energy harvesting logic topologies [15, 16].

Acknowledgements

This work was supported in part by a research grant from the National Science Foundation CNS1646380.

References

[1] B. Behin-Aein, D. Datta, S. Salahuddin and S. Datta, "Proposal for an all-spin logic device with built-in memory", *Nature nanotechnology* **5** (2010) 266–270.

[2] D. B. Strukov, G. S. Snider, D. R. Stewart and R. S. Williams, "The missing memristor found", *nature* **453** (2008) 80.

[3] M. Zwerg, A. Baumann, R. Kuhn, M. Arnold, R. Nerlich, M. Herzog, R. Ledwa, C. Sichert, V. Rzehak, P. Thanigai et al., "An 82μa/mhz microcontroller with embedded feram for energy-harvesting applications", in *Solid-State Circuits Conference Digest of Technical Papers (ISSCC), 2011 IEEE International* (IEEE, 2011), pp. 334–336.

[4] S. H. Kondapalli, X. Zhang and C. Shantanu, "Variance-based digital logic for energy harvesting internet-of-things", in *IEEE Symposium on Circuits and Systems (ISCAS)* (IEEE, 2017).

[5] H. Wen and L. B. Kish, "Noise-based logic: Why noise? a comparative study of the necessity of randomness out of orthogonality", *Fluctuation and Noise Letters* **11** (2012) 1250021.

[6] C. E. Nebel, "Valleytronics: Electrons dance in diamond", *Nature materials* **12** (2013) 690.

[7] R. W. Keyes and R. Landauer, "Minimal energy dissipation in logic", *IBM Journal of Research and Development* **14** (1970) 152–157.

[8] C. H. Bennett, "The thermodynamics of computationa review", *International Journal of Theoretical Physics* **21** (1982) 905–940.

[9] L. B. Kish and C. G. Granqvist, "Energy requirement of control: Comments on szilard's engine and maxwell's demon", *EPL (Europhysics Letters)* **98** (2012) 68001.

[10] L. B. Kish, "Thermal noise driven computing", *Applied Physics Letters* **89** (2006) 144104.

[11] B. E. Akgul, L. N. Chakrapani, P. Korkmaz and K. V. Palem, "Probabilistic cmos technology: A survey and future directions", in *Very Large Scale Integration, 2006 IFIP International Conference on* (IEEE, 2006), pp. 1–6.

[12] L. B. Kish and D. K. Ferry, "Information entropy and thermal entropy: apples and oranges", *arXiv preprint arXiv:1706.01459* .

[13] V. Guruswami and A. Rudra, "Error correction up to the information-theoretic limit", *Communications of the ACM* **52** (2009) 87–95.

[14] E. Cho, M. J. Cho and J. Eltinge, "The variance of sample variance from a finite population", *International Journal of Pure and Applied Mathematics* **21** (2005) 389.

[15] W. Zhao, K. Bhanushali and P. Franzon, "Design of a rectifier-free uhf gen-2 compatible rfid tag using rf-only logic", in *RFID (RFID), 2016 IEEE International Conference on* (IEEE, 2016), pp. 1–6.

[16] S. Briole, C. Pacha, K. Goser, A. Kaiser, R. Thewes, W. Weber and R. Brederlow, "Ac-only rf id tags for barcode replacement", in *Solid-State Circuits Conference, 2004. Digest of Technical Papers. ISSCC. 2004 IEEE International* (IEEE, 2004), pp. 438–537.