An Energy-Efficient High-Swing PAM-4 Voltage-Mode Transmitter

Lejie Lu, Yong Wang, Hui Wu
University of Rochester
Rochester, NY, USA
{lejie.lu,yong.wang,hui.wu}@rochester.edu

ABSTRACT

As the data rate of high-speed I/Os continues to increase, four-level pulse amplitude modulation (PAM-4) is adopted to improve the bandwidth density and link margin at 50 Gb/s and beyond. Compared to non-return-to-zero (NRZ) signaling, however, the PAM-4 eye height is reduced, which calls for larger transmitter swing to maintain signal-to-noise-ratio. A new energy-efficient transmitter is proposed to generate large swing PAM-4 signals with a cascode voltage-mode driver and supporting pre-drivers and logic circuits. By reconfiguring the pull-up and pull-down branches based on the transmit data and steering the bypass currents, the proposed voltage-mode driver significantly reduces power consumption compared to conventional implementation while maintaining impedance matching. Voltage stacking technique is adopted for pre-drivers to further improve energy efficiency. To demonstrate the new transmitter design, a prototype 56 Gb/s PAM-4 transmitter is designed using a generic 28-nm CMOS technology with a 2-V power supply voltage. It achieves a overall output swing of 2 V and a minimum eye height of 490 mV with good linearity (98.7% level separation mismatch ratio). Compared to a conventional voltage-mode transmitter design with the same swing, the static power consumption of the new transmitter is reduced almost by half (from 30 mW to 16 mW), and its overall energy efficiency improves from 0.7 pJ/b to 0.5 pJ/b.

CCS CONCEPTS

• **Hardware → Metallic interconnect**; **Wireline communication**;

KEYWORDS

PAM-4, high swing, low power, transmitter driver

ACM Reference Format:
Lejie Lu, Yong Wang, Hui Wu. 2018. An Energy-Efficient High-Swing PAM-4 Voltage-Mode Transmitter. In *ISLPED '18: ISLPED '18: International Symposium on Low Power Electronics and Design, July 23–25, 2018, Seattle, WA, USA.* ACM, New York, NY, USA, 6 pages. https://doi.org/10.1145/3218603.3218651

ISLPED '18, July 23–25, 2018, Seattle, WA, USA

ACM ISBN 978-1-4503-5704-3/18/07…$15.00
https://doi.org/10.1145/3218603.3218651

1 INTRODUCTION

Driven by the ever-increasing demands by data centers, mobile devices, video streaming services, internet-of-things, and automobile sensor fusion, the I/O bandwidths of CPUs, GPUs and ASIC switches continue to double every 3-4 years, now reaching 50 Gb/s per lane. To enable such ultra-high speed communication in integrated circuits, spectral efficient PAM-4 modulation has been widely adopted to increase the bit rate while keeping the baud rate relatively constant [1–3]. Several limitations of PAM modulation, however, need to be addressed in circuit design:

Compared to conventional non-return-to-zero (NRZ) signaling, PAM-4 suffers a 9.5-dB reduction in signal-to-noise-ratio (SNR) due to the splitting of signal levels from 2 to 4 in the voltage domain. The current practice is to rely on advanced equalization techniques to compensate for the SNR loss, at both the transmitter and receiver sides. The complex equalization circuits, particularly the decision-feedback equalizer (DFE), consume large amount of power. The link power budget fundamentally limits the transmission distance of PAM-4 signals in a lossy channel [4].

Another solution to overcome the SNR penalty is to use a larger PAM-4 signal amplitude at the transmitter output. [4] shows that 1.5-V transmitter output swing (peak-to-peak amplitude) is required for PAM-4 signaling in an 8-cm on-chip channel (or 4-cm in PAM-8). Such a high-swing transmitter allows the link to use less complex equalization. It also relaxes the gain requirement of the receiver front-end, which improves the bandwidth and reduces noise [4].

More importantly, a high-swing transmitter can extend the transmission distance of the link, and hence enables new interconnect architectures based on a transmission-line link bus (TLLB). The latter is recently proposed as an alternative for on-chip communication [5, 6]. Compared to network-on-chip (NoC) designs, it offers significantly lower communication latency. This not only improves the performance of the multi-core chip, but also reduces the overall system power consumption [7].

Still, the energy efficiency of a high-swing PAM-4 transmitter is critical in the overall system power budget, especially at 50 Gb/s and beyond. For this reason, PAM-4 modulation is typically implemented within the output driver and therefore avoids amplifying analog waveforms. Instead, digital driver circuits such as a voltage-mode driver is preferred. Further, to ensure the generated PAM-4 signal is delivered to the channel faithfully, impedance matching at the transmitter output is required. The high-swing PAM-4 transmitter design has to be optimized to meet both goals.

Linearity issue is another challenge in PAM modulation. Compared to NRZ, PAM has more than one eye openings in the voltage domain. Non-linearity will result in different eye heights among them, which degrades bit-error-rate (BER). This effect is usually

quantified by the level separate mismatch ratio (RLM):

$$RLM = (N-1)\frac{V_{min}}{V_{pp}} \tag{1}$$

for PAM-N where V_{min} is the smallest eye height in all eye openings, V_{pp} is the peak-to-peak eye height. At least 92% RLM is recommended by CEI-56G and IEEE802.3bs standards.

This paper is organized as follows: in Section 2, we will review conventional PAM-4 transmitter designs and briefly compare them. Then, we will evaluate power consumption of a voltage-mode driver as a baseline for later comparison. In Section 3, the proposed transmitter is presented, and its static and dynamic power consumption analyzed. Finally, the design and simulation results of a 56-Gb/s prototype transmitter are demonstrated in Section 4.

2 CONVENTIONAL PAM-4 TRANSMITTERS

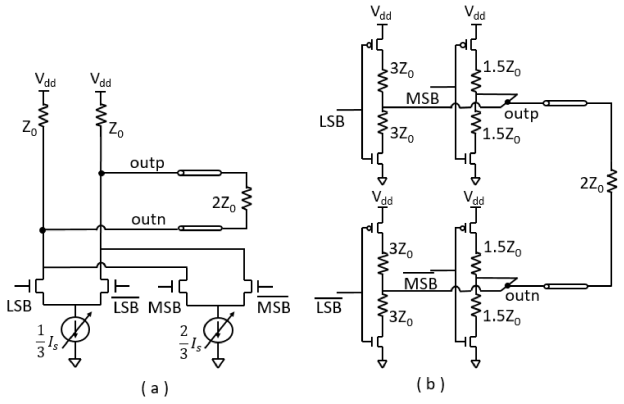


Figure 1: Conventional PAM-4 drivers: (a) CML; (b) voltage-mode.

Typically PAM-4 signals are generated directly by the output driver in the transmitter, which is modified from one of the basic NRZ drivers: current-mode logic (CML), or voltage-mode.

Fig. 1-a shows the conventional PAM-4 CML driver [8, 9]. It uses two differential pairs to combine the output currents corresponding to the upper (MSB) and lower (LSB) bits of a PAM-4 symbol. The currents are weighted by the tail current sources. The differential output current can take four values ($\pm I_S$ and $\pm 1/3 I_S$). Resistors Z_0 convert the differential output current to a differential output voltage (outp-outn), and also serve to achieve impedance matching with the differential load ($2Z_0$).

A voltage-mode driver for NRZ signals uses two inverters to drive the differential output, and impedance matching is achieved by incorporating a series resistor in the pull-up and pull-down paths at the output. Such source-series-terminated (SST) drivers [10] essentially function as switched voltage dividers to generate the output voltage.

A conventional PAM-4 voltage-mode driver is modified from an NRZ one, as shown in Fig. 1-b. To implement PAM-4 modulation and maintain impedance matching at the same time, the SST inverter on each side of the load is split into two branches with $1.5Z_0$ and $3Z_0$ termination, respectively. MSB and LSB signals control these two branches separately. We can easily find the output impedance is always $1.5Z_0//3Z_0 = Z_0$ in four different data symbols.

In comparison, CML drivers typically exhibit inferior linearity due to the headroom limitation on the tail transistor [11–13]. It also consumes more power compared to voltage-mode drivers. Thanks to its better linearity and energy efficiency, voltage-mode drivers are more suitable for PAM applications.

It is worth noting [11] proposed combining both CML and voltage-mode drivers to enlarge the swing up to 1.3 V using 1-V power supply voltage. Beyond 1.3 V, however, the swing is limited again by the CML linearity.

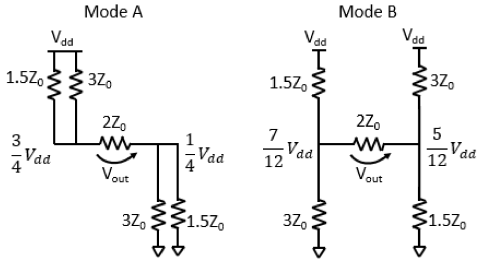


Figure 2: Equivalent circuit of a conventional PAM-4 VM driver for the analysis of static power consumption.

In the following, we analyze the power consumption of a conventional PAM-4 transmitter in order to use it as baseline to compare with the proposed new design later in this paper. Note that the transmitter's power consumption comprises static power dominated by the main driver and dynamic power dominated by the pre-driver. We focus on the former here since it is typically much larger than the latter.

To evaluate the static power, we have to first analyze it in the four PAM-4 symbols, respectively. Figure 2 shows the emphstatic equivalent circuit for the PAM-4 voltage-mode driver. It has two modes of operation, depending on the data symbol. When (MSB,LSB)=(0,0) or (1,1), the static power consumption is expressed as:

$$P_{D,A} = \frac{1}{4}\frac{{V_{dd}}^2}{Z_0} \tag{2}$$

When (MSB,LSB)=(1,0) or (0,1), the static power consumption is:

$$\begin{aligned} P_{D,B} &= I_{tot} V_{dd} \\ &= \left(\frac{V_{dd} - \frac{7}{12}V_{dd}}{1.5Z_0} + \frac{V_{dd} - \frac{5}{12}V_{dd}}{3Z_0} \right) V_{dd} \\ &= \frac{17}{36}\frac{V_{dd}^2}{Z_0} \end{aligned} \tag{3}$$

Note that the total impedance between V_{dd} and ground in Mode B is:

$$Z_{tot} = \frac{36}{17} Z_0 \tag{4}$$

The total static power can be estimated as:

$$P_{D,tot} = \frac{1}{2}P_{D,A} + \frac{1}{2}P_{D,B} = \frac{13}{36}\frac{V_{dd}^2}{Z_0} \tag{5}$$

assuming that the PAM-4 symbols have equal probability in the input data.

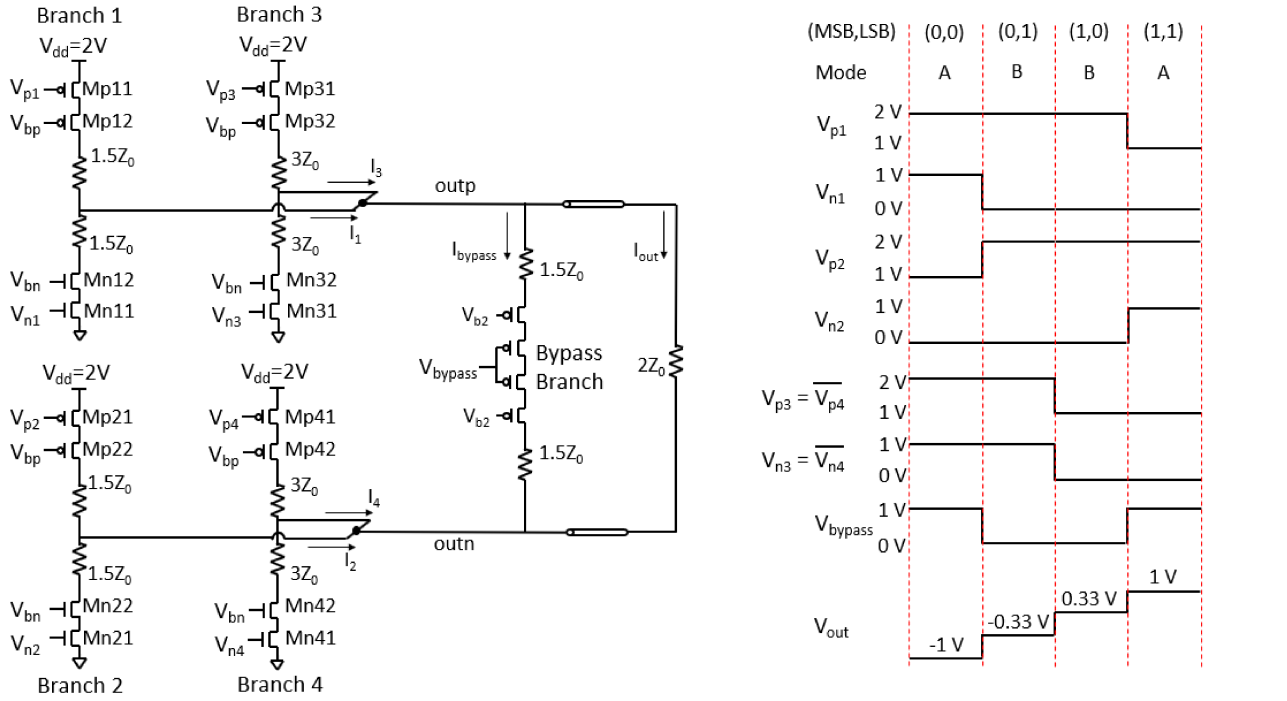


Figure 3: Schematic of proposed PAM-4 VM driver and voltage waveforms at critical nodes when transmitting four types of signal

3 NEW PAM-4 TRANSMITTER

3.1 Proposed PAM-4 Voltage-Mode Transmitter

In this work, we choose the voltage-mode operation for the new PAM-4 transmitter. By adopting a new circuit structure and better control on the current paths, the energy efficiency can be further improved.

Fig. 3 shows the proposed PAM-4 voltage-mode driver. In the following analysis, the design targets a 2-V transmitter output swing, and the power supply voltage V_{dd} is set at 2 V. Larger swing can be achieved by scaling up V_{dd}. There are several changes made from the conventional PAM-4 voltage-mode driver in Fig. 1-b:

- To accommodate the large V_{dd}, cascode transistors M_{pi2} and M_{ni2} (i=1-4) are added in each SST branch to isolate the switch transistors M_{pi1} and M_{ni1} (i=1-4) from the output node, and keeping their drain to source voltage (V_{ds}) below the breakdown voltage.
- Another branch is added across the differential output to bypass part of the output current when this bypass branch is enabled.
- The input voltages to the switch transistors (V_{ni} and V_{pi}, i=1-4), as shown in the static waveforms in Fig. 3, are no longer directly MSB and LSB signals. They are either level shifted, or changed in logic, or both.

This new driver still operates in two modes, as shown in Fig. 4. In Mode A, *i.e.*, when (MSB,LSB)=(0,0) or (1,1), Branch 1 and 2 are enabled ($S_{p1} = \overline{S_{n1}}$, $S_{p2} = \overline{S_{n2}}$), and the bypass branch is disabled. In this case, the new driver operates almost identical to

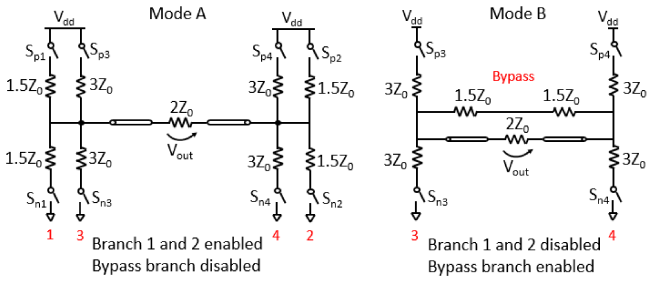


Figure 4: The two operation modes in the proposed PAM-4 voltage-mode driver. The switch and cascode transistor pair in Fig. 3 is shown as a switch for clarity. The control signals S_{ni} and S_{pi} are logic signals here, derived from the input voltage signals in Fig. 3. Branch 3 and 4 are always enabled since $S_{p3} = \overline{S_{n3}} = MSB$, $S_{p4} = \overline{S_{n4}} = \overline{MSB}$

the conventional one. In Mode B, when (MSB,LSB)=(0,1) or (1,0), Branch 1 and 2 are disabled, and the bypass branch is enabled. Now the circuit looks like an NRZ voltage-mode driver with the output current reduced due to the bypass. In both Mode A or B, it can be shown that the output impedance remains $3Z_0//1.5Z_0 = Z_0$ on both sides of the load, or $2Z_0$ differentially.

Fig. 5 shows the pre-driver and supporting logic circuits which generate the input voltages (V_{pi}, V_{ni} and V_{bypass}). Voltage stacking technique is used in these circuits with a middle power supply rail

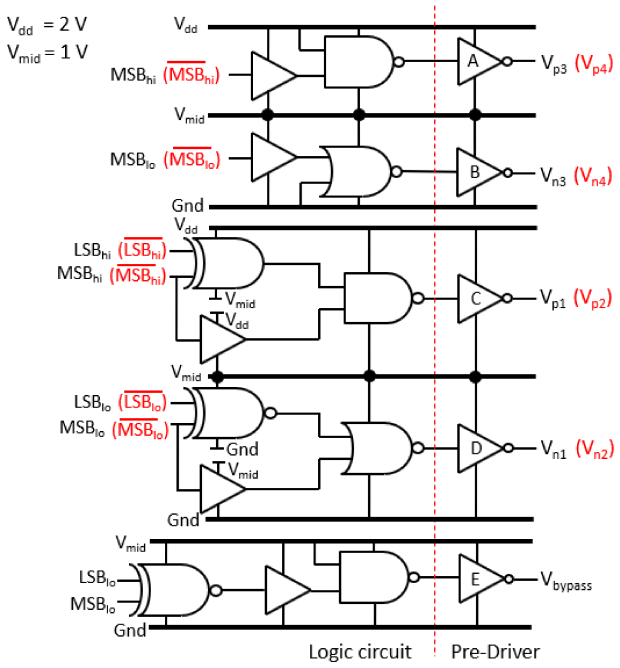
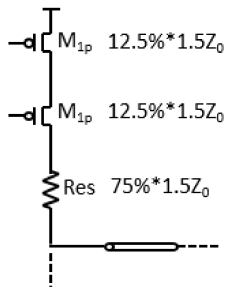


Figure 5: Pre-driver and supporting logic circuits which generate the input voltages to the main driver.

$V_{mid} = \frac{1}{2}V_{dd}$, which is 1 V in this design example. Using level-shifted, half-V_{dd} input signals can significantly reduce dynamic power, and voltage stacking further saves power.



Components	Size
M_{1p}	166u/30u
M_{1p}	166u/30u
Res	56.25 ohm

Figure 6: Resistance and transistor sizing in the SST branch.

In the SST and bypass branches, the output impedance is determined by the transistor's ON resistance and the series resistor. Ideally, the latter should dominate to minimize the detrimental effect of process, voltage and temperature variations (PVT) on the former [14], which is also highly nonlinear and varies with the gate voltages. However, small transistor ON resistance requires extremely large transistor size, and results in large parasitic capacitance, which increases dynamic power consumption. In our design, we set 75% of the output impedance from the series resistor and 25% from transistors. Fig. 6 shows an example of the transistor sizing in one SST branch.

3.2 Static Power Consumption Analysis

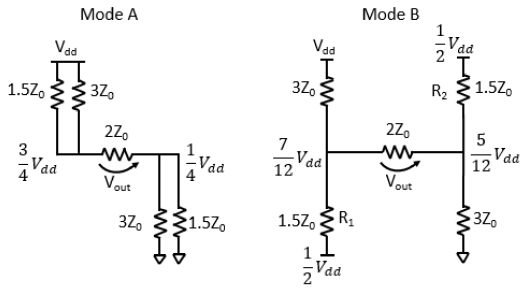


Figure 7: Equivalent circuits of the proposed PAM-4 voltage-mode driver for the analysis of static power consumption. The bypass branch is broken into two parts in the Mode B schematic to compare with Fig. 2.

As seen in Eqn. 5, higher power supply voltage V_{dd} leads to significant increase in the static power consumption in a conventional voltage-mode driver. In this new driver, voltage stacking is implicitly applied to reduce it.

Figure 7 shows the equivalent circuits for the new driver in the two operation modes. In Mode A, when (MSB,LSB) = (0,0) or (1,1), it is the same case as in a conventional voltage-mode driver:

$$P_{D,A} = \frac{1}{4}\frac{{V_{dd}}^2}{Z_0} \tag{6}$$

In Mode B, when (MSB,LSB)=(1,0) or (0,1), the total impedance between V_{dd} and ground is:

$$Z_{tot} = 3Z_0 + (3Z_0//2Z_0) + 3Z_0 = \frac{36}{5}Z_0 \tag{7}$$

Compared to Eqn. 4, the impedance is increased from $\frac{36}{17}Z_0$ to $\frac{36}{5}Z_0$. This leads to lower power consumption:

$$P_{D,B} = \frac{V_{dd}^2}{Z_{tot}} = \frac{5}{36}\frac{V_{dd}^2}{Z_0} \tag{8}$$

Now the total static power consumption is:

$$P_{D,tot} = \frac{1}{2}P_{D,A} + \frac{1}{2}P_{D,B} = \frac{7}{36}\frac{V_{dd}^2}{Z_0} \tag{9}$$

Compared to Eqn. 5, the static power consumption is reduced almost by half.

Clearly, the static power savings in this new design come from when transmitting the lower amplitude symbols, *i.e.*, when (MSB,LSB) = (0,1) or (1,0). In the conventional design, there is a direct current path from V_{dd} to ground going through 1.5Z_0 and 3Z_0 on both sides of the load (see Fig. 2). The wasted current is the price paid for impedance matching. In this new design, this wasted current is routed through both sides by the bypass branch (broke into two parts R_1 and R_2 in Fig. 7), and such current reuse reduces power consumption. Note that because of the circuit symmetry, the middle point in the bypass branch has a voltage of $V_{dd}/2$, which is essentially another application of voltage stacking technique in this circuit.

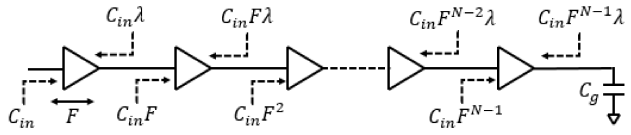


Figure 8: Switching capacitance in N stages Pre-driver

3.3 Dynamic Power Consumption Analysis

Dynamic power consumption is mainly contributed by the pre-drivers and supporting logic circuits. Even though the main driver also consumes dynamic power during the switching transient, it is small enough compared to its static power consumption [15]. To estimate the dynamic power consumption of the pre-driver, the total load capacitance of the pre-driver needs to be calculated first. Figure 8 shows the equivalent circuit of a pre-driver constructed as a buffer chain. C_{in} is the input gate capacitance of first stage, and C_g is the gate capacitance of the main driver. F is the fanout of each stage, and λ is the ratio of drain to gate capacitance.

Thus the total load capacitance of pre-driver can be expressed as:

$$\begin{aligned} C_{pre} &= \sum_{n=0}^{N-1} C_{in}\lambda F^n + \sum_{n=0}^{N-1} C_{in}F^n + C_g \\ &= \frac{(C_g - C_{in})(1+\lambda)}{F-1} + C_g \\ &\approx \frac{C_g(1+\lambda)}{F-1} + C_g \end{aligned} \tag{10}$$

Since C_{in} is small compared to C_g, C_{in} is ignored in above approximation. Then the dynamic power consumption of the pre-driver can be estimated as:

$$P_{D,pre} = \alpha_i f_s C_{pre} V_{dd,pre}^2 \tag{11}$$

where α_i is the average switching activity factor, since the data does not necessarily change states of internal nodes within the pre-drivers at every clock cycle [16]. In the proposed transmitter, Pre-driver A, B, C and D are responsible for driving switch transistors in the main driver. Since the size of these switch transistors are determined by their specified ON resistance, the dynamic power consumption of these pre-drivers should be similar to that in a conventional voltage-mode driver.

4 PROTOTYPE DESIGN AND SIMULATION RESULTS

To demonstrate the new PAM-4 transmitter, an integrated circuit prototype is designed for 56-Gb/s operation using Synopsys generic 28-nm CMOS technology. Power supply voltage V_{dd} is set at 2 V for 2-V maximum output swing. The load impedance Z_0 is set at 50 ohms. From Eqn. 5 and Eqn. 9, therefore, the static power consumption is reduced from 28.9 mW in the conventional design to 15.6 mW in the new design.

For dynamic power consumption, we use the following technology parameters: $\lambda \approx 0.5$, and $C_{gate} = 0.35$ fF/μm for PMOS and 0.4 fF/μm for NMOS. The total width of PMOS and NMOS transistors in the main driver are 268 μm and 229 μm, respectively. To minimize the transition delay, the fanout F is chosen as 2.5. Thus

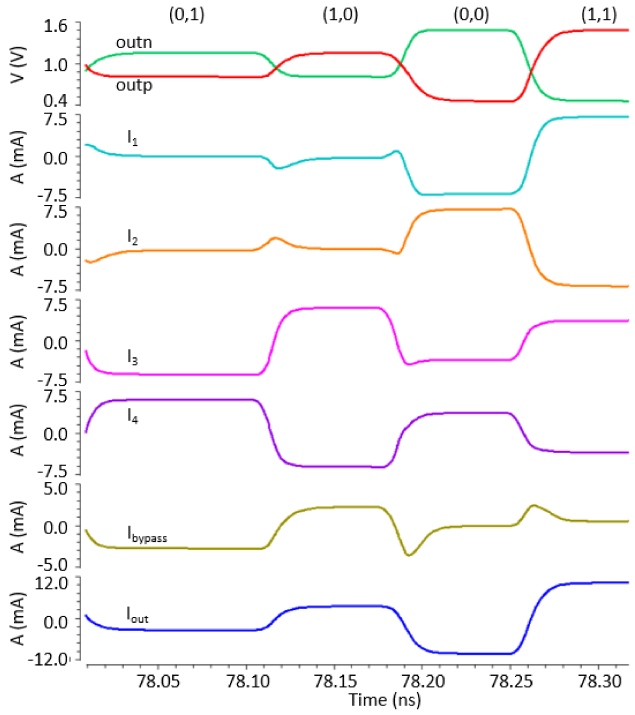


Figure 9: Current waveforms through different critical path

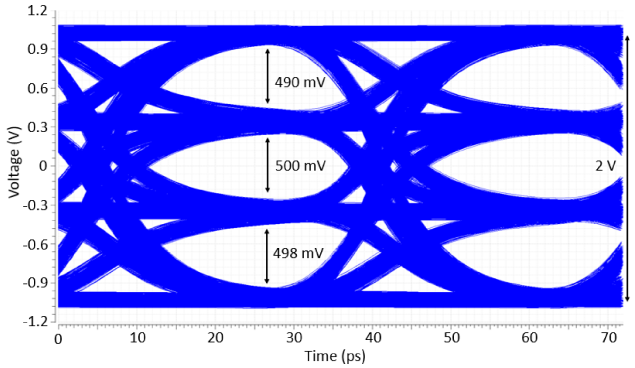


Figure 10: Eye diagram of the PAM-4 transmitter output.

the load capacitance of the pre-drivers A-D is 370 fF from Eqn. 10. If we assume average switching activity factor α_i=0.5, the total dynamic power consumption of the pre-drivers A-D running at 28 GBaud/s can be estimated from Eqn. 11:

$$P_{D,pre} = 2 \times 0.5 \times 28G \times 370fF \times (1V)^2 = 10.4mW \tag{12}$$

where the factor of 2 is for the differential signals. This part is same for both the conventional and new designs. The new design has additional dynamic power consumption from the pre-driver E driving the bypass branch. According to Fig. 3, the two switch transistors in bypass branch should be the same size as the PMOS transistors in Branch 1 and 2. Therefore the load capacitance of the pre-driver E is 248 fF, and its dynamic power consumption is

3.5 mW. So the overall dynamic power consumption is 13.9 mW for the new design.

To verify the design, transistor level simulation is performed using Cadence Custom IC Design tools. 15-bit pseudo-random bit sequence (PRBS-15) signal is applied as the input data and the total data length is 585 ns in time. To model the wiring parasitic capacitance, 1 fF to 4 fF capacitances are added along the critical signal path. The transmission channel uses a 12-cm long transmission line on an FR4 printed circuit board. S-parameters of the channel are extracted from electromagnetic simulation in Sonnet.

Fig. 9 shows the simulated waveforms of the output signal and currents through different branches in the main driver. All waveforms are quite clean without glitches, demonstrating good switching behavior. I_1, I_2, and I_{bypass} exhibit small dips and bumps due to charge redistribution during mode change transitions.

Fig. 10 shows the eye diagram of the transmitter output signal. Four different voltage levels are clearly generated for PAM-4 modulation. The overall output swing is 2-V, and the minimum eye opening is 590 mV. 98.6% RLM is achieved, which demonstrates good linearity of the new design.

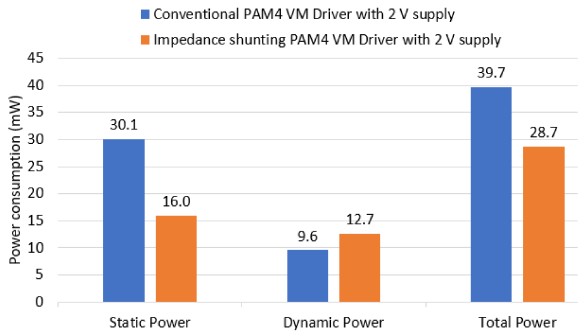


Figure 11: Power consumption comparison.

Figure 11 summarizes the power consumption of the conventional and the proposed PAM-4 transmitters with the same output swing. The static power is reduced almost by half from 30.1 mW to 16 mW, while the dynamic power from the pre-driver increases slight from 9.6 mW to 12.7 mW. The total power of the transmitter is reduced from 39.7 mW to 28.7 mW, and the energy efficiency improves from 0.71 pJ/b to 0.51 pJ/b. The simulation results match well with the analytical values.

By increasing the transmitter swing in this design, we can apply the proposed transmitter circuitry in multi-core chip system-level design such as [7], which proves higher transmitter swing can provide an average of 1.4x performance improvement over baseline and 1.75x overall energy-delay product improvement. With our new stacking and impedance shunting technique, energy is further reduced compared to design in [7], so overall performance will be much better.

5 CONCLUSION

In this paper, we propose a new voltage-mode driver circuit to generate high-speed high-swing PAM-4 signals. It utilizes cascode transistors to handle the increased power supply voltage to achieve larger voltage swing. A bypass branch is introduced, and together with two other SST branches, change the output current for PAM-4 modulation while maintaining the output impedance. This new design significantly improves the energy efficiency compared to the conventional PAM-4 voltage-mode driver. The pre-driver and supporting logic circuits use voltage stacking technique to achieve voltage levels compatible with the driver switch signals, which also improves energy efficiency. In a 56-Gb/s prototype PAM-4 transmitter designed using a generic 28-nm CMOS technology, the main driver saves 47% signaling power compared to a conventional voltage-mode driver, and the overall energy efficiency of the transmitter improves from 0.7 pJ/b to 0.5 pJ/b.

ACKNOWLEDGMENTS

This work is partially supported by NSF grants CCF1514284 and IIS1722847.

REFERENCES

[1] K. Gopalakrishnan et al. A 40/50/100Gb/s PAM-4 Ethernet Transceiver in 28nm CMOS. In *2016 IEEE International Solid-State Circuits Conference (ISSCC)*, pages 62–63, 2016.

[2] Y. Frans et al. A 56Gb/s PAM4 Wireline Transceiver Using a 32-Way Time-Interleaved SAR ADC in 16nm FinFET. In *2016 IEEE Symposium on VLSI Circuits (VLSI-Circuits)*, pages 1–2, 2016.

[3] A. Roshan-Zamir et al. A Reconfigurable 16/32 Gb/s Dual-Mode NRZ/PAM4 SerDes in 65-nm CMOS. *IEEE Journal of Solid-State Circuits*, 52(9):2430–2447, 2017.

[4] Y. Wang and H. Wu. Design High Bandwidth-Density, Low Latency and Energy Efficient On-Chip Interconnect. In *2017 IEEE/ACM International Symposium on Low Power Electronics and Design (ISLPED)*, pages 1–6.

[5] A. Carpenter et al. A Case for Globally Shared-Medium On-Chip Interconnect. In *2011 38th Annual International Symposium on Computer Architecture (ISCA)*, pages 271–281, 2011.

[6] A. Carpenter et al. Using Transmission Lines for Global On-Chip Communication. *IEEE Journal on Emerging and Selected Topics in Circuits and Systems*, 2(2):183–193, 2012.

[7] R. Afoakwa et al. High Swing Pulse-Amplitude Modulation of Transmission Line Links for On-Chip Communication. In *2018 IEEE International Symposium on Circuits and Systems (ISCAS)*, pages 1–5, 2018.

[8] P. C. Chiang et al. 60Gb/s NRZ and PAM4 Transmitters for 400GbE in 65nm CMOS. In *2014 IEEE International Solid-State Circuits Conference (ISSCC)*, pages 42–43, 2014.

[9] G. Steffan et al. A 64Gb/s PAM-4 Transmitter with 4-Tap FFE and 2.26pJ/b Energy Efficiency in 28nm CMOS FDSOI. In *2017 IEEE International Solid-State Circuits Conference (ISSCC)*, pages 116–117, 2017.

[10] M. Kossel et al. A T-Coil-Enhanced 8.5 Gb/s High-Swing SST Transmitter in 65 nm Bulk CMOS With $<<$16 dB Return Loss Over 10 GHz Bandwidth. *IEEE Journal of Solid-State Circuits*, 43(12):2905–2920, 2008.

[11] M. Bassi et al. A High-Swing 45 Gb/s Hybrid Voltage and Current-Mode PAM-4 Transmitter in 28 nm CMOS FDSOI. *IEEE Journal of Solid-State Circuits*, 51(11):2702–2715, 2016.

[12] Nazemi Ali et al. A 36Gb/s PAM4 Transmitter Using an 8b 18GS/S DAC in 28nm CMOS. In *2015 IEEE International Solid-State Circuits Conference (ISSCC)*, pages 1–3. IEEE, 2015.

[13] J. Lee et al. Design of 56 Gb/s NRZ and PAM4 SerDes Transceivers in CMOS Technologies. *IEEE Journal of Solid-State Circuits*, 50(9):2061–2073, 2015.

[14] K. L. Chan et al. A 32.75-Gb/s Voltage-Mode Transmitter With Three-Tap FFE in 16-nm CMOS. *IEEE Journal of Solid-State Circuits*, 52(10):2663–2678, 2017.

[15] K. Jung, Y. Lu, and E. Alon. Power Analysis and Optimization for High-Speed I/O Transceivers. In *2011 IEEE 54th International Midwest Symposium on Circuits and Systems (MWSCAS)*, pages 1–4, 2011.

[16] Emre Salman and Eby Friedman. *High Performance Integrated Circuit Design*. McGraw Hill Professional, 2012.