

# *A DC-coupled Biomedical Radar Sensor with Analog DC Offset Calibration Circuit*

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**Abstract**—A common problem of biomedical radar sensors is the DC offset at the output of radar receiver front-end. In this paper, a DC-coupled Doppler radar sensor system with an analog DC offset calibration circuit is proposed. The calibration circuit can track the change of DC offset continuously, and automatically remove the offset on the fly or in a controlled manner. The proposed calibration circuit uses pure analog components and does not require any digital signal processing (DSP) or software configuration. Compared to existing digitized solutions, the proposed analog calibration technique has the advantage of low cost, low complexity, extremely small delay, and very high resolution. Experiment demonstrates that input signals with a wide range of input DC offset can be processed. Hence the dynamic range of the baseband variable gain amplifier (VGA) can be maximized. Furthermore, the proposed DC offset calibration architecture can be easily adopted by other systems which also face DC offset problem.

**Keywords**— *biomedical radar sensor, Doppler radar, motion sensor, vital signs, DC offset, calibration, variable gain amplifier (VGA), receiver, front-end, mixer, dynamic range*.

## I. INTRODUCTION

Doppler radar is widely used as sensor in different measurement systems. The key applications include vital signs sensing, motion sensing, water level measurement, etc. In recent years, remote sensing and measurement using Doppler radar has gained great momentum in both research and industrial applications [1]-[4]. One of the biggest driving forces behind this is that the entire radar system can be integrated into a single system-on-chip (SOC) solution, which permits the technology to be realized with very low cost and small hardware size.

Doppler radar sensors can be used to sense the displacement of a target. When a Doppler radar is used to measure displacement of a target, the displacement changes the distance between the radar signal source and the target. The signal round trip delay between the radar and the target changes accordingly. This modulated time delay results in the phase modulation of the received signal. By comparing the received signal phase and the transmitted signal phase, the displacement of the target can be extracted.

Most Doppler radar systems adopt a homodyne receiver architecture. A common problem of these systems is the DC offset at the output of radar receiver front-end [5]. It may saturate the baseband amplifier, and reduce the dynamic range of the radar system. DC offset can come from either the radar's

hardware itself or from clutter reflection. Hardware DC offset comes from the imperfection of the components, such as mismatch in the components and local oscillator (LO) leakage. Components mismatch will cause DC operating shift, and LO leakage can mix with itself down to DC, which is known as self-mixing. DC offset originated from Clutter reflection is caused by the reflections from stationary objects near the. If an object near the target is stationary, then the radar will receive a signal reflected by the object with a constant phase. After down-conversion by the mixer, the receiver baseband output shows up as a DC value. Depending on the location of the object, the DC value will change. Both sources of DC offset will change with the environment, and affect the behavior of the radar sensor system. In the worst case, baseband amplifier can be saturated and the system will lose function completely.

To achieve the best dynamic range for the system, the baseband VGA needs to operate at its maximum gain. The maximum gain of VGA is decided by the total input signal level including both the DC and AC components. With a large DC offset in the system, the VGA gain must be reduced so that it will not saturate. An intuitive way to eliminate the DC offset problem is to block the DC completely, and AC-couple the output of receiver front-end to the input of the baseband amplifier [1]. However, this will distort the input signal and can lose useful information as the DC input is blocked completely. This is unacceptable in high precision applications such as unique identification [6] and medical diagnosis [7]. Several techniques to address the DC offset have been proposed in literature. Initially, people used manual calibration to tune out the DC offset [8]. It requires external equipment and must be performed whenever the testing environment changes. In [9], an adaptive feedback loop was proposed to adjust the DC bias of the operational amplifier (op-amp) and hence keep the amplifier always in saturation. The solution requires software to tune an external power supply. It monitors whether the baseband amplifier is saturated or not. If it is saturated, the software will try to adjust the baseband amplifier bias with a different setting. It will keep trying till the amplifier is recovered. The problem is that it is very time consuming, and the information during the DC-tuning period is lost. In [5], a customized integrated circuit with op-amp and current DAC was designed to tune the DC offset. It eliminated the need for external power supply, and the calibration process was done automatically. However, it still requires software reconfiguration. None of those solutions can precisely predict the input DC offset and find the proper setting

to cancel the offset precisely. Another problem of all the solutions that involve software is that, it requires ADC and DAC to interact between the analog and digital world. The quantization noise from the ADC, and mismatch from the DAC elements will limit the system resolution.

In this paper, an analog DC offset calibration circuit is proposed for DC-coupled biomedical radar sensor. The analog calibration algorithm can precisely extract the input signal DC offset in a continuous fashion, and automatically remove the offset before sending the signal to baseband VGA. It requires only basic analog components: resistors, capacitors, switches, and op-amps which does not require any digital signal processing or software configuration. There is no quantization noise in analog systems. Hence, the resolution of the proposed analog DC offset calibration circuit is inherently higher than the aforementioned digitized solutions. The resolution of the proposed architecture is only limited by the offset of the resistors and op-amps, which can be well controlled based on mature circuit techniques. Furthermore, since the input is DC-coupled, it can be easily configured into a high precision mode that permits precise recording of the target displacement.

The detailed design of Doppler radar sensor and analog DC offset calibration circuit will be discussed in the next section. Section III will cover measurement results of proposed calibration architecture and experiment of vital signs sensing with the entire radar system. Conclusions are made in the last section.

## II. DESIGN OF DOPPLER RADAR AND ANALOG DC OFFSET CALIBRATION CIRCUIT

In this section, the basic operation theory of Doppler radar sensor system with a homodyne receiver will be reviewed first. Followed by detailed discussion about proposed analog DC offset calibration circuit.

### A. Basic Theory and Architecture of Dopper Radar Sensor

The diagram of a Doppler radar sensor system is shown in Fig. 1. A voltage controlled oscillator (VCO) is used to generate a pure sinusoidal wave at radio frequency (RF)  $f$ . Then the RF signal will be amplified and radiated out through a transmitter antenna. The transmitted signal is noted as  $T(t)$ , and  $\phi(t)$  is the phase noise

$$T(t) = \cos(2\pi ft + \Phi(t)) \quad (1)$$

When the transmitted signal reaches the target, it will be reflected with certain attenuation and phase shift depending on the target surface condition. Then the reflected signal will be picked up by the receiver antenna with a time delay. Assuming the target is  $d_0$  meters away from the radar with displacement  $x(t)$  on top of it. Ignoring amplitude modulation and other secondary effects, the received signal  $R(t)$  can be written as

$$R(t) = \cos(2\pi ft - \frac{4\pi x(t)}{\lambda} + \Phi(t) - \frac{2x(t)}{c} + \theta) \quad (2)$$

where  $\theta$  is a phase shift related to the distance  $d_0$ . The RF signal  $R(t)$  is then down-converted to baseband signal  $I(t)$  and  $Q(t)$  by mixing  $R(t)$  with  $T(t)$  and a 90-degree phase-shifted

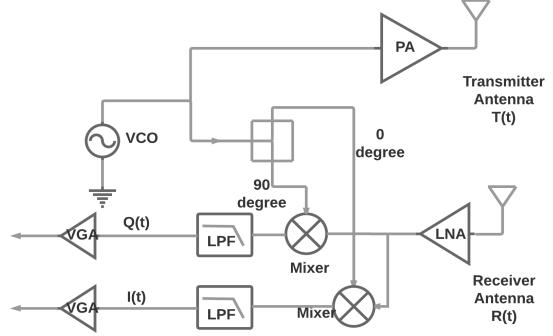


Fig. 1. Doppler radar sensor system diagram.

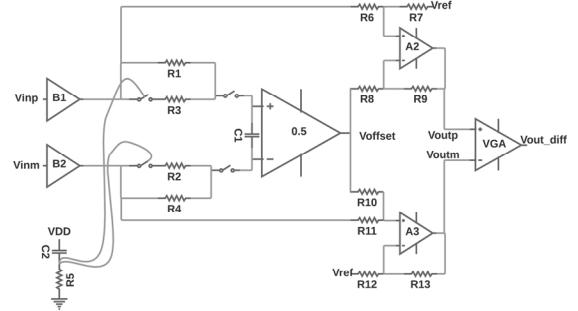


Fig. 2. Proposed analog DC offset calibration circuit diagram.

version of  $T(t)$ , respectively. Therefore, the baseband outputs can be represented as:

$$I(t) = A_I \cos\left(\frac{4\pi x(t)}{\lambda} + \Phi(t) - \Phi(t - \frac{2x(t)}{c}) - \theta + DC_I\right) \quad (3)$$

$$Q(t) = A_Q \cos\left(\frac{4\pi x(t)}{\lambda} + \Phi(t) - \Phi(t - \frac{2x(t)}{c}) - \theta + DC_Q\right) \quad (4)$$

where  $DC_I$  and  $DC_Q$  are the DC offsets caused by hardware imperfection and clutter reflection. The phase noise error term can be ignored in short-range applications according to the range correlation theory [10]. Then  $I(t)$  and  $Q(t)$  will be sent to VGA for amplification. If the DC offset is too large, it will saturate the baseband VGA and cause system failure.

Finally, the  $I$  and  $Q$  channel outputs from the VGA will be sent into an analog to digital converter (ADC). Then, the digitized data will be stored for post processing [11]. In this design, the analog output is sampled by NI USB-6009 which has multiple 14-bit ADCs.

### B. Proposed Analog DC Offset Calibration Circuit

Fig. 2 shows the diagram of the proposed analog DC offset calibration circuit. The input  $Vinp$  and  $Vinm$  shown in the diagram are the differential output of the receiver front-end. Unit gain buffers B1 and B2 are used right after the input to prevent any loading effect that may affect the performance of the preceding circuit. A differential RC low-pass filter (LPF) formed by R1, R4 and C1 is used to extract the DC offset information

from the input  $V_{inp}$  and  $V_{inm}$ . The differential output of the LPF is equal to the DC difference of the two inputs. There are two reasons to choose differential LPF versus single-ended LPF. First, the differential LPF only responds to differential input signal, and thus eliminates the need to charge the LPF holding capacitor C1 in case of common mode jump. Second, differential LPF can save one capacitor and provide twice the cut-off frequency. The cut-off frequency of the LPF needs to be much smaller than the smallest signal frequency of interest. In case of vital sign detection, the frequency of interest could be as low as 0.1 Hz. Therefore, the cut-off frequency needs to be as small as possible for the best filtering performance. Since the time constant of a RC filter is inversely proportional to the cut-off frequency, the problem for using such low cut-off frequency is that it takes a long time for the system to settle and start working properly. The system will not reach its optimal operating point until 10 times the time constant after powering up.

To solve this problem, a fast-charging circuit is proposed to charge the LPF holding capacitor C1 faster during power up. The fast-charging circuit consists of a RC high-pass filter (HPF) which senses the supply jump and a switch which controls the fast charging path. The HPF is formed by capacitor C2 and resistor R5. When the system is powered off, the supply is 0 V, and the voltage on capacitor C2 is also 0 V. This is guaranteed by the design of power-on switch. When the system is powered off, the supply is shorted to ground. During power up, the HPF senses the supply jump from 0 V to VDD. Since the voltage on the capacitor C2 cannot jump abruptly, the output of the HPF must jump to VDD immediately. The switch is turned on and let the buffer charge the LPF C1 directly. Then capacitor C2 will slowly be charged up through the resistor R5. In the end, the voltage on capacitor C2 will be equal to VDD, and the switch will be turned off automatically. The time constant of this HPF decides how long the switch will be on.

However, shorting capacitor C1 to the buffer directly introduces another problem. Because the capacitance of C1 is very large, it will cause stability problem for normal buffers. If the buffer starts ringing or oscillating, the final voltage on capacitor C1 will be unknown depending on when the switch is turned off. There are buffers that can handle this kind of large capacitance, and usually they are very expensive. To reduce the design cost, small series resistors R2 and R3 are intentionally added between the buffer and capacitor C1. They will introduce a pole-zero pair that cancels each other at high frequency. Hence, the stability of the buffer is improved and ringing is prevented.

Ideally, after the fast-charging switch is turned off, the voltage on the capacitor C1 should be equal to the DC difference of the input signals. Because input signals also carry AC signals, there will be small error. Then the LPF filter will kick in and start to filter out the AC signals. In the end, the differential output of LPF should equal to the DC difference of  $V_{inp}$  and  $V_{inm}$  eventually, assuming the cut-off frequency is low enough to filter out the AC signal completely.

The differential output of the LPF is connected to an instrumentation amplifier A1 which has a gain of 0.5. An instrumentation amplifier is necessary to provide high input impedance, since the LPF does not have strong driving capability. The output of A1 is  $V_{offset}$ ,

$$V_{offset} = 0.5 * (V_{inp\_dc} - V_{inm\_dc}) + V_{ref} \quad (5)$$

where  $V_{inp\_dc}$  and  $V_{inm\_dc}$  is the DC value of the input signals, and  $V_{ref}$  is the common mode bias of the system. As can be seen,  $V_{offset}$  equals precisely to the amount that the input signals need to be adjusted for.

Then, two more op-amps A2 and A3 are used as adder and subtractor to adjust  $V_{inp}$  and  $V_{inm}$  separately. Both the op-amps are configured with gain equals to one. The positive input of op-amp A2 is connected to  $V_{inp}$  and its negative input is connected to  $V_{offset}$ . The output of A2 is named as  $V_{outp}$ . The positive input of op-amp A3 is connected to  $V_{inm}$ , and negative input is connected to  $V_{ref}$ . Note that the reference point of op-amp A3 needs to be connected to  $V_{offset}$ . The output of A3 is named as  $V_{outm}$ .

$$V_{outp} = V_{inp} - 0.5 * (V_{inp\_dc} - V_{inm\_dc}) \quad (6)$$

$$V_{outm} = V_{inm} + 0.5 * (V_{inp\_dc} - V_{inm\_dc}) \quad (7)$$

It is shown that the final output of the proposed analog calibration circuit is exactly the input minus the DC offset. After calibration, the VGA should see the input without DC offset and its dynamic range can thus be maximized.

It should be noticed that the proposed circuit tracks the input DC offset in real time, and the offset is automatically removed by the circuit. As a result, if the input signal itself has DC components, it will also be removed from the final output  $V_{outp}$  and  $V_{outm}$  automatically. There are two solutions to solve this problem. Since the entire system is DC-coupled, the circuit can be easily reconfigured to pass through input signal DC changes. In applications that require precise displacement information, the LPF can be connected or disconnected in a controlled manner. After the LPF is settled, we can disconnect the LPF, and let the holding capacitor C1 hold the voltage. In this mode, the circuit can remember the hardware DC offset and the clutter reflection DC offset from the previous moment. The undesired offset will still be removed, while the change in input signal DC can pass through the calibration circuit. In the other solution, the LPF can be kept on, and the distorted signal can be compensated. The input signal DC information is removed from the final output, but it is not lost. Comparing equation (5)-(7) reveals that the final output distorted part is the same as  $V_{offset}$  held on the capacitor C1. By combining them together, the actual precise input signal can be reconstructed.

### III. EXPERIMENT SETUP AND MEASUREMENT RESULTS

To demonstrate the functionality and characterize the performance of the proposed analog DC offset calibration circuit for biomedical radar sensor, several experiments were carried out on a PCB prototype. First, a detailed DC sweep was performed to find out the DC operational range of the circuit and the achievable resolution. In the second experiment, an AC signal was added on top of the DC to mimic the real situation. It demonstrated that after DC offset was removed, the VGA gain can be increased to achieve the maximum dynamic range. In the end, the proposed analog DC calibration circuit was connected to the output of a real DC-coupled Doppler radar sensor front-end and the system demonstrated the capability of detecting vital

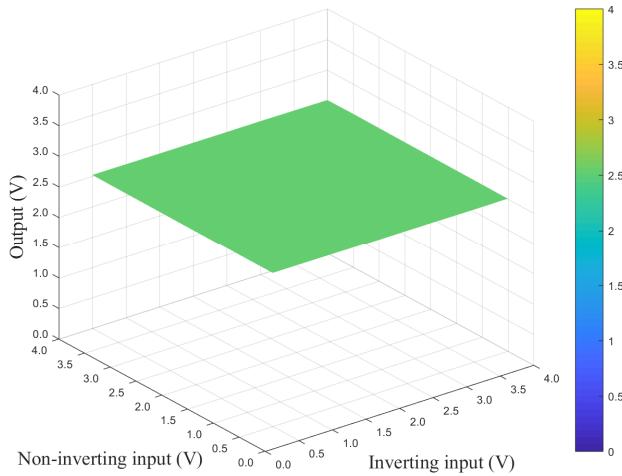


Fig. 3. DC characteristic of presented architecture

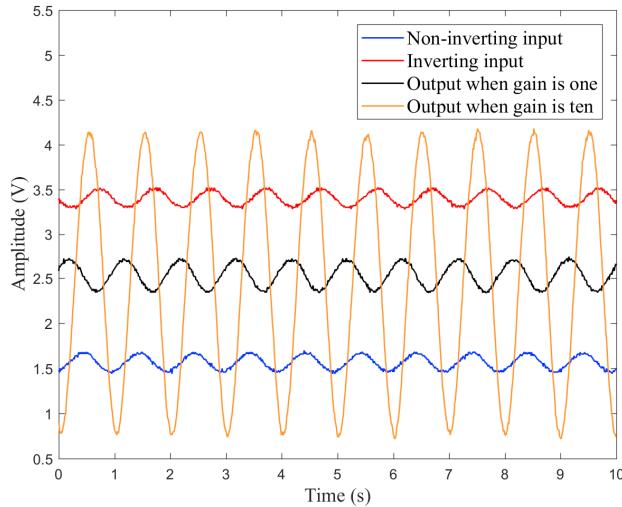


Fig. 4. Analog DC offset cancellation circuit Diagram

signals. The calibration circuit shared the same supply as the Doppler radar sensor front-end, which operates between GND and 5V supply.

#### A. DC Characteristics

To demonstrate the proposed analog DC offset calibration circuit is robust with different input DC levels,  $V_{inp}$  and  $V_{inm}$  were connected to two different DC voltage sources. Both voltage sources were swept independently to cover all the possible combinations, and the output of VGA  $V_{out\_diff}$  was measured. A 3D surface plot of the measurement result was given in Fig. 3 for easy visualization. The X-axis is  $V_{inp}$ , the Y-axis is  $V_{inm}$ , and the Z-axis is  $V_{out\_diff}$ . As can be seen, the surface is almost flat. For a wide range of input DC levels, the final VGA output is always very close to 2.5 V, which is the designed common mode signal level. It demonstrated the robustness of the proposed architecture over a wide input range, while maintaining a high resolution. The resolution was measured by the residue DC offset after calibration.

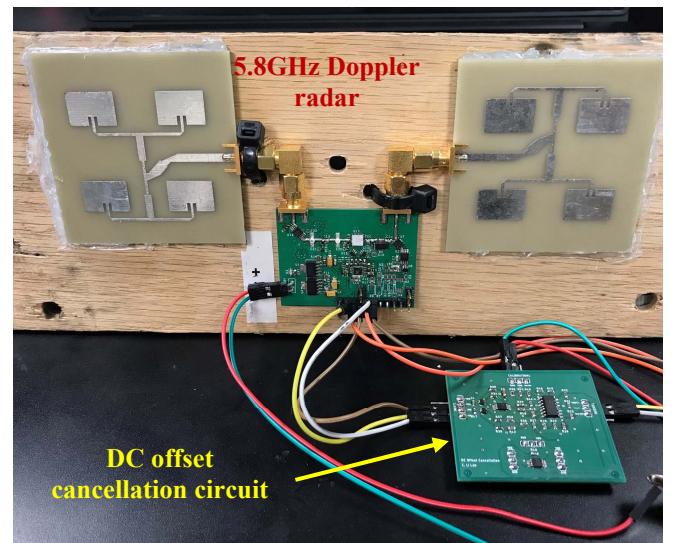


Fig. 5. Vital sign monitoring experiment setup.

#### B. Dynamic Range Improvement

The real baseband input is always DC plus AC. Since it is difficult to precisely control the signal level of the output of a real Doppler radar sensor receiver front-end, signal generators were used to mimic the differential outputs of a radar receiver front-end and connected to  $V_{inp}$  and  $V_{inm}$  directly in this experiment. It gives better control of the input signal levels, such that the proposed architecture can be characterized in detail. Fig. 4 is one of the results that represents a tough environment in real situation. The total DC offset is 2V in this case, and the differential AC signal is about 340-mV peak to peak. The 340 mV AC is chosen so that the oscilloscope can capture it clearly. Without DC offset calibration, the VGA gain is limited to the minimal setting 1 by its DC offset. The experiment result shows that, the proposed circuit is immune to the DC input offset, and the VGA gain can be increased by 10 times. Hence the dynamic range of the system can be maximized. In real world applications, the input AC amplitude can be much smaller, and the VGA gain can be set to a higher value.

#### C. Vital Signs Detection

To further demonstrate the functionality of the proposed DC calibration circuit in practical applications. A remote sensing of human vital signs experiment was conducted in a typical lab environment using a 5.8 GHz Doppler radar with the utilization of the DC calibration circuit. System setup is shown in Fig. 5. Since the full radar system with differential  $I/Q$  channels is still under development, only single-ended  $I/Q$  channels are tested in this work. Therefore, single-ended  $I/Q$  channel signals from the 5.8-GHz Doppler radar were used to connect to the two differential inputs of the DC calibration circuit. Instead of analyzing the output of the VGA,  $V_{outp}$  and  $V_{outm}$  are of interest because two inputs are both single-ended.

In the experiment, a seated human subject was 1.5 m in front of the radar. Both the original  $I/Q$  signals from the radar directly and the DC calibrated  $I/Q$  signals after the offset calibration

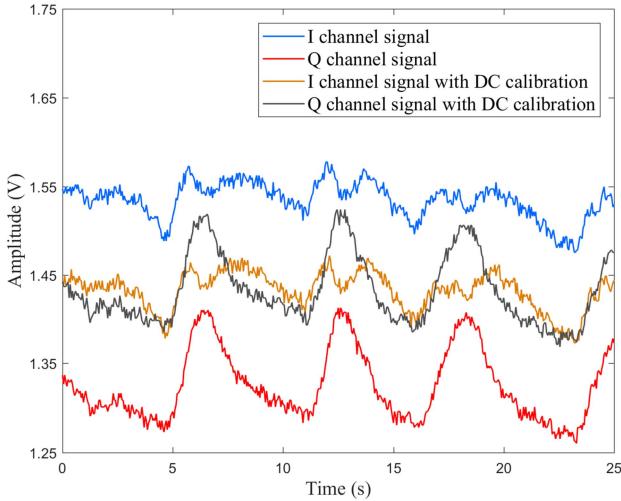


Fig. 6. Recorded *I/Q* channel signals with and without DC offset calibration.

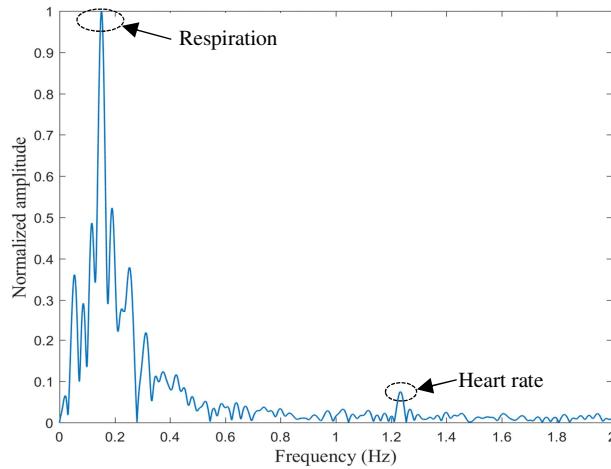


Fig. 7. Vital signs measured by 5.8G Radar sensor with the use of proposed DC offset calibration circuit.

circuit were sampled through an NI UAB-6009 acquisition unit. The measurement results are presented in Fig. 6. It clearly shows that there is around 0.2 V DC difference between the original *I/Q* signals. The difference is removed after the DC calibration circuit, so that they have the same DC level at the circuit output and the overall dynamic range is successfully increased. However, the dynamic range is not maximized for single-ended input. If we observe VGA output  $V_{out\_diff}$ , the common mode is fixed at 2.5 V, which is the VDD/2, and the dynamic range can be maximized for differential input signals.

Fast Fourier transform (FFT) was applied to the complex signal combined from the *I/Q* channels with DC offset calibration. Respiration rate of around 0.2 Hz and heart rate of about 1.23 Hz can be identified clearly in the FFT frequency spectrum in Fig. 7, which corresponds to 12 breaths and 74 heart beats per minutes, respectively.

#### IV. CONCLUSION

In this paper, an analog DC offset background calibration circuit is proposed to solve the DC offset issue in DC-coupled Doppler radar sensor with a homodyne architecture. The PCB prototype is tested with an existing DC-coupled Doppler radar sensor. Experiments demonstrate that the proposed circuit can automatically correct a wide range of DC offset with high accuracy, without requiring any software programming. Therefore, an improved dynamic range can be achieved. Vital signs sensing is also demonstrated with a human subject in a lab environment. It successfully demonstrated the functionality of the proposed analog DC offset calibration circuit.

#### ACKNOWLEDGMENT

The authors would like to acknowledge grant support from National Science Foundation (NSF) CNS-1718483 and ECCS-1254838.

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