A 0.3-0.86V Fully Integrated Buck Regulator with 2GHz Resonant Switching for Ultra-Low Power Applications

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Abstract

A fully integrated buck regulator for ultra-low voltage application is presented featuring (1) an ultra-high switching frequency at 2GHz with small inductor size at low load current and (2) a resonant switching technique rendering significant efficiency improvement. With small on-chip inductors, the test chip shows a wide voltage tuning range of 0.3-0.86V, at 10-40mA low current, up to 73% efficiency and only occupies 0.073mm^2 in a 65nm CMOS process.

Introduction

Ultra-low voltage operation from near or sub-threshold computing poses significant challenges for fully integrated on-chip regulators due to the low load current. Conventional buck converters are normally designed with off-chip inductors [1-2] or on-chip inductors with high load current at several hundred mA [3-5]. Based on the fundamental equation of step-down voltage $\Delta V = L \cdot \frac{\partial i}{\partial t} \propto L \cdot f_{sw} \cdot I_{out}$, at a current condition of only tens of mA, orders of magnitude larger inductor is needed. Fig. 1(a) shows the relationship between load current, $f_{sw}$and inductor values [3-5]. To enable the use of small on-chip inductor, this work presents a design with a switching frequency f_{sw} of 2GHz, which is the highest switching frequency reported so far, or 4X of that reported in [5]. As a high switching frequency f_{sw} inevitably causes high switching power loss, a special resonant switching technique is presented to reduce switching power consumption. As shown in Fig. 1(b), a resonant network is formed between the main switches and a resonant inductor, providing significant saving of switching power. Fig. 1(c) shows the simulation results on switching power contribution as well as efficiency improvement with and without resonant switching. An 8~21% efficiency improvement is observed using the resonant switching at low voltages from 0.3V to 0.8V.

Proposed Design

The overall scheme of the proposed buck regulator is shown in Fig. 2. Different from conventional design, to utilize resonant switching, the PMOS and NMOS power switches are jointly switched through a resonant network where a resonant inductor L_2 resonates with the switches' gate capacitance $C_{gate,p}$ and $C_{gate,n}$. Capacitor C_{gnd} is used to provide a self-biasing AC ground with a value of 30pF [6]. The degradation of slew rate from resonant operation leads to large short circuit current and switch conduction power loss. To suppress the short circuit current, NMOS switch is AC coupled and biased at low voltage near its threshold voltage. To recover slew rate, the switching voltage V_{sw} is generated by a special digital tunable slew rate control block as shown in Fig. 3. The control of slew rate is done separately by V_p and V_n by adjusting the timing of clock driver M_{P2} and M_{N2} through the tunable capacitors $C_{n,array}$ and $C_{p,array}$, respectively. Since recovery on slew rate requires extra clock power, a careful design tradeoff needs to be played. In this work, V_{sw} is tuned with fast rising slew rate to reduce high conduction loss through M_{P1} and M_{N1} due to high current flow at rising transition and is tuned with slow falling slew rate to retain resonant energy saving. Fig. 4 shows a digital duty cycle control block which adjusts duty cycle of V_{sw} for different output voltage/current. The duty cycle control is done through a feedback loop at 250MHz. The comparison results of V_{out} and V_{ref} issues digital control signals to a R-2R DAC which changes the trip voltages of digital buffers providing adjustment of the duty cycle between 18% and 84%. The main inductance L_1 is 3nH and the resonant inductance L_2 is 8.2nH with similar size and smaller Q factor.

The power loss breakdown of the proposed regulator is analyzed in Fig. 5. An optimal f_{sw} is observed at the balance of switch conduction loss (increase with f_{sw}) and inductor loss (decrease with f_{sw}). Because L_1 carries >10X more current than L_2 and resides in a close vicinity, the mutual coupling effects are studied to avoid noise injection into switching transistors. EM simulation in Fig.6 shows 20MHz resonant frequency shift due to mutual inductance and the overall coupling from L_1 to L_2 is less than -40dB.

Measurement Results

The proposed regulator is fabricated in 65nm CMOS process with 1.1V input voltage. Fig. 7 shows the test chip configurations, which also include a digital logic load circuit that can operate under dynamic frequency scaling (DFS). Fig. 8 shows transient voltage measurement probed at output pin. Under static loading, a 32mV ripple at 2GHz is observed. The loop dynamic shows a response speed of 5ns for small voltage change of 40mV. Multiple loop clock cycles are needed for settling larger voltage change, e.g. 100mV. Under instantaneous large load I_{out} transient, an undershoot/ overshoot of ~80mV is observed which can be mitigated by using larger decoupling capacitors. Digital logics were activated with a dynamic frequency scaling from 140MHz to 200MHz. A slightly larger dynamic ripple of ~50mV was observed at digital clock frequency. Fig. 9 shows the measured efficiency. At 0.6V, an efficiency of 65% was observed similar to [7]. A wide voltage range from 0.3V to 0.86V is achieved with efficiency up to 73%. An optimal frequency is observed at 1.9G~2.0G matching simulation expectation in Fig. 5. Fig. 10 shows the die photo. The overall regulator area is 0.073 mm^2, with 91% area occupied by inductors at top metal. Table 1 compares the design with prior works. Compared with previous switched cap (SC) design in 22nm with similar low power specification [7], the proposed design achieves 30% less area, wider output range and similar efficiency performance in a 65nm process.

Acknowledgement

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References

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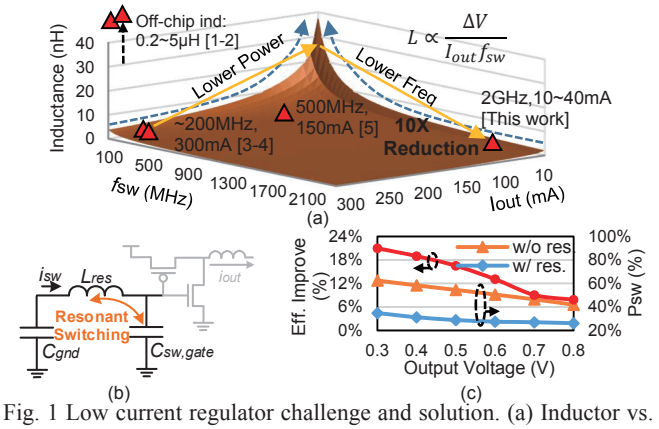


Fig. 1 Low current regulator challenge and solution. (a) Inductor vs. frequency and load current for buck regulator; (b) Resonant switching concept; (c) Efficiency improvement from resonant switching.

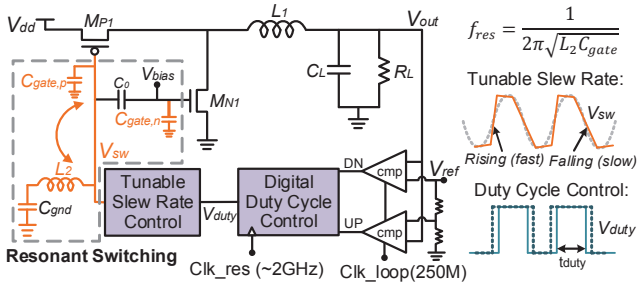


Fig. 2 Overall scheme of the proposed buck regulator with resonant switching scheme.

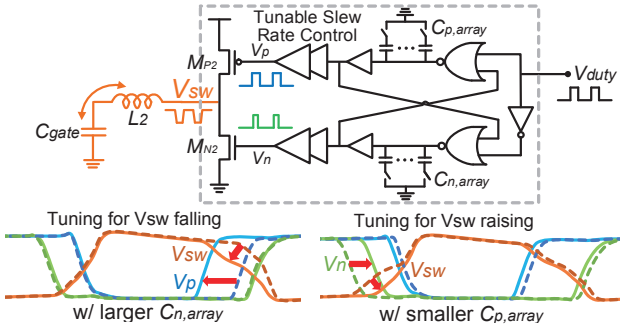


Fig. 3 Tunable slew rate control block and its tuning strategy for the clock rising and falling slew rate.

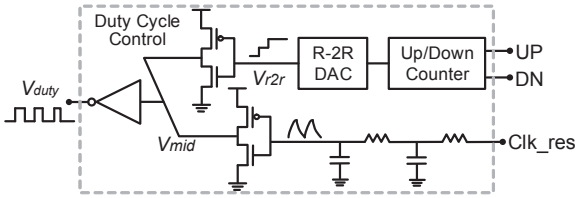
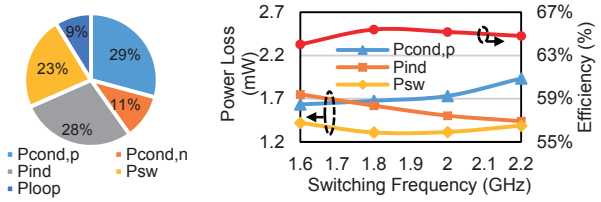


Fig. 4 Digital duty cycle control block.



Power Loss Analysis:

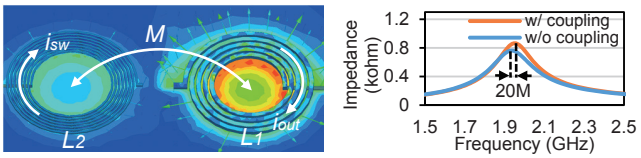
$$P_{Loss} = P_{cond,p/n} + P_{ind} + P_{sw} + P_{loop}$$

$$P_{cond,p/n} = I_{ds}^2 R_{on} + \int_0^{t_{transition}} i_{ds} v_{ds} dt \cdot f_{sw} \quad \propto \quad f_{sw} \text{ , (for } M_{P1} \text{ \& } M_{N1})$$

$$P_{ind} = I_{out}^2 R_{ind} = (\Delta V / 4 L f_{sw})^2 R_{ind} \quad \propto \quad 1/f_{sw}^2 \text{ , (for Inductor } L_1)$$

$$P_{sw} = \alpha \frac{\pi}{4Q} C_{gate} V_{dd}^2 \cdot f_{sw} + P_{clk} \quad \propto \quad f_{sw} \text{ , (for } C_{gate} \text{ and clock power)}$$

Fig. 5 Simulation of power loss breakdown at V_{out}=0.6V and power loss model versus switching frequency f_{sw}.



$$L_{eff,1} = L_1 + M \frac{\partial i_{sw}/\partial t}{\partial i_{out}/\partial t} \approx L_1 \quad L_{eff,2} = L_2 + M \frac{\partial i_{out}/\partial t}{\partial i_{sw}/\partial t} \quad i_{out} \gg i_{sw}$$

Fig. 6 Simulation on inductor mutual coupling.

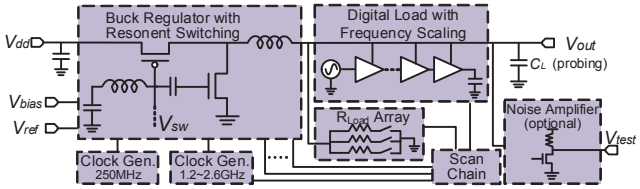


Fig. 7 Test chip diagram.

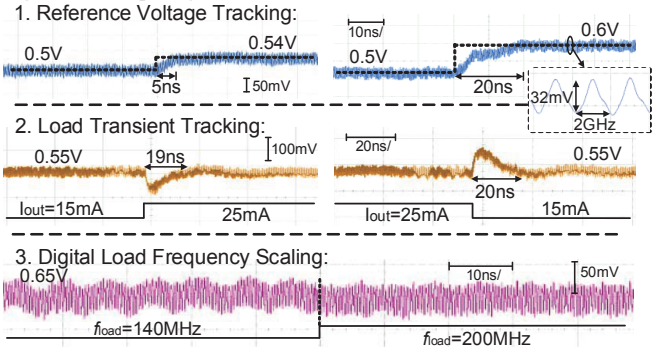


Fig. 8 Regulator output voltage tracking and ripple measurement.

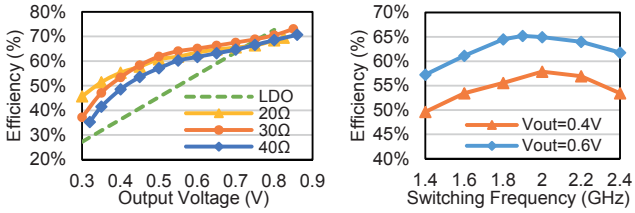


Fig. 9 Regulator efficiency measurement.

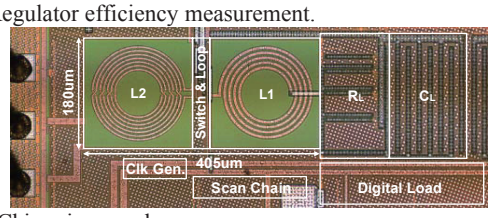


Fig. 10 Chip micrograph.

TABLE I. PERFORMACE SUMMARY AND COMPARSION

	[3]	[4]	[5]	[7]	This work
Topology	Buck	Buck	Buck	SC	Buck
Inductor/ Capacitor	on-chip spiral	on-chip spiral	on-chip spiral	MIM cap	on-chip spiral
Process (nm)	130	130	22	22	65
Fsw (MHz)	170	50-250	500	250	2000
Iout (mA)	350	250	150	10-88	10-40
L (nH)	2	4	1.5	--	3
C_L (nF)	5.2	10	5	0.1	0.12
Vin (V)	1.2	2.4	1.5	1.23	1.1
Vout (V)	0.9	0.4-1.4	0.4~1.2	0.45-0.85 (SC)	0.3-0.86
Ripple (mV)	40	>50	8	43	32
Response (ns)	--	20	52	3-5	5
Peak Eff. (%)	77.9	77	70	~73 (SC)	73
Eff. at 0.6V (%)	~60	~50	~45	~65	65
Area (mm^2)	1.5	5	1.5	0.103	0.073