Hardware-Efficient Logic Camouflaging for Monolithic 3D ICs

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***Abstract*—Circuit camouflaging is a layout-level technique to thwart image analysis based reverse engineering attacks. An efficient dummy contact based camouflaging method for monolithic three-dimensional (3D) integrated circuits (ICs) is proposed. 3D ICs achieve ultra-high density device integration enabled by fine-grained monolithic inter-tier vias (MIVs). Standard cell libraries are developed to evaluate the effects of circuit camouflaging on large-scale 2D and monolithic 3D ICs. These libraries are used to design a camouflaged SIMON (lightweight block cipher) and several academic benchmarks. Simulation results demonstrate that the monolithic 3D technology is highly effective to facilitate the utilization of camouflaging technique against reverse engineering attacks. At the expense of a slight degradation in timing characteristics, monolithic 3D technology eliminates not only the area, but also the power overhead related to camouflaging.**

***Index Terms*—Hardware security, circuit camouflaging, reverse engineering, monolithic 3D integration, 3D cell library.**

I. Introduction

The security of integrated circuits (ICs) has emerged as a fundamental issue due to the threats from the globalized semiconductor supply chain. Circuit camouflaging is an effective technique to thwart reverse engineering attacks that try to recover the original netlist through scanning electron microscopy (SEM) images [1]–[4]. The circuit obfuscation level achieved by the camouflaging technique, however, depends upon the number and location of the camouflaged gates [2]. Thus, these parameters play an important role in achieving the desired attack resilience. A larger number of camouflaged gates strengthens the countermeasure at the expense of significant overhead in area, power, and delay characteristics [2].

Recently, monolithic 3D technology [5]–[7] has been conceptually proposed as a countermeasure against reverse engineering since it has the potential to reduce the overhead of traditional circuit camouflaging [8]. Transistor-level camouflaged logic locking method for monolithic 3D IC security has also been proposed [9]. These studies follow the highly encouraging recent developments on monolithic 3D technology that relies on sequentially fabricating multiple transistor layers [10]. Monolithic 3D ICs not only enable ultra-high density device integration, but also introduce novel opportunities and challenges on managing hardware security [8], [9], [11], [12]. For example, existing split manufacturing techniques developed primarily for through silicon via (TSV) and interposed based vertical integration are not applicable to monolithic 3D ICs. Unlike TSV based 3D ICs, in monolithic 3D ICs, all of the tiers are manufactured sequentially by the same foundry, as depicted in Fig. 1. Thus, splitting the system functionality into multiple tiers is not effective to protect monolithic 3D ICs from reverse engineering and hardware intellectual property (IP) piracy attacks from untrusted foundries.

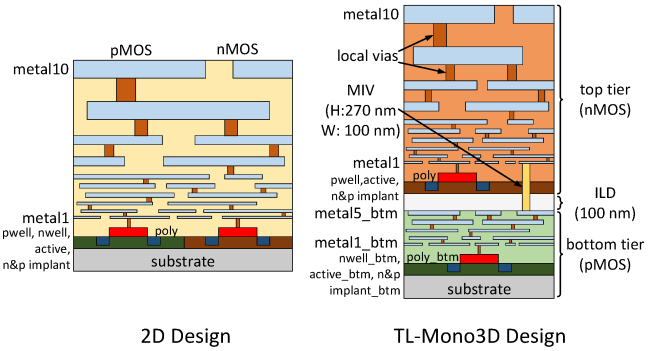

Fig. 1. **Cross-sections of the conventional 2D and transistor-level monolithic (TL-Mono) 3D technology with two tiers. The top tier hosts the nMOS transistors whereas the pMOS transistors are placed within the bottom tier.**

In this paper, an efficient logic camouflaging method for monolithic 3D ICs is presented. Full custom cell libraries are developed and fully characterized to camouflage large-scale 2D and 3D circuits. The area, power, and timing overhead of circuit camouflaging is evaluated both at the cell- and chip-levels. The opportunities for chip security enhancement provided by monolithic 3D technology are quantified.

The rest of the paper is organized as follows. A brief background and contributions of this work are summarized in Section II. Proposed camouflaged 2D and monolithic 3D IC cell libraries are provided in Section III. Simulation results for SIMON block cipher and several academic benchmarks are presented in Section IV. The paper is concluded in Section V.

II. Background and Contributions

A. Circuit Camouflaging

Circuit camouflaging is a method to obfuscate logic function by making subtle changes to the physical layout of standard cells [1]–[3]. The primary goal of camouflaging is to disguise the circuit against a reverse engineer who utilizes SEM pictures to recover the original chip design. For example, from the SEM image analysis, a camouflaged logic cell appears to be a 2-input NAND gate. In practice, however, that cell

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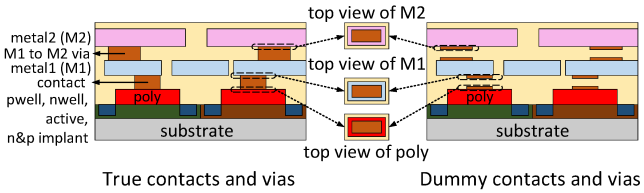

Fig. 2. **Illustration of true and dummy contacts/vias.**

TABLE I
LIST OF STANDARD CELLS IN THE CAMOUFLAGED 2D AND MONOLITHIC 3D LIBRARIES.

Regular Standard Cells		Camouflaged Standard Cells
INVX1	INVX2	NAND2X1 & NOR2X1
CLKBUF1	CLKBUF2	AND2X1 & OR2X1
DFFPOSX1	FILL	XNOR2X1 & XOR2X1

can be a 2-input NOR gate. This wrong perception can be achieved by small changes on metal contacts and vias [13]. As shown in Fig. 2, the contacts between metal 1 (M1) and the polysilicon layers are physically connected on the left cell, but disconnected after a thin layer of contact material on the right cell. The top views of M1 (and polysilicon) for the gates with or without camouflaging are identical. Same technique can be applied to vias between metal layers. As demonstrated in [1], the conventional and camouflaged 2-input AND gates have exactly the same SEM image. Thus, an attacker cannot entirely rely on SEM image analysis to successfully extract the correct circuit netlist. Since reverse engineers cannot partially etch a layer [4], circuit camouflaging with dummy contacts/vias has become an effective method to obscure the original circuit.

B. Contributions of This Paper

The primary contributions of this paper are as follows:

- Camouflaged monolithic 3D cells are developed and fully characterized by using cell stacking method.
- Chip-level analysis is performed on fully placed and routed 2D and monolithic 3D circuits to quantify and compare the area, power, and delay overhead of camouflaging technique. An important observation is that the cell-level power overhead (that is typically reported in existing work) is compensated by the reduction in chip-level interconnect power for monolithic 3D technology.
- Advantages and limitations of circuit camouflaging for 3D monolithic technology are discussed. To the best of the authors' knowledge, this study is the first work that quantitatively investigates the overhead of circuit camouflaging on monolithic 3D ICs.

III. LOGIC CAMOUFLAGING FOR MONOLITHIC 3D ICS

A. Camouflaged Cells in 2D and Monolithic 3D Technologies

Two camouflaged standard cell libraries are developed. The first one is for conventional 2D technology whereas the second one is for monolithic 3D technology with inter-tier vias. Both of these libraries are generated based on the 2D 45 nm process design kit *FreePDK45* [14]. Thus, the process and physical characteristics such as transistor models and on-chip metal layers are obtained from *FreePDK45*.

As shown in Fig. 1, in the transistor-level 3D monolithic technology, there are two tiers where the top tier is used for

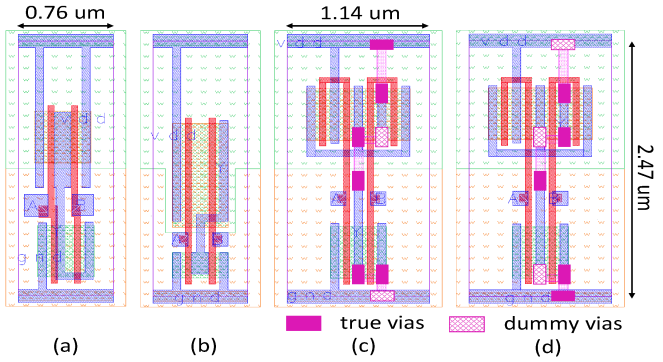

Fig. 3. **Standard cell layouts in 2D technology: (a) conventional NAND, (b) conventional NOR, (c) camouflaged NAND, and (d) camouflaged NOR.**

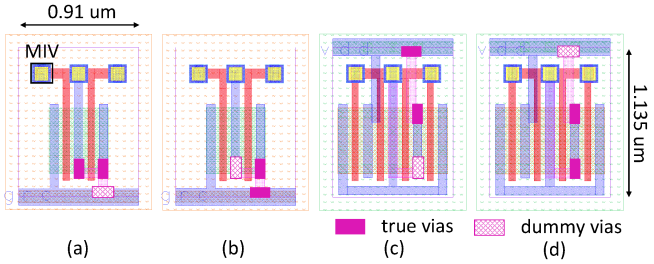

Fig. 4. **Camouflaged cell layouts in monolithic 3D technology: (a) top tier of NAND gate, (b) top tier of NOR gate, (c) bottom tier of NAND gate, (d) bottom tier of NOR gate.**

nMOS transistors whereas the pMOS transistors are placed within the bottom tier, similar to [15]. The top tier is separated from the bottom tier with an inter-layer dielectric (ILD) with a thickness of 100 nm. The 10 metal layers that originally exist in 2D *FreePDK45* and camouflaged 2D cell library remain the same for the top tier in camouflaged monolithic 3D technology. Alternatively, the bottom tier metal layers of the 3D technology are primarily for intra-cell routing. The intra-cell connections that span the two tiers are achieved by monolithic inter-tier vias (MIVs). Each MIV has a width of 100 nm and height of 270 nm [16].

Twelve standard cells are developed in both 2D and 3D camouflaged cell libraries, as listed in Table I. Of these cells, NAND, NOR, AND, OR, XOR, and XNOR are camouflaged. For example, NAND and NOR cells are designed to look identical where the actual function depends upon the real and dummy contacts. This behavior also holds for AND/OR and XOR/XNOR cell pairs. The camouflaged 2D NAND and NOR gates with both dummy and real contacts/vias are shown, respectively, in Figs. 3(c) and (d). As a reference, the non-camouflaged NAND and NOR gates are also illustrated in Figs. 3(a) and (b), respectively.

In camouflaged monolithic 3D cells, the power rail is located at the top of the bottom tier and the ground rail is located at the bottom of the top tier. MIVs are distributed within the cell to minimize the interconnect distance and reduce the cell height, as shown in Fig. 4, where the camouflaged 3D NAND and NOR gates are illustrated. Both the top [see Figs. 4(a) and b)] and bottom tiers [see Figs. 4(c) and d)] in each cell look identical from top view.

In camouflaged 3D cells, the cell height is 1.135 μm, which is 54% smaller than the standard cell height (2.47 μm shown

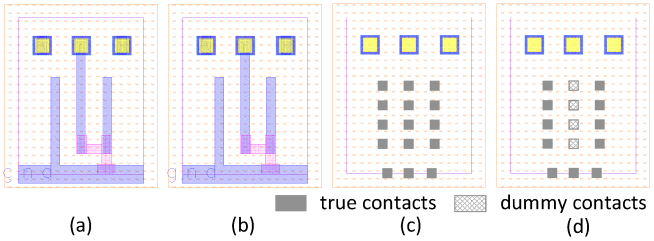

Fig. 5. **Metal layers and true/dummy contacts within the top tier of camouflaged monolithic 3D cells: (a) NAND metal layers, (b) NOR metal layers, (c) NAND contacts, (d) NOR contacts.**

TABLE II
AREA, AVERAGE DELAY AND POWER CHARACTERISTICS OF CONVENTIONAL 2D, CAMOUFLAGED 2D (2D_C), MONOLITHIC 3D, AND CAMOUFLAGED MONOLITHIC 3D (3D_C) STANDARD CELLS. ALL OF THE PERCENTAGES ARE WITH RESPECT TO CONVENTIONAL 2D RESULTS.

Std Cell	Design	Area (μm^2)	Delay (ps)	Power (μW)
NAND_2D	2D	1.88	7.61	1.28
	2D_C	2.82 (**50%**)	8.93 (**17%**)	1.82 (**42%**)
NAND_3D	3D	0.6 (**-68%**)	8.95 (**18%**)	1.45 (**13%**)
	3D_C	1.04 (**-45%**)	10.3 (**35%**)	1.97 (**54%**)
NOR_2D	2D	1.88	8.73	1.41
	2D_C	2.82 (**50%**)	8.05 (**-8%**)	1.80 (**28%**)
NOR_3D	3D	1.04 (**-45%**)	9.05 (**4%**)	1.42 (**1%**)
	3D_C	1.04 (**-45%**)	8.22 (**-6%**)	1.82 (**29%**)
AND_2D	2D	2.87	14.2	2.28
	2D_C	3.66 (**28%**)	17.0 (**20%**)	2.98 (**31%**)
AND_3D	3D	1.27 (**-58%**)	15.3 (**8%**)	2.32 (**2%**)
	3D_C	1.42 (**-51%**)	18.1 (**27%**)	2.99 (**31%**)
OR_2D	2D	2.87	15.4	2.26
	2D_C	3.66 (**28%**)	15.6 (**1%**)	2.75 (**22%**)
OR_3D	3D	1.42 (**-51%**)	16.9 (**10%**)	2.35 (**4%**)
	3D_C	1.42 (**-51%**)	17.0 (**10%**)	2.76 (**22%**)
XNOR_2D	2D	4.67	29.6	9.82
	2D_C	4.67 (**0%**)	31.2 (**5%**)	10.3 (**5%**)
XNOR_3D	3D	3.10 (**-34%**)	31.4 (**6%**)	10.2 (**4%**)
	3D_C	3.10 (**-34%**)	32.9 (**11%**)	10.5 (**7%**)
XOR_2D	2D	4.67	29.3	10.1
	2D_C	4.67 (**0%**)	30.6 (**4%**)	10.5 (**4%**)
XOR_3D	3D	3.10 (**-34%**)	31.7 (**8%**)	10.4 (**3%**)
	3D_C	3.10 (**-34%**)	32.5 (**11%**)	10.7 (**6%**)

in Fig. 3) in *Nangate* 45 nm cell library [17]. The top tier metal layers and true/dummy contacts of these camouflaged cells are illustrated in Fig. 5 for both NAND and NOR cells. Note that contrary to non-camouflaged cells that utilize only metal 1 for intra-cell routing, camouflaged cells require both metal 1 and metal 2 for routing, which affects both the cell-level (see Section III-B) and chip-level (see Section IV) area, power and timing characteristics.

B. Cell-Level Evaluation

The effect of camouflaging on cell-level area, delay, and power consumption is investigated for both 2D and 3D technologies. The results are listed in Table II.

1) Footprint: For the 2D camouflaged cells, the increase in cell area varies from 0 to 50%, depending upon the cell type. For example, for XNOR and XOR gates, there is no overhead in area since the transistors in both cells have the same sizes. Thus, it is not necessary to upsize the cells to make them look identical. Furthermore, the inherent cell area is sufficiently large, leaving sufficient space for intra-cell routing needed for camouflaging the cells. For camouflaged monolithic 3D standard cells, the cell area is reduced as compared to non-camouflaged 2D cells due to the inherent advantage of monolithic 3D technology. This reduction in cell area varies from 34% to 51%. Despite more than 50% reduction in cell height, the average area reduction is less than 50% due to camouflaging overhead and MIVs. The area of the non-camouflaged 3D cells is also listed in the table as a reference.

2) Delay and Power Consumption: HSPICE simulations are performed on the extracted non-camouflaged 2D, 3D, and camouflaged 2D and 3D netlists to compare the cell-level power and delay characteristics at nominal operating conditions. Non-camouflaged 2D results are considered as the baseline for all of the percentages reported here. In general, the 2D camouflaged cells of this work have significantly less delay and power overhead as compared to [2]. As listed in Table II, for the 2D camouflaged cells, the percent change in average propagation delay varies from -8% (for the NOR gate) to 20% (for the AND gate), while for the monolithic 3D technology, it varies from -6% (for the NOR gate) to 38% (for the NAND gate). Thus, except the NOR gate, camouflaging increases the delay in both 2D and 3D technologies due to additional interconnects and vias. For the camouflaged NOR gate, the size of the nMOS has been increased from 0.25 μm to 0.5 μm (since the size of each nMOS in the NAND gate is 0.5 μm due to series connection), thereby lowering the average propagation delay.

For the camouflaged 2D cells, the increase in power consumption varies from 4% (for the XOR gate) to 42% (for the NAND gate), while for the camouflaged monolithic 3D cells the power overhead is between 6% (for the XOR gate) and 54% (for the NAND gate).

According to Table II, camouflaged 3D cells have, on average, 7.82% higher propagation delay and 2.33% higher power consumption as compared to the camouflaged 2D cells. This slight increase in the delay and power is due to the MIV impedances and the denser cell layout that produces additional coupling capacitances. Thus, for monolithic 3D technology, significant reduction in cell area is achieved at the expense of slight increase in cell-level power and delay characteristics. The chip-level implications of these effects are investigated in the following section.

IV. CHIP-LEVEL SIMULATION RESULTS

Proposed camouflaged 2D and camouflaged monolithic 3D standard cell libraries are used to investigate the system-level power and timing characteristics with existing physical design tools. Specifically, standard cells listed in Table I are used to generate four camouflaged circuits: a SIMON block cipher (balanced Feistel cipher to fulfill the security concerns of sensitive and hardware constrained applications [18]) and three ISCAS'89 academic benchmarks.

A. Experimental Setup

The proposed camouflaged cells are characterized (after *RC* extraction) with *Encounter Library Characterizer (ELC)* to obtain timing and power characteristics. SIMON and ISCAS'89 benchmark circuits are synthesized using *Synopsys Design Compiler*. Synthesized netlists are placed (at 70%

TABLE III
THE OVERALL NUMBER OF GATES AND DISTRIBUTION OF CAMOUFLAGED AND NON-CAMOUFLAGED CELLS.

Circuit	Number of Gates	Non-Camouflaged Cells		Camouflaged Cells					
		DFF	INV	NAND	NOR	AND	OR	XOR	XNOR
SIMON	903	168 (18.6%)	23 (2.5%)	529 (58.6%)	20 (2.2%)	1 (0.1%)	0	1 (0.01%)	161 (17.8%)
s35932	21281	1728 (8.1%)	7349 (34.5%)	0	0	11052 (51.9%)	1152 (5.4%)	0	0
s38417	22978	1636 (7.1%)	11253 (49.0%)	554 (2.4%)	848 (3.7%)	8121 (35.3%)	566 (2.5%)	0	0
s38584	20423	1426 (7.0%)	6784 (33.2%)	974 (4.8%)	1096 (5.4%)	7642 (37.4%)	2498 (12.2%)	1 (0.005%)	2 (0.01%)

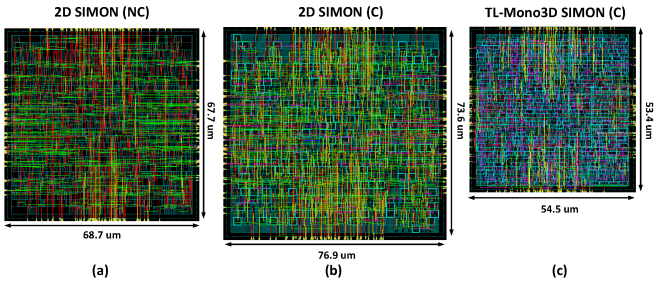

Fig. 6. **The layout views of SIMON cipher in (a) conventional 2D technology without camouflaging, (b) conventional 2D technology with camouflaging, (c) transistor-level monolithic 3D technology with camouflaging.**

placement density) and routed using *Cadence Encounter*. The clock frequency is 0.5 GHz for all of the circuits.

B. System-Level Evaluation

The distribution of cells in camouflaged SIMON cipher and ISCAS'89 benchmarks is listed in Table III. The percentage of camouflaged cells varies significantly depending upon the circuit.

1) Footprint and Wirelength: Physical layouts of the conventional 2D, camouflaged 2D, and camouflaged monolithic 3D implementations of the SIMON block cipher are depicted in Fig. 6. Approximately 80% of the gates is camouflaged. The area and overall wirelength characteristics in conventional 2D, camouflaged 2D, and camouflaged monolithic 3D are listed in Table IV. According to this table, in camouflaged 2D circuits, the area and wirelength increase, respectively, by 21.1% and 11.3%. For the camouflaged monolithic 3D circuit, however, the area and overall wirelength are reduced, respectively, by 37.7% and 15.7% as compared to the conventional 2D implementation.

For the three larger ISCAS'89 benchmarks, the average area increase for camouflaged 2D circuits is 17.5%. Alternatively, for camouflaged monolithic 3D technology, the area is reduced, on average, by 47.5%. The increase in the overall wirelength for camouflaged 2D circuits is highly design dependent and varies from approximately 6.3% (for s35932) to 17.6% (for s38584). For camouflaged monolithic 3D technology, the overall wirelength can be reduced, on average, by 19.7%.

2) Power Characteristics: The power consumption of the conventional 2D, camouflaged 2D, and camouflaged monolithic 3D circuits is compared in Table V. All of the three components of power consumption (gate, interconnect, and leakage) are provided. The camouflaged 2D circuits consume, on average, 8.3% more power than the conventional 2D version. This increase is primarily due to the increase in camouflaged gate power (see Table II) and longer interconnects. In camouflaged 2D cells, an additional metal layer is needed for intra-cell routing to make the two cells with different logic functions look identical. Since this metal layer occupies a routing track for inter-cell routing, the overall interconnect length increases (see Table IV), thereby increasing the net power. Alternatively, camouflaged monolithic 3D circuits consume, on average, 6.3% less power than the conventional 2D version. This reduction is primarily due to reduced area and therefore shorter interconnects. Thus, an important observation for monolithic 3D technology is that the cell-level power increase due to camouflaging (see Table II) is compensated by the reduction in interconnect power. Also note that in SIMON cipher and s38584, gate power is slightly reduced

TABLE IV
AREA AND WIRELENGTH CHARACTERISTICS IN CONVENTIONAL 2D, CAMOUFLAGED 2D (2D_C), MONOLITHIC 3D, AND CAMOUFLAGED MONOLITHIC 3D (3D_C) CIRCUITS. ALL OF THE PERCENTAGES ARE WITH RESPECT TO CONVENTIONAL 2D RESULTS.

Circuit	Design style	Area (mm^2)	Change (%)	Wirelength (μm)	Change (%)
SIMON_2D	2D	0.0047	-	10694	-
	2D_C	0.0057	**21**	11905	**11**
SIMON_3D	3D	0.0025	**-47**	8530	**-20**
	3D_C	0.0029	**-38**	9008	**-16**
s35932_2D	2D	0.086	-	163247	-
	2D_C	0.102	**18.6**	173471	**6.3**
s35932_3D	3D	0.042	**-51**	125921	**-23**
	3D_C	0.045	**-48**	127852	**-22**
s38417_2D	2D	0.080	-	133106	-
	2D_C	0.092	**15**	145519	**9.3**
s38417_3D	3D	0.041	**-49**	108975	**-18**
	3D_C	0.042	**-48**	110415	**-17**
s38584_2D	2D	0.080	-	170008	-
	2D_C	0.095	**18.8**	199865	**17.6**
s38584_3D	3D	0.040	**-50**	129650	**-24**
	3D_C	0.042	**-48**	135329	**-20**

TABLE V
COMPARISON OF POWER CONSUMPTION IN CONVENTIONAL 2D, CAMOUFLAGED 2D (2D_C), MONOLITHIC 3D, AND CAMOUFLAGED MONOLITHIC 3D (3D_C) CIRCUITS. *INT* REFERS TO INTERCONNECT POWER. ALL OF THE PERCENTAGES ARE WITH RESPECT TO CONVENTIONAL 2D RESULTS.

Circuit	Design style	Power Component (mW)			
		Gate	Int.	Leakage	Total
SIMON_2D	2D	5.57	1.43	0.20	7.20
	2D_C	5.89	1.59	0.25	7.73 (**7.4%**)
SIMON_3D	3D	4	1.12	0.20	5.32 (**-26%**)
	3D_C	4.18	1.17	0.25	5.60 (**-22%**)
s35932_2D	2D	66.42	16.45	3.48	86.35
	2D_C	73.31	17.58	4.42	95.13 (**10.2%**)
s35932_3D	3D	64.77	12.32	3.00	80.09 (**-7%**)
	3D_C	68.56	13.53	3.99	86.09 (**-0.3%**)
s38417_2D	2D	59.42	14.31	2.77	76.5
	2D_C	63.17	15.09	3.45	81.7 (**7%**)
s38417_3D	3D	59.64	11.03	2.45	73.12 (**-4%**)
	3D_C	60.93	11.89	3.14	75.96 (**-1%**)
s38584_2D	2D	58.74	14.03	2.77	75.54
	2D_C	62.56	16.50	3.55	82.61 (**9%**)
s38584_3D	3D	57.42	10.7	2.57	70.69 (**-6%**)
	3D_C	58.57	11.73	3.38	73.69 (**-2%**)

TABLE VI
TIMING CHARACTERISTICS IN CONVENTIONAL 2D, CAMOUFLAGED 2D (2D_C), MONOLITHIC 3D, AND CAMOUFLAGED MONOLITHIC 3D CIRCUITS. ALL OF THE PERCENTAGES ARE WITH RESPECT TO CONVENTIONAL 2D RESULTS.

Circuit	Design Style	Worst Slack (ns)
SIMON_2D	2D	0.921
	2D_C	0.770 **(-16%)**
SIMON_3D	3D	0.885 **(-4%)**
	3D_C	0.745 **(-19%)**
s35932_2D	2D	1.210
	2D_C	1.127 **(-7%)**
s35932_3D	3D	1.064 **(-12%)**
	3D_C	1.035 **(-14%)**
s38417_2D	2D	0.617
	2D_C	0.396 **(-36%)**
s38417_3D	3D	0.406 **(-34%)**
	3D_C	0.279 **(-55%)**
s38584_2D	2D	0.734
	2D_C	0.721 **(-2%)**
s38584_3D	3D	0.583 **(-21%)**
	3D_C	0.578 **(-22%)**

in 3D technology despite the increase at the cell-level power consumption. This behavior is due the reduced interconnect length in 3D technology which improves the average signal slew (due to lower interconnect resistance), which in turn reduces the short circuit power (one of the components of gate power).

3) Timing Characteristics: The worst slack (from the slowest timing path) of the conventional 2D, camouflaged 2D, and camouflaged monolithic 3D circuits is compared in Table VI. Note that the timing constraints are satisfied in all of the circuits at 0.5 GHz frequency. According to this table, camouflaging degrades the timing characteristics for both 2D and 3D technologies since the slack is reduced. The average reduction in slack is approximately 15.2% (equivalent to 5.85% percent of the clock period) for camouflaged 2D and 27.4% (equivalent to 10.6% percent of the clock period) for camouflaged 3D circuits. Note that in s38417, a relatively larger reduction in worst slack is observed. This characteristic is due the presence of a large number of NAND and AND gates along the critical path (specifically 54 out of 110 gates). According to Table II, largest increase in cell delay is observed for these two gates for both 2D and 3D camouflaging.

To better observe the change in timing characteristics, the slack histogram of the 50 slowest paths is provided in Fig. 7, where the effect of 2D and 3D camouflaging on slack is illustrated. 2D camouflaging degrades the slack by approximately 120 ps (6% of the clock period). 3D camouflaging causes an additional degradation of approximately 50 ps (with respect to non-camouflaged 2D) due to larger cell-level delays.

V. CONCLUSION

Circuit camouflaging has recently received attention to thwart image analysis based reverse engineering attacks. The number of camouflaged gates, however, should be sufficiently high to ensure its efficacy, which incurs significant overhead. The benefits provided by monolithic 3D technology in circuit camouflaging has been investigated at the cell- and chip-levels. Both 2D and 3D camouflaged cell libraries have been developed and fully characterized. The results obtained from fully placed and routed SIMON cipher and several academic

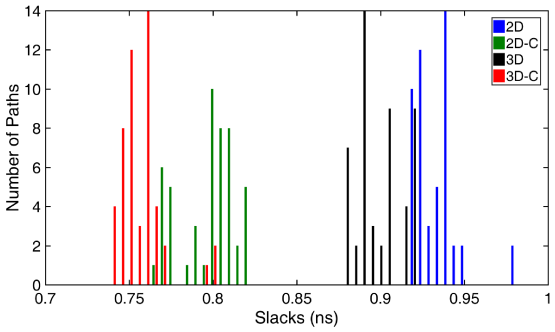

Fig. 7. **Slack distribution of the 50 slowest paths in SIMON cipher for 2D technology without (2D) and with (2D-C) camouflaging, and monolithic 3D technology without (3D) and with camouflaging (3D-C).**

benchmark circuits demonstrate that monolithic 3D technology is highly effective in eliminating not only the area, but also the power overhead of circuit camouflaging at the expense of a slight degradation in timing characteristics.

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