Towards High-Performance Polarity-Controllable FETs with 2D Materials

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***Abstract*— As scaling of conventional silicon-based electronics is reaching its ultimate limit, two-dimensional semiconducting materials of the transition-metal-dichalcogenides family, such as MoS_2 and WSe_2, are considered as viable candidates for next-generation electronic devices. Fully relying on electrostatic doping, polarity-controllable devices, that use additional gate terminals to modulate the Schottky barriers at source and drain, can strongly take advantages of 2D materials to achieve high on/off ratio and low leakage floor. Here, we provide an overview of the latest advances in 2D material processes and growth. Then, we report on the experimental demonstration of polarity-controllable devices fabricated on 2D-WSe_2 and study the scaling trends of such devices using ballistic self-consistent quantum simulations. Finally, we discuss the circuit-level opportunities of such technology.**

I. Introduction

Conventional CMOS logic circuits are based on doped, *n* or *p*, unipolar devices. With physical gate lengths as small as 14nm in modern devices, doping processes have become increasingly complicated to control [1]. Very abrupt doping profiles are needed, and due to random fluctuations of the number of dopants in the channel, device variability has been increasing, *i.e.,* fluctuations in the dopant number causes shifts in the threshold voltage value [2].

A device concept that does not require any doping would thus be highly desirable for new generation electronic devices, and 2-dimensional semiconducting *Transition Metal Di-Chalcogenide* (TMDCs) materials provide an excellent platform for its exploration. 2D-TMDCs have recently drawn considerable attention as viable candidates for flexible and beyond-CMOS electronics [3-8] thanks to their physical and electrical properties. The key enabler for the concept of polarity-controllable devices is the exploitation and control of the inherently ambipolar behavior, also known as ambipolarity, of *Schottky-barrier Field Effect Transistors* (SB-FETs). Both electrons and holes can be injected in the intrinsic device channel depending on the voltage applied to the gate. Ambipolarity is usually considered a drawback in standard CMOS devices and is suppressed thanks to the doping process that creates strictly unipolar devices. In polarity-controllable devices instead, the polarity is not set during the fabrication process, but it can be dynamically changed thanks to an additional gate, named *Polarity Gate* (PG). The PG modulates the SB at source and drain, and therefore enables us to select the carrier type to be injected into the device at runtime. In principle, no dopant implantation is required in the fabrication process of the device, thus there is no need for the separate development of *n*- and *p*-type device, to the benefit of fabrication simplicity and device regularity.

Here, we report on WSe_2 polarity-controllable devices with *on/off* currents ratio $>10^6$ for both electrons and holes conduction [9], and we study scaling trends with quantum transport simulations for ultra-scaled polarity-controllable devices [10]. We concluded that 2D-TMDCs with an energy bandgap of ~0.8eV could provide a successful scaling path for this technology. For the simulated MX_2 material, we showed $I_{on}>10^3$ μA/μm and $I_{on}/I_{off}>10^5$ down to L_G=5nm for both *p*- and *n*-type polarities. We use the results from the quantum transport simulations to study circuit performances for a 32-bit adder. We show that, thanks to the enhanced properties of the devices, we can achieve 7× lower EDP, when comparing to HP-CMOS.

II. Advances in 2D-materials

The demonstration of novel devices based on 2D films has often been carried out thanks to the exfoliation technique [11] originally developed for graphene. Although this top-down technique allows for the production of high quality thin flakes, with dimensions as big as tens of microns, this method is not scalable and does not allow any systematic control of the flake size and thickness. Moreover flake-to-flake variations, like folding and cracks, make it very challenging to extract any statistical behavior on the fabricated devices.

To enable the creation of a reliable technology based on 2D-TMDCs, that would go beyond the simple demonstration of stand-alone working devices, it is essential to develop methods for the production of defect-free, atomically thin films with uniform structural and electrical properties. Methods for the growth of TMDCs materials are based on *Chemical Vapor Deposition* (CVD) [12-21], Van der Waals

epitaxy [22-24] and molecular-organic CVD (MOCVD) [25]. These techniques have shown promising results for mono(few)-layer MoS_2 [12-15, 17-19, 25], WSe_2 [20,21], WS_2 [16, 25] and for creating 2D heterostructures [22-24].

Basic operational circuits [12] have been demonstrated on monolayer CVD grown MoS_2 with single devices showing gigahertz radio frequency performances combined with high current densities, exceeding 200μA/μm, and intrinsic low-field mobility up to 55 $cm^2.V^{-1}.s^{-1}$ [15]. Recently, a 1-bit microprocessor, consisting of 115 bi-layer MoS_2 transistors has been demonstrated [18], and remains the most complex circuit realized with 2D-materials to date. With respect to the challenge of growing a uniform and continuous 2D-film, growth of monolayer MoS_2 and WS_2 has been demonstrated [25] on a 4-inch wafer, using MOCVD, with a resulting device yield of 99%. However, the process has the drawback of being very slow, with growth times in the order of several hours per wafer. A considerable effort has also been spent in studying the variability of grown materials and the impact of the different fabrication steps on the film quality [26-28].

Together with growth methods the development of an efficient transfer technique for the semiconducting thin-film is necessary as these materials can often be grown only on particular substrates (sapphire, gold, etc.) that are not well suited for standard electronic fabrication processes. The ability of transferring the semiconducting 2D material from the growth substrate to any desirable substrate [13] will allow to completely decouple the material growth from the device realization. It is important to point out that the CVD methods that have shown to provide the best material quality are high-temperature processes (T>800° C), and are not compatible with monolithic 3D-integration on top of CMOS where a low temperature process is needed (<350° C).

Moreover, to ensure 3D integration on the back-of-the-line CMOS process also the doping process need to be addressed, as it often requires high-temperature annealing. The idea of replacing physical with electrostatic doping is very appealing in this regard, and our work on polarity-controllable devices aims at exploring this possibility.

III. Polarity Control on 2D-WSe_2

We used mechanically exfoliated multilayer WSe_2 (7.5 nm thick), that was transferred and aligned on a substrate where buried metal lines were used as PG, while the silicon substrate was used as CG (Fig. 1a). The metal contacts (Ti/Pd) were evaporated and provided a band-alignment suitable for the injection of both charge carriers (near mid-gap contacts).

The ambipolar behavior of the device can be seen in Fig. 1b, where the PG and CG gates were kept at the same potential during the voltage sweep. When using the two gates independently, the transistor polarity could be dynamically changed by the PG, while the CG controlled the *on/off* status of the device (Fig. 2). The experimental transfer characteristics showed a *p*-type behavior for V_{PG} <-6V, Fig. 2a, while *n*-type conduction properties are shown for V_{PG} >4V, Fig. 2b, on the same device. I_{on}/I_{off} ratios of 10^7 and 10^6 were achieved for *n*- and *p*-type operation respectively [9].

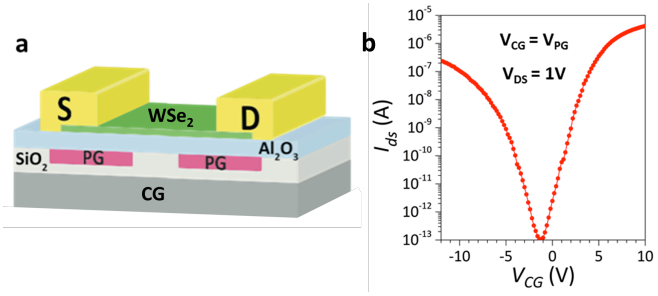

Figure 1. (a) 3D schematic of the fabricated devices. (b) Ambipolar transfer characteristics measured keeping $V_{PG} = V_{CG}$.

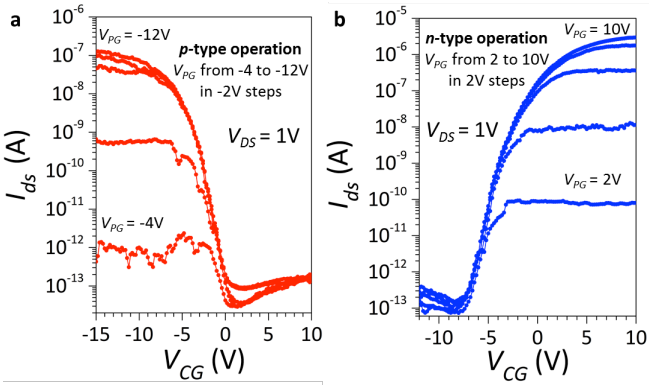

Figure 2. (a) Transfer characteristics of the device obtained for negative bias of the PG, showing *p*-type beahvior and complete subpression of *n*-current. (b) Transfer characteristics of the device obtained for positive bias of the PG, showing *n*-type beahvior and complete subpression of *p*-current.

IV. Quantum Simulations of Scaled Devices

To explore the potentials and limitations of these devices, we analyzed the performances of ultra-scaled polarity-controllable transistors [10] based on the schematic presented in Fig.3. HfO_2 (κ=25, EOT=0.47nm) was used as gate dielectric in a *Double-Independent-Gate* (DIG) structure. The length of the gated segments (L_{PG}, L_{CG}) were kept equal and the spacing (L_{OPEN}) was set to $L_{CG}/2$.

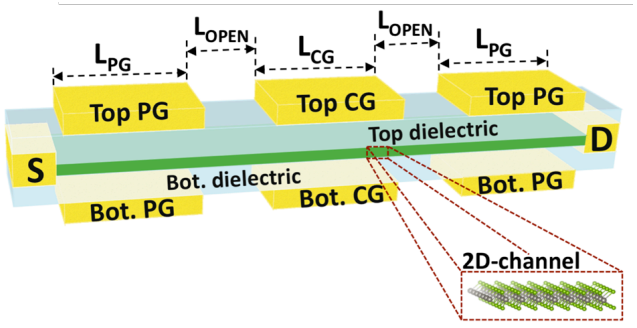

Figure 3. 3D schematic of the simulated polarity-controllable double-gated devices.

No doping was introduced at source and drain contacts and we assumed mid-gap Schottky barrier contacts, to achieve a symmetric behavior between the *n*- and *p*-type conduction branches. We performed self-consistent ballistic

simulations, iteratively solving Poisson and Schrödinger equation (within the NEGF formalism), with an open-source quantum transport code [29]. We used a 2-band tight-binding Hamiltonian to model the conduction and valence band of the 2D-material. The model was extended from monolayer to bilayer 2D materials by adding an interlayer hopping parameter in the effective-mass Hamiltonian, to account for coupling between the two layers [30].

Bilayer (2L) WSe_2 was first studied as a channel material. 2L-WSe_2 is reported to show a bandgap of ~1.1 eV [31], which is considerably reduced with respect to the ~1.5eV [32] bandgap of monolayer (1L) WSe_2. The smaller bandgap translates in a lowering of the Schottky barriers at the contacts (ϕ_{SB} = 0.55eV), which enables a more efficient carrier injection. Combined with the extra mobile charge provided by the additional layer, we expect 2L-WSe_2 to show better performances than 1L-WSe_2 for polarity-controllable devices. We studied the device switching properties by fixing the bias on the PG, thus setting its polarity, and sweeping the CG applied voltage. The ON-currents extracted from the simulated transfer characteristics are ~300 µA/µm, and there is an excellent control on the device *off* state with I_{off} well below 10^{-3} µA/µm, providing $I_{on}/I_{off} > 10^6$ down to L_G=4nm. However, the I_{on} of the device is still too low with respect to what is foreseen for unipolar doped 2D-transistors (I_{on}~2mA/µm) [33].

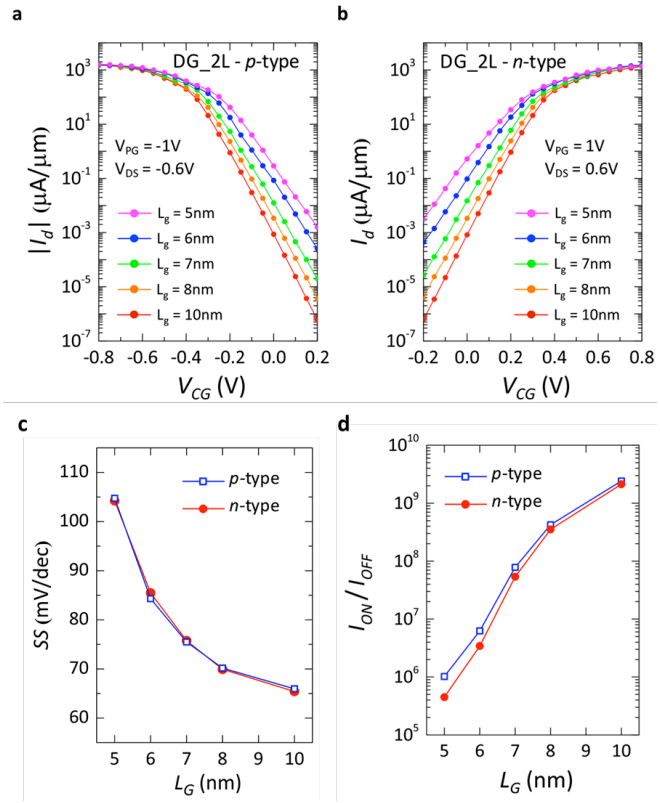

Figure 4. (a) Simulated transfer characteristics of *p*-type and (b) *n*-type FET. The gate length is varied from 10 nm down to 4 nm. (c) Sub-threshold slope, extracted from the simulated transfer characteristics for both *n*- and *p*-type behavior (d) I_{ON}/I_{OFF} for both *p*- and *n*-type behavior. In both cases, $I_{ON}/I_{OFF} > 10^5$ is shown down to L_G = 5nm.

To increase the performances of the device, and provide a successful scaling path, we need to use a 2D channel material with a lower energy bandgap, thus lowering the height of the Schottky barriers at source and drain.

Theoretical calculations [34-36] have shown that several materials, such as ZrS_2, HfS_2, $HfSe_2$, etc., have a lower semiconducting band-gap (0.7-0.9eV) and could prove to be well suited for application in SB-DIG FETs. Based on these theoretical analyses, we modelled a 2D-material (with E_G=0.8eV) and studied its potential application as a semiconducting channel in polarity-controllable FETs.

Fig. 4(a-b) shows the transfer characteristics for *n*- and *p*-type behavior at different L_G, with the corresponding values of subthreshold slope extracted from the simulations (Fig. 4c). Thanks to the lower Schottky barrier height at source and drain (ϕ_{SB} = 0.4 eV), the I_{on} is increased to ~1.5 mA/ µm, while I_{off} is well below 10^{-2} µA/µm down to L_G = 5 nm. The I_{on}/I_{off} ratios are above 10^5 down to L_G = 5nm (see Fig. 4d) for both *n*- and *p*-type behavior, showing the potential for the realization of ultra-scaled devices.

CIRCUIT LEVEL ANALYSIS

A. BCB Methodology

The 32-bit adder, as one of the *Beyond-CMOS Benchmarking* (BCB)'s flagship circuits [37], can be used as a performance metric for higher-level combinational circuits. The design, as adapted in BCB, utilizes the standard ripple-carry configuration.

While CMOS *High Performance* (HP)'s adders are optimized by a NAND-driven design, DIGFET's adders are optimized by an XOR- & MAJ-driven design due to (1) superior performance results at the gate level, and (2) the parallel computation of the carry signals.

Indeed, DIGFET technology allows for a full design style compatibility with CMOS due to the realization of unipolar pFETs and nFETs DIGFET transistors [38]. Nevertheless, DIGFET technology's rich set of operations, due to additional independent gate terminals, allow the three-input XOR gate and the three-input MAJ gate to be compacted within four transistors [38,39]. These gates are used here as the building blocks of the DIGFET-based adders. In particular, the 1-bit adder primitive can be implemented using a 3-input XOR gate (*sum*), a 3-input MAJ gate (*carry*), and an additional 3-input MAJ gate to realize in parallel the inverted carry signal.

B. Benchmarking Results

The integration of 2D-DIGFET technology into the BCB benchmarking approach allows us to compare DIGFET with other beyond-CMOS devices. Fig. 5(a) shows promising results for the 32-bit adder using 2D-MX_2 DIGFET technology.

When using the adapted ripple-carry adder described above, the *Energy-Delay Product* (EDP) is 7.2× smaller than CMOS HP and 8.4× smaller than CMOS LV. In fact, the EDP for DIGFET surpasses every beyond-CMOS device in BCB 3.0 for the 32-bit adder.

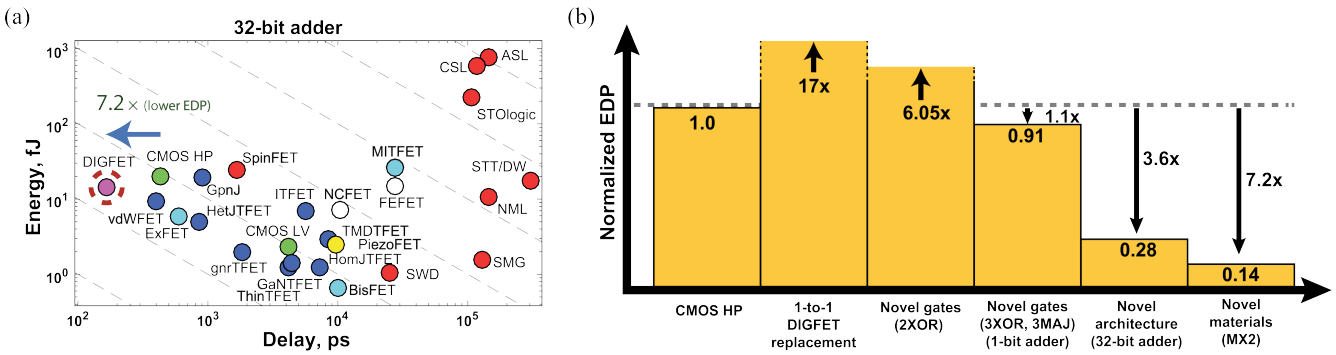

Figure 5. 32-bit adder's (a) switching energy and delay comparison and (b) EDP gain origin.

C. *Origin of the Benefit*

The integration of DIGFET technology into the BCB benchmarking can be broken-down into different parts to identify the different contributions to the EDP, as shown in Fig. 5(b). The benefits come both from the intrinsic capabilities of DIGFETs to realize compact logic gates and from the novel MX_2 material used in the analysis.

In order to break down the different factors we start our analysis considering *Silicon NanoWires* (SiNW) DIGFETs. We first consider the 1-to-1 replacement of CMOS transistors with SiNW-DIGFETs and observe a 17× EDP penalty (normalized to CMOS HP). The EDP increase is primarily due to the DIGFETs having (1) a 2.6× larger device area, a 2.5× larger parasitic capacitances - due to additional contacts - and (3) a 3.6× smaller ON-current for a 19% increase in supply voltage - due to the Schottky barrier at source and drain terminals.

Next, we introduce our 2-input XOR gate with DIGFET architecture [40] and observe a reduction of the EDP penalty to 6.05× . While this gate allows for an improvement of 2.9× in EDP, compared to the 1-to-1 replacement, the overall delay and energy are still larger than CMOS HP due to a 3.5× larger parasitic capacitance and 4.4× larger $V_{DD}/\ I_{ON}$. Note that, at this stage, while the 2-input XOR's are no longer NAND dominated, the full adders still contain a large number of sub-optimal NAND DIGFET gates.

Then, we introduce next our 3-input XOR and 3-input MAJ gates to fully take advantage of the DIGFET design capabilities and observe a benefit of 1.1× in EDP compared to CMOS HP. These circuits allow us to build the previously NAND-driven 1-bit full adders with one 3-input XOR gate and one 3-input MAJ gate. While we still observe 4.4× larger $V_{DD}/\ I_{ON}$, the reduction of contacts (1.4× lower number of gates) leads to a reduction in parasitic capacitance which leads to an overall EDP benefit.

Next, the introduction of the 32-bit adder novel architecture gives a benefit of 3.6× in EDP by allowing the parallel computation of both carry and inverted carry signals, compacting the logic depth. While this increases the energy consumption by 1.3×, the delay is reduced by 4.2×. This architecture was not previously used with the NAND-based beyond-CMOS devices in BCB due to their inefficient NAND-based MAJ gates.

Lastly, the introduction of bilayer-MX_2 [10], as the channel material, showed a benefit of 7.2× in EDP. The MX_2–based device outperformed the SiNW-based in terms of EDP of a factor of 2.0×, thanks to the reduced capacitance and the higher ON-current achievable. These results are consistent with previous studies on conventional doped devices [41].

V. Conclusions

We analyzed recent advances in the large area growth of 2D-materials and provided an overview of novel experimental results reported in literature. We addressed the need for doping-free device concepts that would ensure 3D integration on the back-of-the-line CMOS process.

Thus, we focused our attention on 2D-polarity controllable FETs. This novel class of devices fully relies on electrostatic doping of the Schottky contacts, using additional gate terminals, to allow polarity-controllable behavior at run-time.

We experimentally demonstrated the feasibility of polarity-control on 2D-WSe_2 and studied performances and scaling trends for different 2D-MX_2 materials using quantum transport simulations. Our results show I_{on} >10^3 µA/µm and I_{on}/I_{off} >10^5 down to L_G=5nm for both *p*- and *n*-type polarities.

Finally, we used the results from the quantum transport simulations to study circuit performances for a 32-bit adder. We showed that, thanks to the enhanced properties of the devices and the use of a 2D-MX_2 semiconducting channel, we can achieve 7× lower EDP, comparing to HP-CMOS.

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