A 12mW 70-100GHz Mixer-First Receiver Front-End for mm-Wave Massive MIMO Arrays in 28nm CMOS

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Multi-user MIMO (multiple-input multiple-output) systems are promising enablers for high-capacity wireless access in next-generation mobile networks. Leveraging antenna arrays at the access point, narrow beams can be steered to different users simultaneously, enhancing user capacity through spatial multiplexing. By employing a number of array elements M much larger than the number of users K (i.e. massive MIMO), simple linear beamforming algorithms can achieve nearly-optimal operation [1]. Operating massive MIMO systems at mm-waves results in compact antenna arrays and wide channel bandwidths. Within the available spectrum, the E-Band communication bandwidth (71-76GHz, 81-86GHz, and 92-95GHz) has recently gained attention for both access and wireless backhaul, due to low oxygen attenuation.

Hardware implementation of mm-wave massive MIMO systems poses several challenges and opportunities. On one hand, array gains allow one to relax the performance of the individual transceiver element, e.g. RX noise figure (NF) and TX power [1]. On the other hand, per-element area and power consumption have to be minimized. RF signal and local oscillator (LO) phase shifting and combining are popular in single-beam mm-wave phased arrays [2]. However, in a multi-beam system MxK mm-wave phase shifters would be required, resulting in significant area and power overhead. A baseband-combining architecture, as shown in Fig. 1, is hence more suitable for massive MIMO receivers, as compact analog or digital Cartesian beamformers can be employed [2]. As a drawback, since spatial filtering is performed after the RX front-end, high linearity is required to cope with in-band out-of-beam interferers.

In this paper, we propose an E-Band mixer-first RX front-end, minimizing area and power consumption without sacrificing linearity and bandwidth. Most wideband mm-wave receivers employ magnetically or capacitively coupled multi-stage LNAs [3]. However, compensating losses in interstage networks requires significant power consumption. Since power reduction, rather than noise figure minimization, is key in massive MIMO front-ends, a mixer-first receiver can be adopted instead. A 60GHz passive mixer was presented in [4], and achieves >30% matching bandwidth and 11-14dB NF. However, it employs wide MOS transistors (i.e. 64um/60nm) for ideal-

switch operation. At mm-waves, these require significant LO power to be driven, thus lowering the transceiver power efficiency. In [5], a low-power 5GHz mixer-first receiver is proposed, featuring small mixer switches that present a high input impedance, and are matched to the antenna through a 1-to-6 transformer. The input matching network provides passive voltage gain, resulting in moderate noise figure (~5.3dB) in spite of high mixer series resistance. Unfortunately, high-turn-ratio transformers cannot be implemented at mm-waves due to low-frequency self-resonance.

The proposed RX front-end is shown in Fig. 2. A passive quadrature downconverter is followed by open-loop differential baseband amplifiers. Neglecting the mixer's input capacitance, the input impedance of a capacitively-loaded passive mixer ($Z_{IN,MIX}$) has a peak centered around the LO frequency (f_{LO}), whose bandwidth is set by the mixer's load capacitance. The in-band impedance is proportional to the mixer switch series resistance [5]. In the proposed mixer, small switches (6um/30nm) are employed, resulting in ~400Ω in-band $Z_{IN,MIX}$ when the mixer is driven by a 600mV,diff,0-pk sinusoidal 80GHz quadrature LO. Matching this impedance to 50Ω would require a high-Q passive network, preventing wideband operation. Hence, frequency-translational feedback is employed to reduce $Z_{IN,MIX}$. Auxiliary feedback mixers are placed between the baseband amplifier output and the mixer input. Feedback switches are sized to obtain loop gain $G_{LOOP}\approx1$, resulting in $Z_{IN,MIX}$ being decreased by a factor of two within the loop bandwidth, as shown in Fig. 2. Since the baseband amplifier contributes to G_{LOOP}, the feedback switches can be considerably downsized compared to the mixer, hence contributing to only ~10% capacitance overhead. Since $G_{LOOP}\approx1$, the feedback does not lead to stability concerns.

The remaining input impedance matching is performed by a wideband transformation network, combining an L-match and an input shunt resonator, as shown in Fig. 2. The input resonator not only neutralizes the pad capacitance, but also improves the matching bandwidth. DC bias and ESD protection are placed on the negative terminal of the shunt inductance, which is AC shorted to ground. The network provides ~6dB passive voltage gain, hence amplifying the signal before it enters the noisy passive mixer. Simulated RX noise figure is ~8dB, 3dB higher than [5] due to higher losses at mm-waves, unavailability of a 25% duty cycle LO and ~1dB noise penalty due to the feedback. The baseband amplifier is designed to provide 13dB gain with 2mA current

consumption. Gate-drain neutralization is employed to reduce the input capacitance, so that the dominant pole is located at the amplifier output.

Neutralized differential LO buffers with resonant loads, shown in Fig. 3, were co-designed with the mixer to provide 7dB maximum gain. Given the small mixer size, the buffer load impedance magnitude is ~500Ω, resulting in only 2mA nominal current consumption for each buffer. An LC series trap, tuned at ~85GHz, and a choke inductor were added to improve common-mode rejection at f_{LO}. A differential transformer-coupled quadrature hybrid is employed to generate the quadrature LO.

A prototype was realized in 28nm CMOS without ultra-thick metal (see Fig. 7). The RX core area, including input pad, LO buffers and quadrature hybrid, is only 0.085 mm^2. The front-end is followed by a VGA and a matched output buffer for measurement purposes. The die was wire-bonded to a PCB, and high-frequency probes were used for the RF and LO pads. The LO was generated off chip, and a constant 300mV,diff,0-pk swing was provided at the LO buffer input. Fig. 4 shows measured S11 for different values of f_{LO}. Wideband matching with S11<-10dB over 74-94 GHz is achieved, and the bandwidth is improved to 70-100 GHz when the LO buffer current is increased to 4 mA to compensate losses at the edge of the buffer bandwidth.

NF, conversion gain and input-referred 1dB compression point (ICP1dB) at 100MHz offset from f_{LO} are shown in Fig. 5. Gain and ICP1dB were measured using a frequency-translational VNA, whereas a W-Band noise source and a spectrum analyzer were used to evaluate NF with the Y-factor method. The RX front-end achieves 19.5-25.3dB voltage gain and 8-12.7dB NF over a wide operation range, ultimately limited by the LO chain bandwidth. Conversion gain increases at high frequency due to a rise in the matching network voltage gain. Linearity gets worse at the bandwidth edges, since the reduced LO swing results in soft switching in the mixer. The baseband bandwidth is 1.8 GHz, when driving a 100fF differential load. The flicker noise corner, set by the baseband amplifier, is at 10MHz.

Measurement results are compared to state-of-the-art low-power CMOS mm-wave receivers in Fig. 6. The proposed receiver covers all the licensed E-Band communication spectrum with -24dBm worst-case ICP1dB and 9.5dB worst-case NF, and only 12mW power consumption including the LO buffers, the lowest reported for quadrature mm-wave CMOS receivers to our knowledge. Ultra-low-power operation and small footprint, together

with linearity comparable with state of the art, suggest the use of the proposed front-end for massive MIMO mm-wave arrays.

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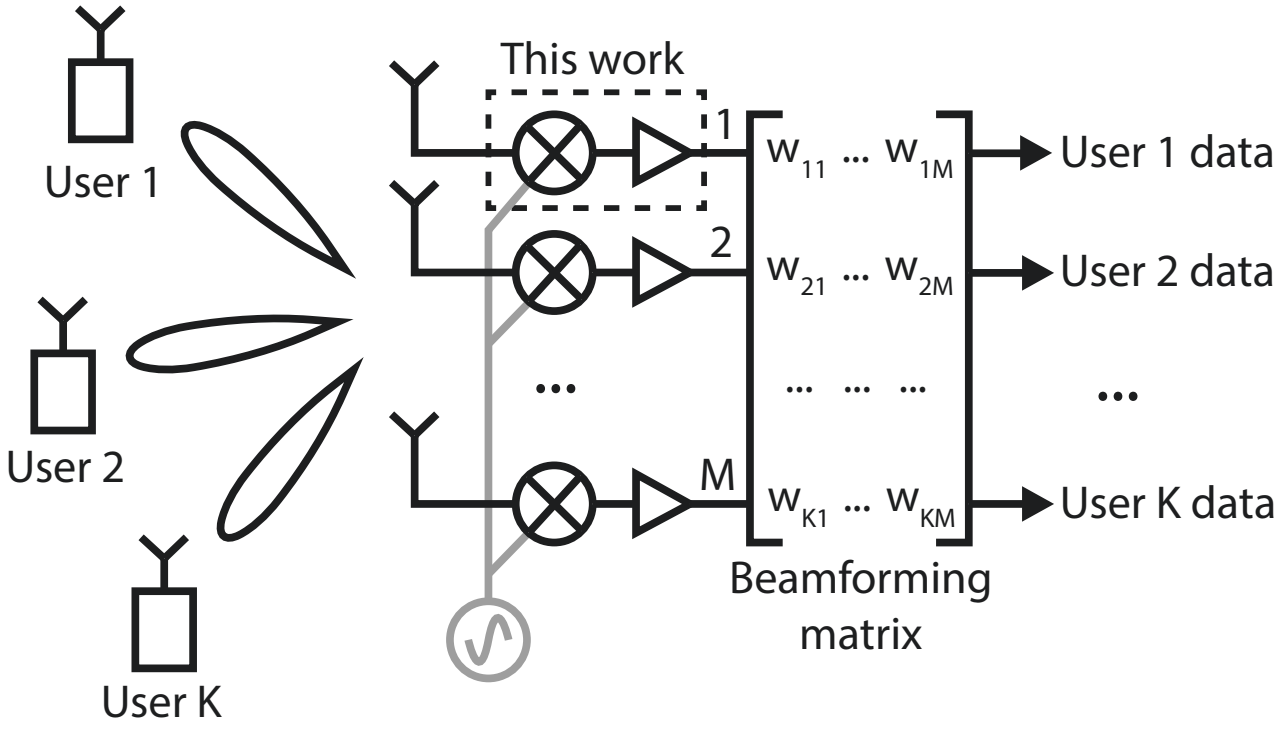

Fig. 1. Multi-user MIMO receiver architecture with baseband signal combining.

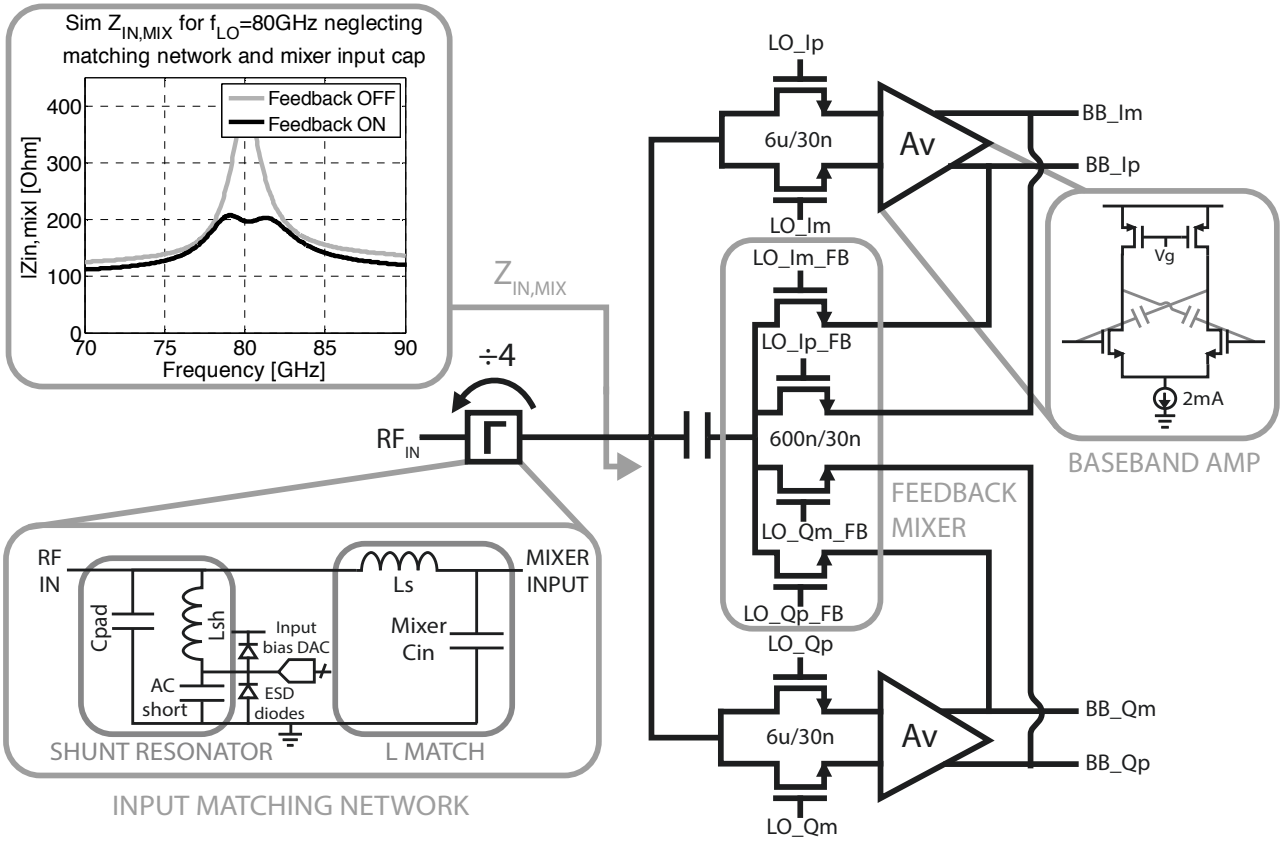

Fig. 2. Receiver schematic and simulated mixer input impedance.

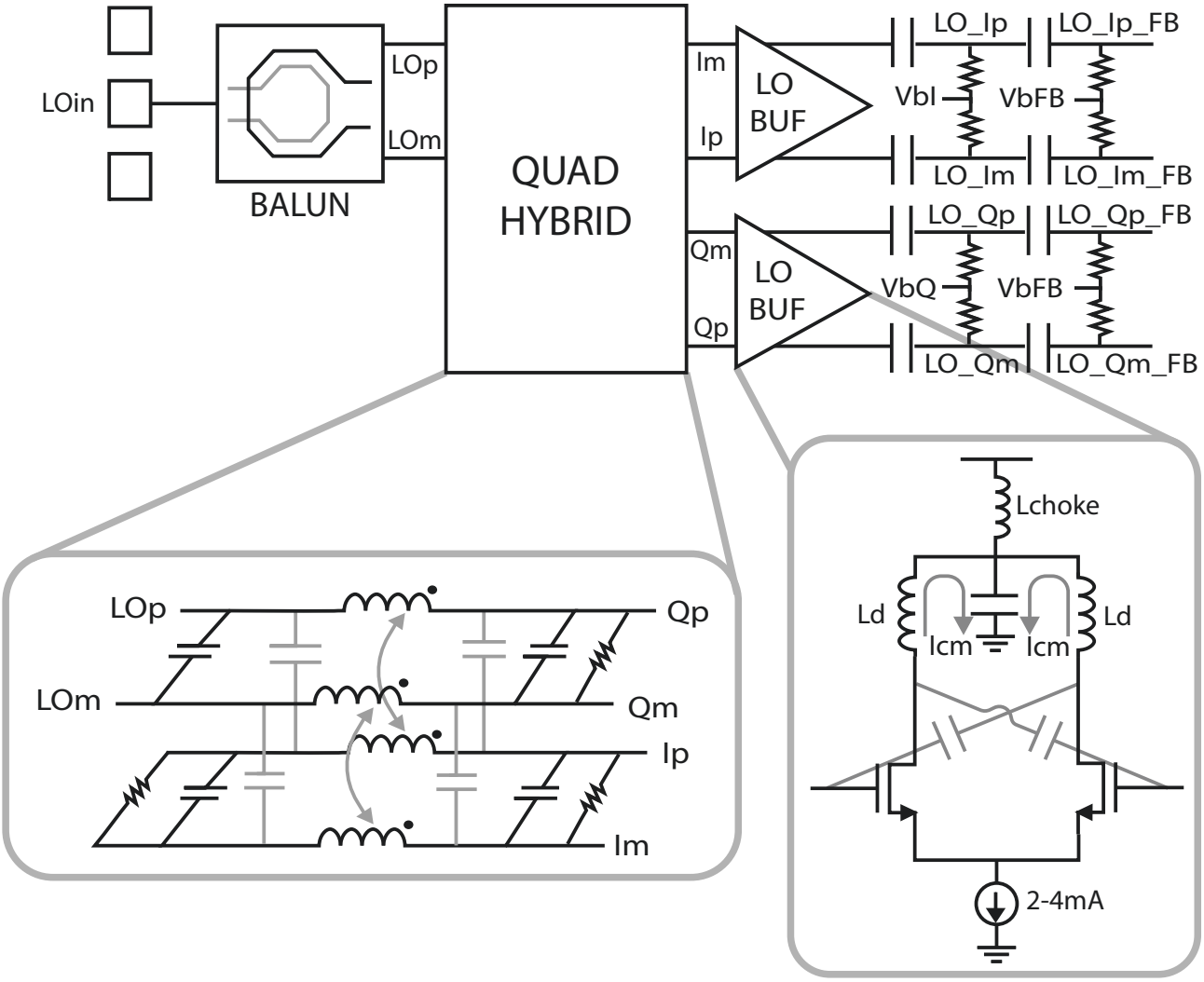

Fig. 3. LO distribution chain.

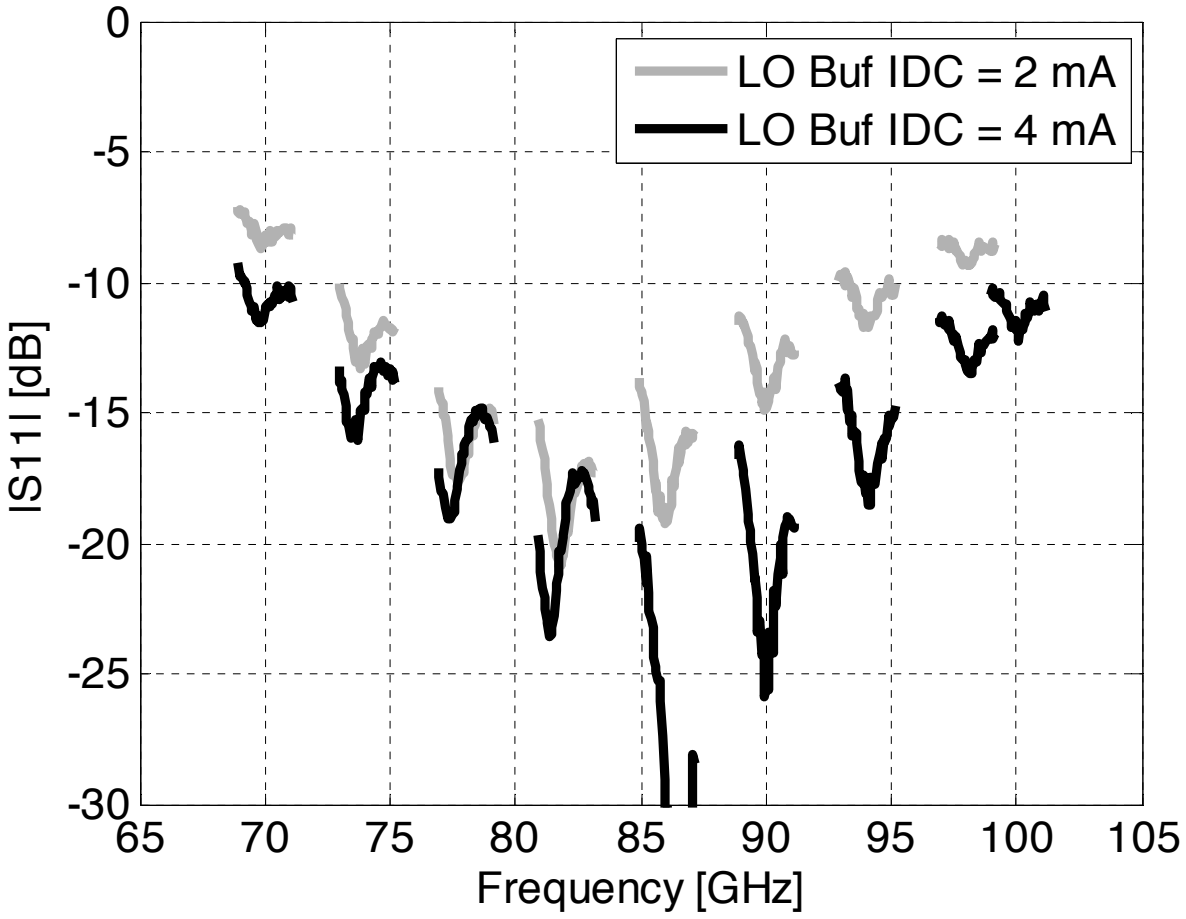

Fig. 4. Measured S11 magnitude when sweeping the RF frequency within ±1GHz around the LO frequency.

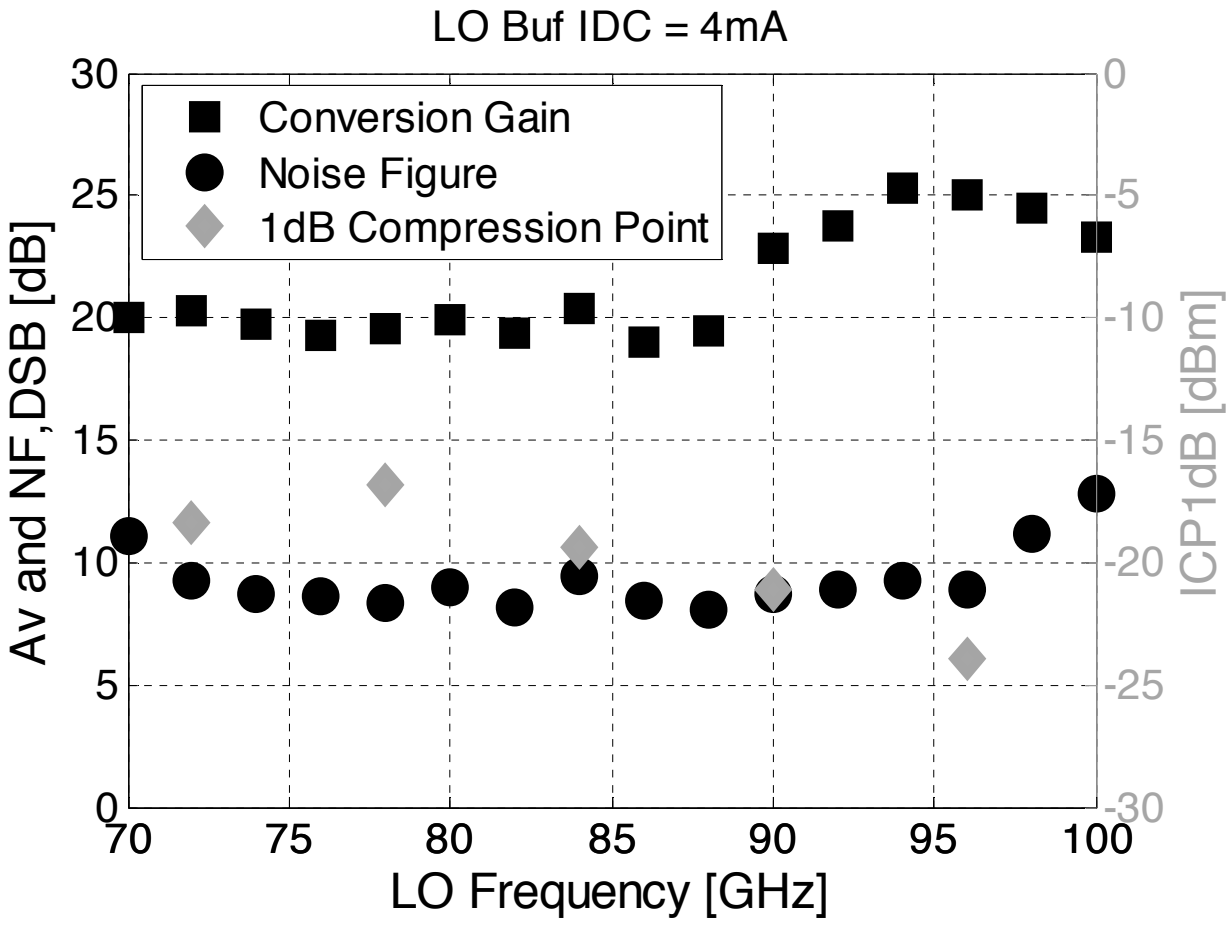

Fig. 5. Measured DSB noise figure, conversion voltage gain and input-referred 1dB compression point at 100MHz offset for different values of f_{LO}.

	This work		[3]		[6]	[2]		[4]
Technology	**28nm CMOS**		28nm CMOS		65nm CMOS	45nm CMOS SOI		65nm CMOS
Architecture	**Mixer-first direct conversion**		Sliding IF heterodyne		Direct conversion	Direct conversion		Mixer-first direct conv
Vdd [V]	**1**		0.9		1.8	0.6	1.1	1.2
Center freq [GHz]	**84**	**85**	75		83	55		58
Fractional RF BW	**26.5%**	**35.3%**	36.7%		19%	38%		>31%
Baseband BW [GHz]	**1.8**	**1.8**	N/A	N/A	9	1.2		0.32
Voltage gain [dB]	**21-26**	**19.5-25.3**	23.6	30.8	13	20.2º	26.2º	13
NF,DSB (best) [dB] §	**8.2**	**8**	7.3	9.5	5.5	7.7	5.5	11
NF,DSB (worst) [dB]	**10.8**	**12.7**	9.1	12.9	7.5	12^º	10^º	14
ICP1dB (best) [dBm] §	**-18**	**-16.8**	-25	-20	-16	-28 º	-27 º	-12
ICP1dB (worst) [dBm]	**-26.5**	**-24**	-30.7^	-25.3^				
Pdc [mW]	**8**	**12**	57		89 +	14º	30º	14
Area [mm^2]	**0.085**		0.675		0.23 +	0.225º		0.18 *

+ no quadrature output
^ estimated from plot
º per element
* estimated from chip photo
§ best and worst performance reported over operating frequency range

Fig. 6. Performance summary and comparison with state-of-the-art integrated mm-Wave receivers.

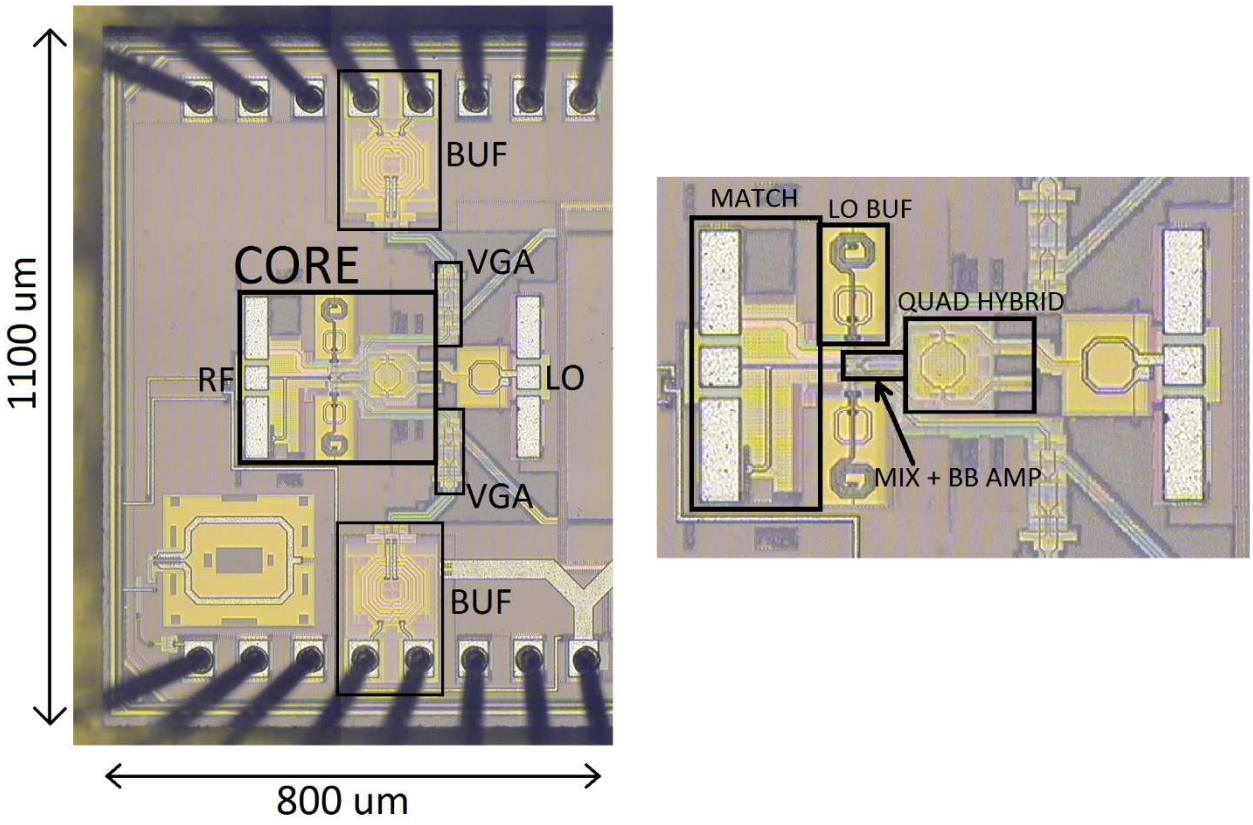

Fig. 7. Chip micrograph and detailed view of the RX front-end layout.

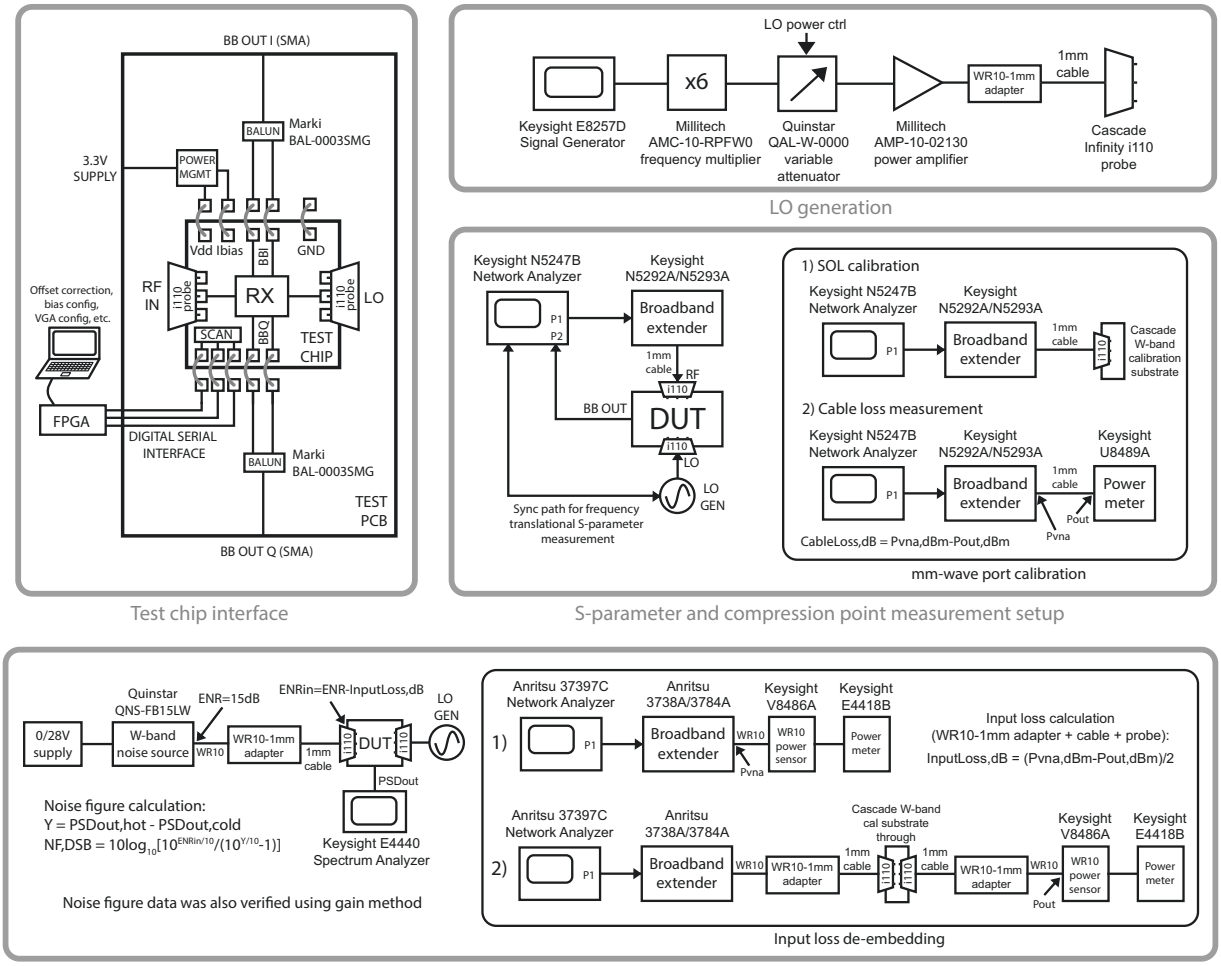

Fig. S1. Measurement setup.

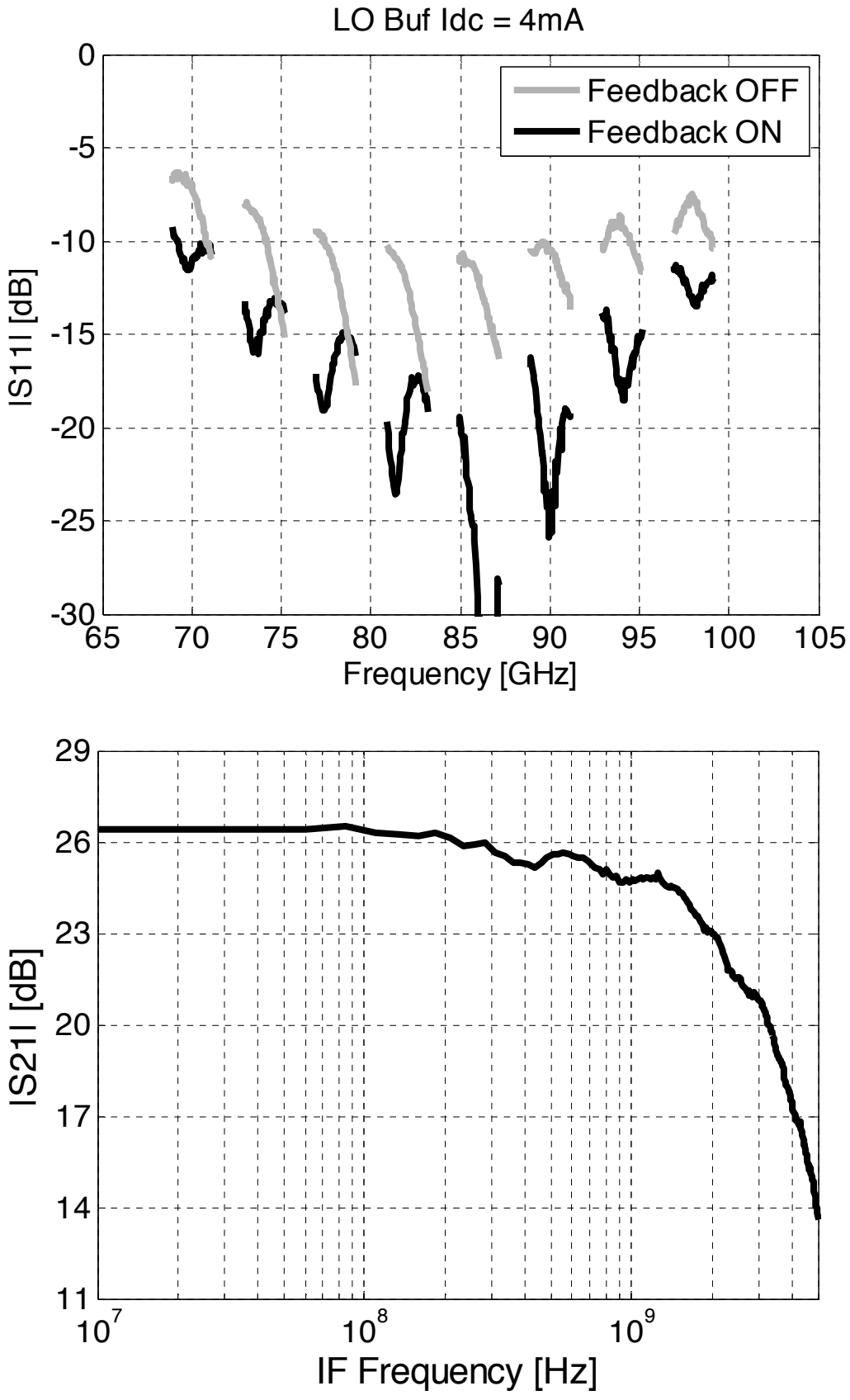

Fig. S2. Measured S11 vs f_{LO} with and without feedback mixer enabled, and measured frequency-translational S21 at 78GHz f_{LO}. S21 measurement includes gain contribution of on-chip VGA and output buffer.

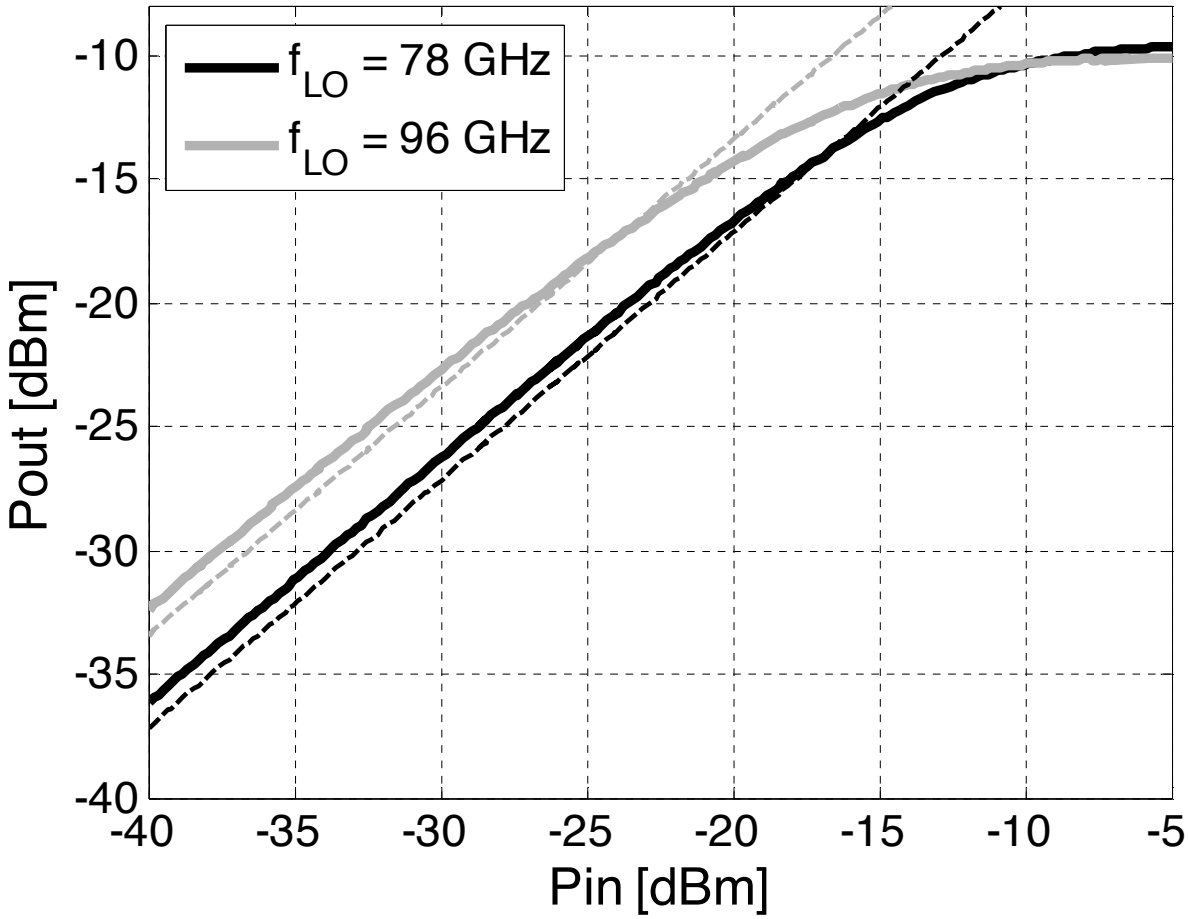

Fig. S3. Measured output power vs input power at 100MHz offset from 78GHz and 96GHz f_{LO}.