

PROCEEDINGS OF SPIE

[SPIDigitalLibrary.org/conference-proceedings-of-spie](https://spiedigitallibrary.org/conference-proceedings-of-spie)

Novel cubic phase III-nitride complementary metal-oxide-semiconductor transistor technology

C. Bayram, R. Grady, K. Park

C. Bayram, R. Grady, K. Park, "Novel cubic phase III-nitride complementary metal-oxide-semiconductor transistor technology," Proc. SPIE 10540, Quantum Sensing and Nano Electronics and Photonics XV, 105401G (26 January 2018); doi: 10.1117/12.2286738

SPIE.

Event: SPIE OPTO, 2018, San Francisco, California, United States

Novel cubic phase III-nitride complementary metal–oxide–semiconductor transistor technology

C. Bayram¹, R. Grady, and K. Park

Department of Electrical and Computer Engineering, University of Illinois at Urbana-Champaign, Urbana, IL USA 61801

Innovative COmpound semiconductoR Laboratory, Micro and Nanotechnology Laboratory, Urbana, IL USA 61801

ABSTRACT

Here we propose a new wide band gap logic circuitry providing emerging power electronics with reliable logic control capabilities with 500 MHz+ switching speeds and withstanding 300V+. Particularly, a three-stage ring oscillator composed of NMOS ($\mu_e = 1000 \text{ cm}^2/\text{V}\cdot\text{s}$) and PMOS ($\mu_h = 250 \text{ cm}^2/\text{V}\cdot\text{s}$) cubic phase GaN devices (with V_T of 0.77 V and -0.84 V , respectively) is simulated. The propagation delay is minimized by optimizing the width-to-length ratio (W/L) between the NMOS and PMOS devices. Transient response of the simulation illustrates the ability of the CMOS inverter to operate at a maximum frequency of 1.22 GHz with a full voltage swing between V_{DD} of 2.5 V and 0 V. The proposed cutting-edge p-channel GaN high hole mobility transistor (HHMT) solves one of the most longstanding problems in power electronics and constitutes the basis of an innovative reduced total life cycle cost that will serve as the cornerstone of the next generation of integrated, scalable, and reliable power systems.

Keywords: logic, high electron mobility transistor, high hole mobility transistor, Gallium Nitride, ring oscillator

1. INTRODUCTION

Silicon CMOS continues to drive to impressive levels of RF performance. At the same time, these impressive levels of performance come with massive integration density, allowing large digital correction or signal-conditioning circuits to be integrated on the same die as the power/RF ones. One significant challenge for silicon devices is in supporting high-voltage, high-power-density applications in power amplification and power conversion. For power conversion applications, discrete Si-trench devices can achieve breakdown voltages only in excess of 50 V and with switching frequencies below 1 MHz. Low switching frequencies lead to large passive sizes, degraded transient response, and inability to support RF and millimeter-wave applications.

For nitride-based compound semiconductors, the large bandgap (3.4 eV for GaN and 6.2 eV for AlN), high critical electric field strength (on the order of 10^6 V/cm), and high saturated electron drift velocities (on the order of 10^7 cm/s) make these materials ideal for high-power, high-voltage applications (Table 1). The formation of a two dimensional electron gas (2DEG) in the AlGaIn/GaN system due to conduction band offsets and polarization-induced doping results in sheet concentrations of the order of 10^{13} cm^{-2} and relatively high mobility values of the order of $1500 \text{ cm}^2/\text{V}\cdot\text{s}$ [1], leading to transistor cutoff frequencies in excess of 300 GHz.

For next-generation high-power high-voltage applications, GaN transistors are ideal replacements for Si ones [2]. The integration of GaN transistors with power systems leads to new levels of performance in both power amplification and power conversion. GaN devices used in the power amplifier and in the power train of the buck converter allow high-power densities, high performance, and reduced volume unachievable with any silicon-only-based technology. For instance, in electric vehicles, such high-current transistors will increase charging speeds, hence considerably increase vehicle mobility. GaN transistors for high-power, high-voltage, high-temperature applications are extremely important for the future of power transistors because it is compatible with existing silicon technologies [3], saves energy, and brings additional capabilities to the silicon-dominated transistor world.

¹ cbayram@illinois.edu ; <http://icorlab.ece.illinois.edu/> ; Phone: +1 (217) 300-0978

One critical challenge in the deployment of GaN devices in such demanding applications is the logic circuitry. GaN devices can sustain high temperatures and hence reduce cooling needs. Nonetheless, lack of suitable logic circuitry necessitates cascode formations where Si logic circuitry is used for managing GaN high-power/RF devices. As such, the entire system is limited by the Si devices and the full potential of GaN devices becomes bottlenecked. Hence, it is essential to create GaN-based complementary logic circuits capable of operating under the very same demanding conditions as GaN-based high-power/RF circuits. Here we report theoretical investigation and simulation of a novel cubic phase III-nitride complementary metal–oxide–semiconductor transistor technology platform that bridges material, device, and architectural innovations and integrates both n- and p-channel GaN transistors on silicon substrates for GaN logic circuitry.

Current Approaches to Normally-off Transistors

A key issue in GaN high mobility transistors (HMTs) is normally-on n-channel operation. Because of the inherent polarization fields in hexagonal (h-) phase GaN, conventional h-phase GaN HEMTs are normally-on, meaning a conductive 2DEG electron channel is formed in the AlGaIn/GaN heterointerface even under no external bias. For safety and energy savings in high-power/high-frequency applications, normally-off HEMTs are desired. For CMOS devices, p-channel HEMTs are needed.

There are primarily three current means of achieving a normally-off n-channel GaN HEMT device:

- **Fluorine implantation:** [4] The implantation is typically performed using a CF₄ plasma treatment followed by rapid thermal annealing (RTA). The resulting devices have a high density of fluoride ions near the 2DEG channel, which prevent the 2DEG formation. This technique is highly sensitive to the implant conditions and suffers from a reduced on-state I_{DS}.
- **Gate recessing:** [5] Recessed gate HEMTs are made by etching a portion of the barrier (i.e., AlGaIn) and thus reducing the distance between the gate contact and the 2DEG in a selective region. This increases the turn-on voltage V_T; however, achieving high turn-on voltages is problematic and low leakage currents at operating voltages can be difficult.
- **P-doped GaN gate contact:** [6] This approach achieves high turn-on voltages of up to 3V. The biggest problem is the activation of the p-type dopants. Magnesium is typically used to achieve a p-doped GaN layer, but the large activation energy (~ 200meV) leads to a much lower hole concentration than chemical concentration.

Current Approaches to p-channel Transistors

For logic circuits, a p-channel device is a must. There are primarily two current means of achieving a p-channel GaN HEMT device:

- **Inverted GaN/AlGaInN heterostructures:** [7 – 9] This design relies on polarization doping to form the 2DHG at the GaN-AlGaInN interface. AlGaInN material quality impacts the GaN atop hence also the 2DHG mobility. Besides, the structure also has an AlGaInN-GaN substrate interface which could form an n-channel leading to electronic crosstalk across double channels. This technique is highly sensitive to the deposition conditions, and the devices created using this technique suffer from low 2DHG mobility.
- **N-polar structures:** [10] N-polar III-nitrides are formed through changing the material deposition conditions (such as very high ammonia flow rate). This reduces the material quality due to reduced adatom mobility. The drawbacks of this approach are reliability and scalability concerns.

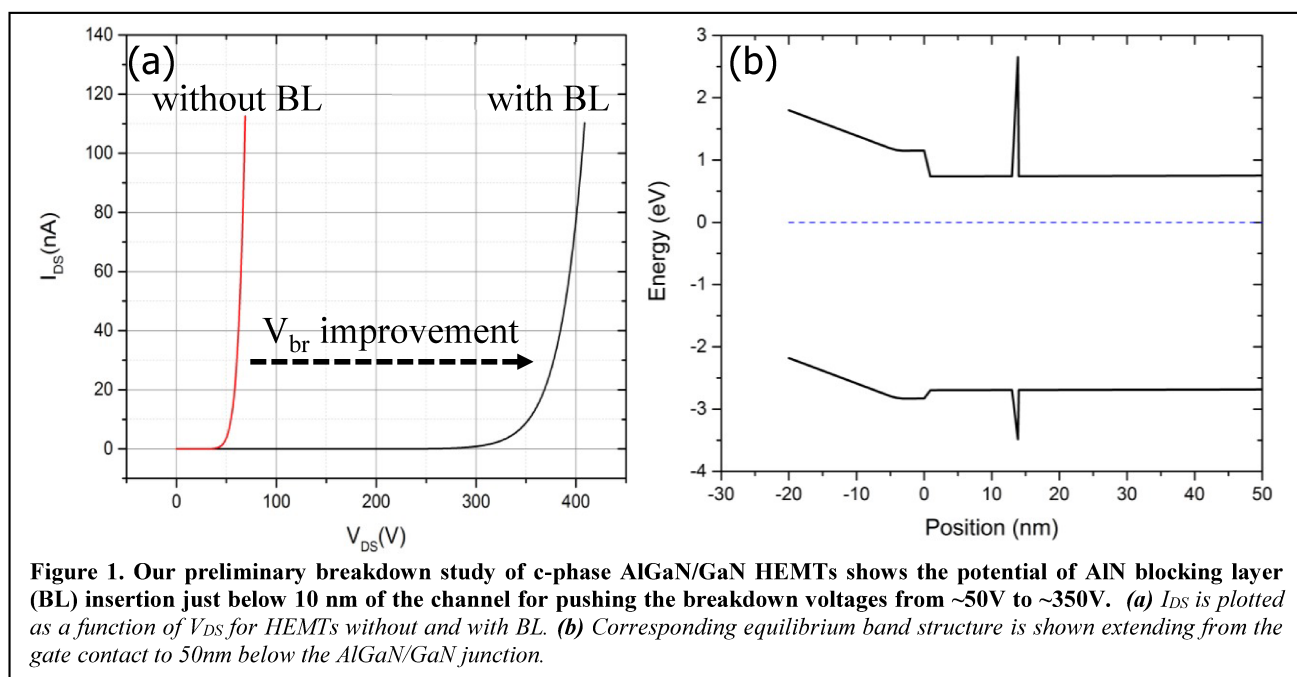
	JFOM	BFOM	BHFFOM
Expression	$\frac{E_c v_s}{2\pi}$	$\epsilon \mu E_G^3$	$(R_{on} C_{in})^{-1}$
Si	1	1	1
4H-SiC	410	290	34
GaN	790	910	100

Table 1. Johnson's, Baliga's, and Baliga's high frequency figures of merit (FOM) of Si, 4H-SiC, and GaN when normalized to Si [2]. E_c is critical electric field, v_s is the saturation velocity, E_G is bandgap, R_{on} is on resistance, C_{in} is input capacitance, ϵ is the dielectric constant, and μ is the mobility.

Proposed Approach to p-channel Transistors

A key issue in GaN HEMTs is normally-on n-channel operation. Because of the inherent polarization fields in hexagonal (h-) phase GaN, conventional h-phase GaN HEMTs are normally-on, meaning a conductive 2DEG electron channel is formed in the AlGa_xN/GaN heterointerface even under no external bias. For safety and energy savings in high-power/high-frequency applications, normally-off HEMTs are desired. For CMOS devices, p-channel HEMTs are needed.

Here we exploit the polarization-free characteristics (along the growth direction) of cubic phase GaN materials to enable normally-off p-channel cubic phase AlGa_xN/GaN HEMTs. The c-phase Al_xGa_(1-x)N/GaN HEMT structure under investigation consists of an Al_xGa_(1-x)N layer grown on top of a c-GaN substrate. The Al_xGa_(1-x)N barrier layer is composed of three parts: undoped layers of AlGa_xN₁ and AlGa_xN₃ (with thickness of t_1 and t_3) and δ -doped layer of AlGa_xN₂ (with thickness of t_2). The δ -doped AlGa_xN₂ layer provides carriers to the hole channel formed at the AlGa_xN/GaN heterointerface while the AlGa_xN₃ layer separates the δ -doped AlGa_xN₂ layer from the channel and reduces the impurity scattering effects. The AlGa_xN₁ layer separates the gate contact from the 2DEG, controlling the gate-contact-induced electric field effects on the 2DEG channel. The structure is detailed in Figures 4 and 5.



2. SIMULATION

In the simulation, we use the Varshni model to calculate bandgaps and will consider thermionic emission currents for electrons to accurately model carrier flow along the heterojunction, following the literature [11]. For carrier flow and densities when confined along the triangular well, a quantum potential is considered. The equations solved at each step of the simulation are Poisson's equation, the continuity equation for both electrons and holes, and the quantum potential equations [12 – 14].

For simulating the band structure of the wide bandgap materials, the temperature dependence given by the Varshni model [15] $E_G(T) = E_G(0) \times \alpha T^2 / (\beta + T)$ is used, with values of α , β as given in ref [13 – 14]. During the course of our simulations, Fermi statistics are used to improve accuracy as Fermi level energy (E_F) exceeds valence band energy (E_V). Thermionic emission currents are considered for holes to accurately model carrier flow along the heterojunction, following the literature. [11]

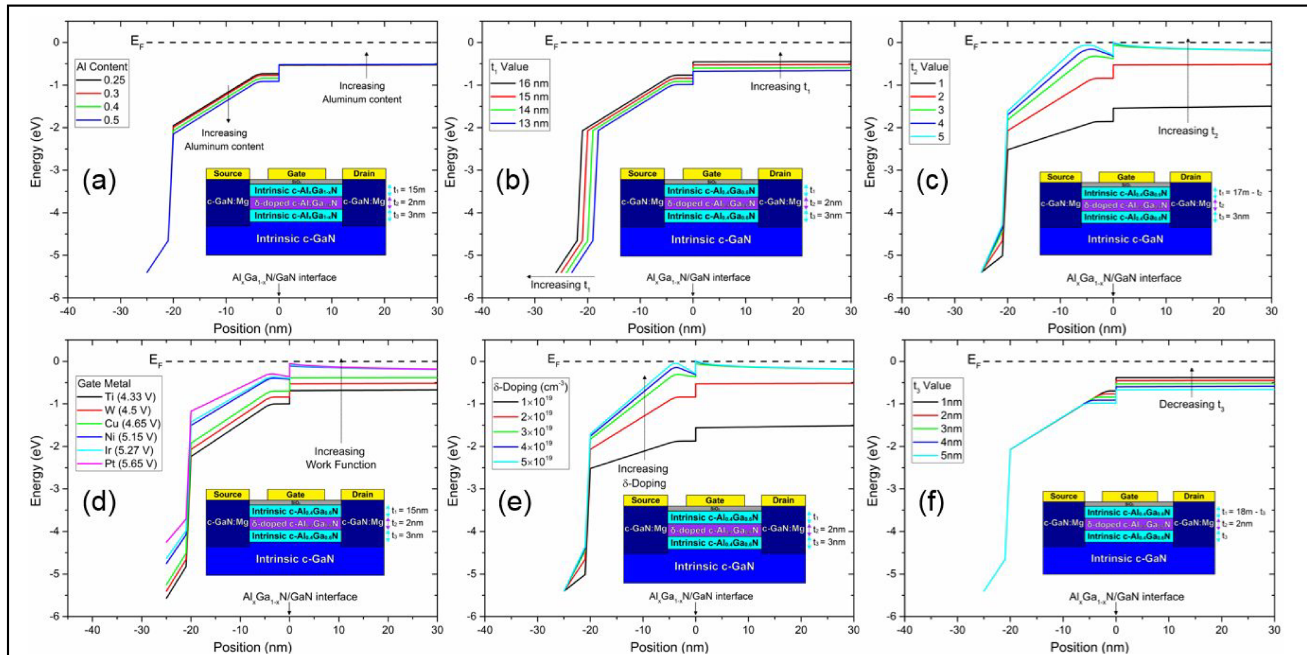


Figure 2. Our preliminary systematic study of cubic phase p-channel AlGaIn/GaN HEMT parameters. The equilibrium band structure is shown extending from the gate contact to 30nm below the $Al_xGa_{(1-x)}N/GaN$ junction. The insets show the simulated structures as functions of (a) Al-content, (b) t_1 , (c) t_2 , (d) gate metal, (e) δ -doping, and (f) t_3 . Control over normally-on and normally-off p-channel AlGaIn/GaN HEMTs can be enabled through gate metal selection, t_2 thickness, and δ -doping. [13]

For carrier flow and densities when confined along the triangular well, a quantum potential is to be considered. This potential, denoted Λ_h , adds quantization to carrier densities (h) in the quantum well according to

$$h = N_c F_{1/2} \left(\frac{E_{F,h} - E_v - \Lambda_h}{kT_n} \right) \text{ without impacting simulation times significantly [12]. } \Lambda_h \text{ is obtained by solving}$$

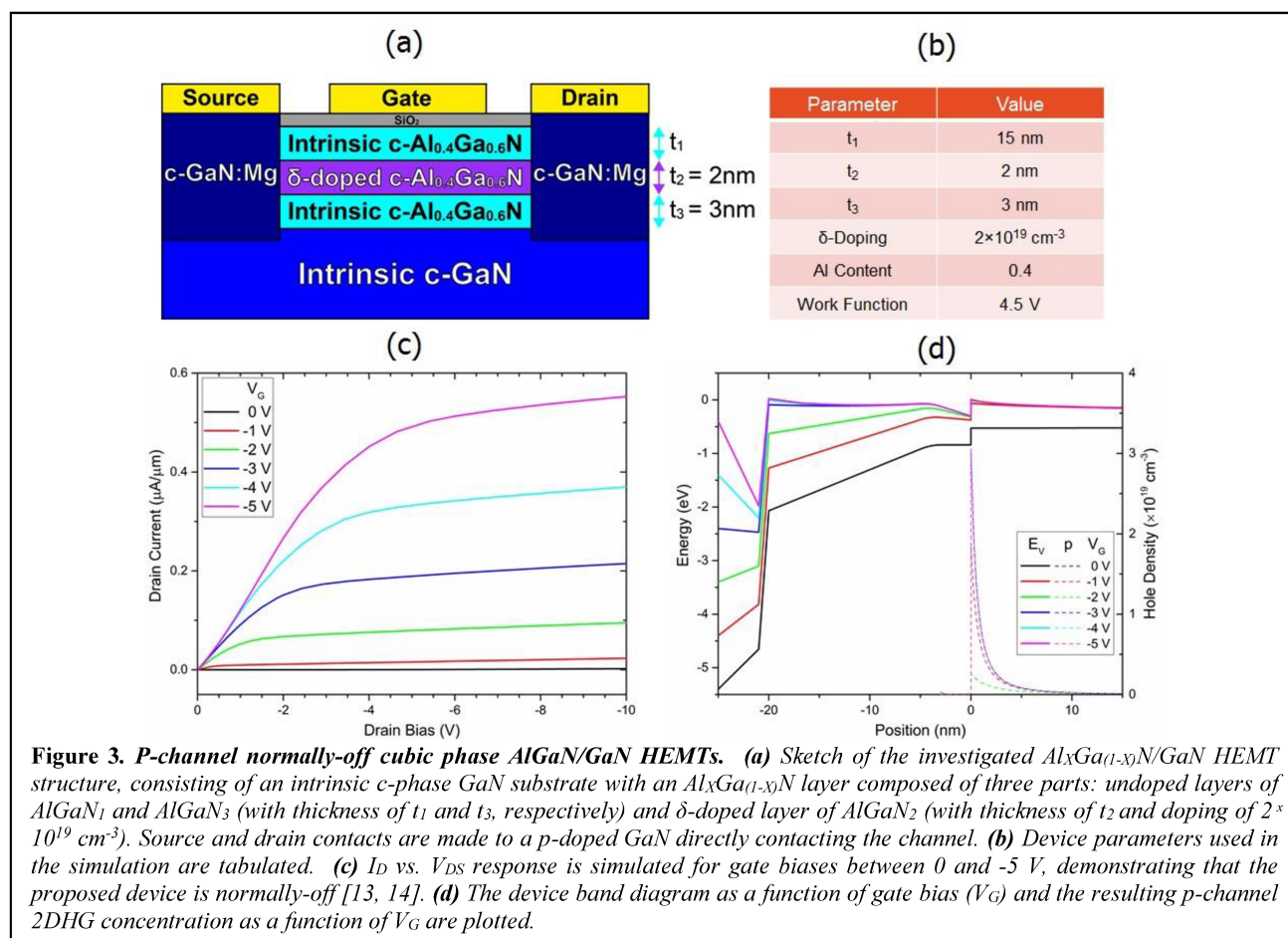
$$\Lambda_h = -\frac{\gamma \hbar^2}{12m_h} \left\{ \nabla^2 \ln h + \frac{1}{2} (\nabla \ln h)^2 \right\} = -\frac{\gamma \hbar^2}{6m_h} \frac{\nabla^2 \sqrt{h}}{\sqrt{h}}, \text{ where } \gamma \text{ is a fit factor. The effects of bandgap narrowing}$$

with heavy doping will be neglected initially. Carrier recombination is computed using a combination of Shockley-Read-Hall (SRH) recombination, Auger recombination, and radiative recombination models. While modeling the electrical behavior of the structure, the basic transport equations are solved, as the potential at various electrodes is swept. Transient behavior is ignored, and only quasi-stationary solutions are used. Three equations are solved at each step of the simulation. They are Poisson's equation $\nabla \cdot \epsilon \nabla \phi = -q(p - n + N_D^+ - N_A^-)$, where ϵ is the material permittivity and ϕ refers to the electrostatic potential, the continuity equation for both electrons and holes $\pm \nabla \cdot \vec{J}_{n,p} = qR_{net} + q \frac{\partial n,p}{\partial t}$ with the positive term corresponding to n and the negative to p , as well as the quantum potential equations [12].

3. RESULTS AND DISCUSSION

Cubic Transistor Simulation

TCAD Synopsys Sentaurus is used to study the electrical properties of GaN HEMTs. We start with constructing the device geometry by defining the material, length, width, and thickness of each layer; the mole fraction of $\text{Al}_x\text{Ga}_{1-x}\text{N}$ layers; and contact dimensions. Also, the doping concentrations, trap types, and densities are specified. After the platform is created, we assign the physical parameters to be used for each material or layer. Because we use different Al compositions for different AlGa_xN layers, the properties are mole-fraction-dependent. These parameters include bandgap energy, mobility, saturation velocity, and polarization-related parameters, such as piezoelectric coefficients, spontaneous polarization, stiffness constants, and lattice constants.



Using these parameters, a set of equations is solved until the solutions converge. The piezoelectric and spontaneous polarization equations are combined to calculate the polarization charge. Poisson's equation is solved to calculate the potential in the device. Plugging in this potential to the drift-diffusion model, the electron and hole currents are evaluated. This sequence is repeated until the solutions are self-consistent. The numerical methods in solving these equations are also selected. Especially, for better convergence of simulations incorporating wide bandgap materials, the numerical accuracy needs to be enhanced due to the extremely low intrinsic carrier densities in these materials. Finally, the converged solutions obtained from the calculations are post-processed and visualized.

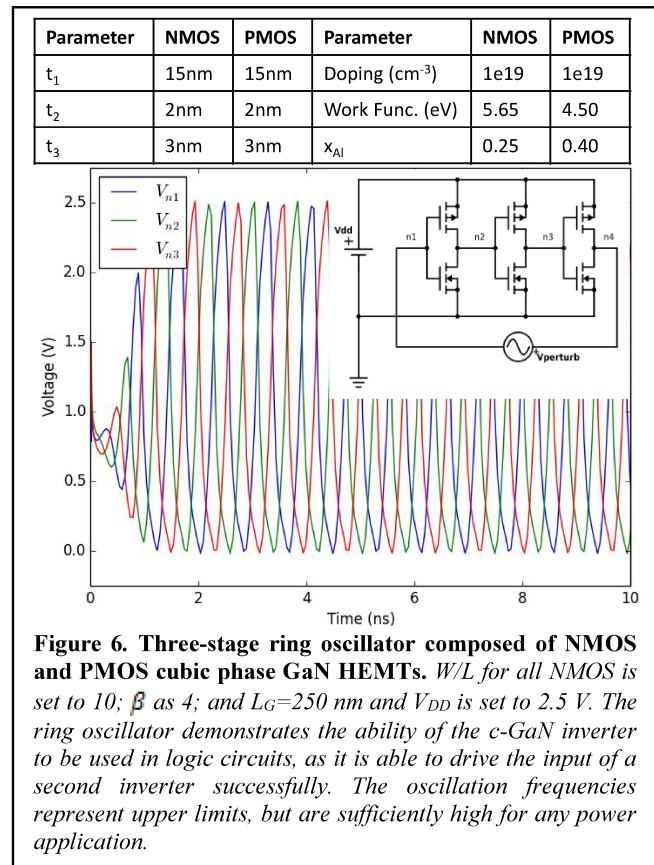
The results of c-phase $\text{Al}_x\text{Ga}_{(1-x)}\text{N}/\text{GaN}$ transistor simulation are shown in Figures 4 and 5. For the initial optimization, Al content in the $\text{Al}_x\text{Ga}_{(1-x)}\text{N}$ barrier (x_{Al}) is varied from 0.25 to 0.50; gate Schottky barrier height (ϕ_b) is varied from 1.2 to 2.0 eV; and $\text{AlGaIn}_{1,2,3}$ thicknesses are varied as t_1 from 13 to 16 nm, t_2 from 1 to 5 nm, and t_3 from 1 to 5 nm. As the $\text{Al}_x\text{Ga}_{1-x}\text{N}$ electron affinity (χ_s) changes with aluminum content according to Vegard's law, barrier height acts as a better experimental control, and thus we vary the gate Schottky barrier height (ϕ_b) (opposed to varying the work function of the gate metal [ϕ_M]). The effects of each variable $\{x_{\text{Al}}, \phi_b, t_1, t_2, t_3\}$ on HEMTs were studied, as each variable is varied independently. The criterion for normally off behavior is taken as 2DHG formation when the Fermi level is below the valence band minimum at the $\text{AlGaIn}-\text{GaN}$ heterointerface.

The value of h_s is of particular relevance in HEMT devices for power applications. It is directly related to the valence band offset, which is in turn influenced by x_{Al} . Based on this fact, h_s has been studied as a function of aluminum content and V_{GS} . The sheet density is calculated by integrating the carrier density along the depth, following the literature [16]. The sheet density is seen to scale with both aluminum content and gate bias. By further optimizing the parameters t_2 and δ -doping density, higher values of 2DHG density (h_s) ($> 2 \times 10^{13} \text{ cm}^{-2}$) should be attainable.

In summary, our investigation shows the p-channel operation regime of c-phase $\text{Al}_x\text{Ga}_{(1-x)}\text{N}/\text{GaN}$ HEMTs via varying key design parameters ($x_{\text{Al}}, t_1, t_2, t_3, \delta$ -doping amount, and ϕ_M). Particularly, we consider and study the tradeoffs between x_{Al}, t_1 , and ϕ_M (via its impact as ϕ_b) to maximize V_T and h_s . Considering Matthews-Blakeslee critical thickness, we offer design guidelines for maximizing V_T while minimizing defectivity in [13]. Our results are encouraging for the use of c-phase GaN HEMTs, given the wide-range tenability in V_T and n_s , for p-channel operation [13, 14].

Ring Oscillator Simulation

Recently, we have simulated a three-stage ring oscillator consisting of three inverters (each composed of a single NMOS and PMOS style cubic GaN transistor) using TCAD and HSPICE. First, we simulated an inverter consisting of a single NMOS and PMOS style cubic GaN transistor with respective values of $t_1, t_2, t_3, x_{\text{Al}}, N_D, N_A$, and ϕ_M as listed in Figure 6. We set supply voltage (V_{DD}) high enough to 2.5 V to assure more than the theoretical minimum supply voltage ($V_{\text{DD,min}} = V_{\text{Th}} + |V_{\text{Tp}}| = 1.61 \text{ V}$) and low enough to reduce the dynamic and static power consumption. We measured the average current drawn from the supply voltage when the gate output was high as 1.36 pA and calculated the static power consumption as 3.40 pW. Time-averaged current drawn from the supply voltage as the output transitioned from low to high became 3.5 mA and dynamic power consumption is calculated as 8.7 mW. Then, a three-stage ring oscillator composed of NMOS ($\mu_e = 1000 \text{ cm}^2/\text{V-s}$) and PMOS ($\mu_h = 250 \text{ cm}^2/\text{V-s}$) cubic phase GaN devices (with V_T of 0.77 V and -0.84 V , respectively) is simulated. We minimized the propagation delay by optimizing the width-to-length ratio (W/L) between the NMOS and PMOS devices. Both NMOS and PMOS gate lengths are set to 250 nm. The gate widths of NMOS and PMOS are optimized to be 2.5 μm (such that $\beta = (W/L)_{\text{PMOS}}/(W/L)_{\text{NMOS}} = 10$) and 10 μm (such that $\beta = 4$), respectively. The propagation



delay (t_p) of each stage of the ring oscillator was optimized by varying the gate width of the PMOS device and the minimum t_p is then 130 ps. Transient response of the simulation (Figure 6) illustrates the ability of the CMOS inverter to operate at a maximum frequency of 1.22 GHz with a full voltage swing between V_{DD} and 0 V.

4. CONCLUSION

We simulate a new kind of gallium nitride (GaN) high-electron-mobility transistor (HEMT) with **two-dimensional-hole-gas (2DHG) p-channel behavior** and provide fundamental new knowledge on **complementary logic circuits enabled by p- and n-channel GaN HEMTs**. Silicon-based transistors are reaching their limits as more applications (such as DC/DC power conversion, 5G networks) demand high-power and high-speed operation, motivating investigations of new materials and device structures. GaN HEMTs are ideal candidates for addressing emerging needs, particularly in high-power (>10 W), high-frequency (>10 GHz), high-ambient-temperature (> 200 °C) applications. *The challenge for conventional GaN HEMTs is the p-channel operation, which is necessary for complementary logic circuits.* Because of the inherent polarization fields in hexagonal (h-) phase GaN, conventional GaN HEMTs of h-phase are n-channel, meaning a conductive two-dimensional electron gas (2DEG) channel is formed in the AlGaIn/GaN heterointerface – even under no external bias. For complementary logic applications, 2DHG p-channel HEMTs are required. Several methods of implementing p-channel GaN HEMTs have been explored including inverted GaN/AlGaInN heterostructures and N-polar structures. However, p-channel devices enabled by these approaches rely on polarization doping which limits p-channel hole concentration and hole channel mobility. **Here, we report a new method for the creation of a p-channel GaN HEMT: Employment of the naturally polarization-free cubic (c-) phase and δ -doping technology.** This approach can also be used to create n-channel devices enabling complementary logic GaN HEMT applications on the very same platform. Additionally, the proposed research is scalable on a CMOS-compatible Si substrate so as to facilitate industrial adoption and generate new knowledge about GaN-Si hetero-integration. This new knowledge prompts novel p-channel and n-channel HEMT designs and concurrently enhances our understanding of advanced wide bandgap logic/power/RF electronics. Overall, the research results lead to concept of a p-channel cubic phase GaN HEMT and complementary metal-oxide-GaN transistor logic circuitry – both firsts amongst electronic devices.

This work is partially supported by the Independent Study Funds of Electrical and Computer Engineering Department, University of Illinois at Urbana-Champaign, IL, USA and partially by the National Science Foundation Faculty Early Career Development (CAREER) Program under award number NSF-ECCS-16-52871. This work was carried out in the Micro and Nanotechnology Laboratory, University of Illinois at Urbana-Champaign, IL, USA.

REFERENCES

- [1] Lee, H-P, Perozek, J., Rosario, L. N. D., Bayram, C., “Investigation of AlGaIn/GaN high electron mobility transistor structures on 200-mm silicon (111) substrates employing different buffer layer configurations,” *Sci. Rep.* **6**, 37588 (2016).
- [2] Chow, T. P., Tyagi, R., “Wide bandgap compound semiconductors for superior high-voltage unipolar power devices,” *IEEE Trans. Electron Devices*, **41**, 1481 (1994).
- [3] Lee, K.-T., Bayram, C., Piedra, D., Sprogis, E., Deligianni, H., Krishnan, B., Papasouliotis, G., Paranjpe, A., Aklimi, E., Shepard, K., Gallagher, W. J., Palacios, T., Sadana, D. K., “Heterogeneous Integration of GaN Devices on a 200 mm Si(100) Wafer via Scalable CMOS Technology,” *IEEE Electron Device Lett.* **38** 1094 - 1096 (2017).
- [4] Saito, W., Takada, Y., Kuraguchi, M., Tsuda, K., Omura, I., “Recessed-gate structure approach toward normally off high-Voltage AlGaIn/GaN HEMT for power electronics applications,” *IEEE Trans. on Electron Devices* **53**, 356 (2006).
- [5] Ishida, M., Ueda, T., Tanaka, T., Ueda, D., “GaN on Si Technologies for Power Switching Devices,” *IEEE Trans. Electron Devices*, **60** (10), 3053 (2013).
- [6] Hwang, I., Kim, J., Choi, H. S., Choi, H., Lee, J., Kim, K. Y., Park, J.-B., Lee, J. C., Ha, J., Oh, J., Shin, J., Chung, U.-I., “p-GaN Gate HEMTs With Tungsten Gate Metal for High Threshold Voltage and Low Gate Current,” *IEEE Electron Device Lett.* **34**, 202 (2013).
- [7] Shatalov, M., Simin, G., Zhang, J., Adivarahan, V., Koudymov, A., Pachipulusu, R., Khan, A. M. “GaN/AlGaIn p-channel inverted heterostructure JFET,” *IEEE Electron Device Lett.*, **23**, 452–454 (2002).
- [8] Zimmermann, T., Neuburger, M., Kunze, M., Daumiller, I., Denisenko, A., Dadgar, A., Krost, A., Kohn, E., “P-channel InGaIn-HFET structure based on polarization doping,” *IEEE Electron Device Lett.* **25**, 450–452 (2004).

- [9] Li, G., Wang, R., Song, B., Verma, J., Cao, Y., Ganguly, S., Verma, A., Guo, J., Xing H., Jena, D., “Polarization-Induced GaN-on-Insulator E/D Mode p-Channel Heterostructure FETs,” *IEEE Electron Device Lett.* **34**, 852–854 (2013).
- [10] Zhang, L., Ding, K., Yan, J. C., Wang, J. X., Zeng, Y. P., Wei, T. B., Li, Y. Y., Sun, B. J., Duan, R. F., Li, J. M., “Three-dimensional hole gas induced by polarization in (0001)-oriented metal-face III-nitride structure,” *Appl. Phys. Lett.* **97**, 062103 (2010).
- [11] Schroeder, D., [*Modelling of Interface Carrier Transport for Device Simulation*], Springer, (1994).
- [12] Sentaurus Device User Guide Version K-2015.6, Synopsys, Mountain View, CA, USA (2015).
- [13] Grady, R., Bayram, C., “Simulation of zincblende AlGaIn/GaN high electron mobility transistors for normally-off operation,” *J. Phys. D: Appl. Phys.* **50**, 265104 (2017).
- [14] Bayram, C., Grady, R., Park, K., “Normally-off Cubic Phase GaN Transistors and Method of Forming the Same,” US Patent Application Serial No 62/397,151, filed on September 20, 2017.
- [15] Varshni, Y. P., “Temperature dependence of the energy gap in semiconductors,” *Physica* **34**, 149-154 (1967).
- [16] Ambacher, O., Smart, J., Shealy, J. R., Weimann, N. G., Chu, K., Murphy, M., Schaff, W. J., Eastman, L. F., Dimitrov, R., Wittmer, L., Stutzmann, M., Rieger, W., Hilsenbeck, J., “Two-dimensional electron gases induced by spontaneous and piezoelectric polarization charges in N- and Ga-face AlGaIn/GaN heterostructures,” *J. Appl. Phys.* **85**, 3222 (1999).