Design and Implementation of a Series Resonant Solid State Transformer

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Abstract—The focus of this study is on the design of a full-bridge unidirectional resonant LLC Solid State Transformer. The proposed topology uses a high-frequency transformer to optimize the size and weight of the converter. This converter has the capability of operating at fluctuating load conditions while it keeps the voltage regulated in different operation point. The converter is designed to maintain soft switching by using a resonant circuit in this design to minimize the switching loss of the high frequency converter. ZVS in the leading leg for turn on mode and ZCS commutation in the lagging leg for all of the modes are achieved in the H-bridge through the suggested circuitry which is analyzed mathematically in detail in this study. A combination of Pulse frequency modulation (PFM) and Phase Shifting Modulation (PSM) are utilized to control this resonant converter. The experimental setup for the suggested configuration was implemented and the results of the simulation and calculations have been verified with test results. The hardware set up was tested with two different power levels and the output results confirm that the control method works properly to feed the load and keeps the converter working in the expected frequency range and maintaining the soft switching to decrease switching loss. The results shows conversion efficiency of 97.18% is achieved.

Keywords— Power electronic transformer, phase shift control, resonant solid state transformer, SST soft-switching, zero current switching, zero voltage switching.

I. INTRODUCTION

The concept of SST has been formulated by several researchers since late 1990s [1-3]. In this concept, a combination of power electronic converters and high- or medium-frequency transformers forms a converter to connect two systems with different voltage levels and types (AC or DC). If active converters are used for both SST ends, the power flow can be bi-directional. Since a medium- or high-frequency transformer provides galvanic isolation, the size and cost of the SST is generally much less than the conventional isolated converters with the same voltage and power rating (1) [14], [15].

$$W_a A_c = \left(\frac{I S x 10^4}{K_f K_{cu} K_j f B_{pk}} \right)^{1.16} \qquad (1)$$

W_a is the window area, A_c is the cross-sectional core area, K_f relates rms voltage to volt-seconds, K_j relates area product to current density, f is the switching frequency and B_{pk} is the peak flux density in the core.

SSTs can be used to offer several functionalities in a smart grid configuration including (i) protecting loads from power system disturbances, (ii) protecting power system from load disturbances, (iii) integrating energy storage systems (energy buffer), (iv) providing DC ports for distributed generation connection, and (v) supporting voltage and power profiles. On the other hand, SSTs can play an important role in realizing the next-generation integrated power system. They will link the micro-grids to the MV transmission system as well as low voltage AC and low voltage DC systems [4-10].

One of the main concerns in realizing SST topologies is high switching loss in multiple high frequency conversion stages. Applying resonant behavior to these topologies can significantly improve the efficiency of the converter. Several researches have been published on the techniques to add resonant circuit to the SST configuration. Jung et al. (2013) described a CLLC topology for a bidirectional SST for DG interface [11]. A complex dead-band control at sub resonant frequency is used and the switching frequency is limited at the resonant frequency. Agamy and Jain (2008) explained a three-level resonant single-stage PFC converter which is suitable for high power applications [12]. Variable frequency phase shifted modulation (VFPSM) is used in [12], and switching frequency is limited above resonant frequency to achieve ZVS, whereas ZCS operation is not targeted in this work.

In this paper, a series resonant SST topology is developed, designed, implemented and tested which promises higher efficiency than existing systems. The resonance feature is achieved by adding a series capacitor on the high frequency link. The switching frequency can change from under half of resonant frequency to super resonant frequency.
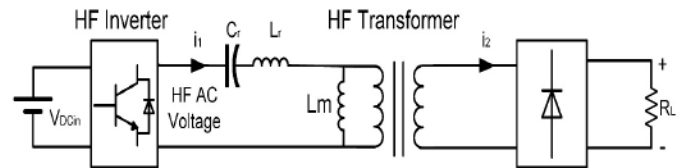

Figure 1: Resonant Solid State Transformer configuration.

A combination of Pulsed Frequency Modulation (PFM) and Phase Shifting Modulation (PSM) is used to regulate the voltage.

The leakage inductance of the transformer has been set by adjusting the space between winding layers to match the inductance required for resonant circuit. The topology of the proposed SST is depicted in Figure 1.

II. CIRCUIT ANALYSIS FOR THE RESONANT SST

The LLC resonant network acts as a filter for the square wave voltage seen at the terminals of the full-bridge converter. This results in a pseudo sinusoidal current seen at the primary side of the transformer. The detailed circuit representation of the proposed topology is presented in Fig.2 . In most common modes of operation, the controlled switch network produces a square wave voltage output V_d whose frequency is close to the tank network resonant frequency. The tank output waveform is then rectified to produce the DC load voltage V_o. The magnitude of the tank ringing responses can be modified by changing the switching frequency f_s to change the DC output voltage. In this case, the resonant tank responds primarily to the fundamental component (f_s) of the switch waveform V_s, and has negligible response at the harmonic frequencies $(2n+1)*fs$, n=3, 5, 7 ... [13]. First Harmonic Approximation (FHA) is used to obtain the transfer function that describes the gain of the resonant network. The resulting circuit for FHA analysis is shown in

The input of the resonant network is a square wave varying between $-V_d$ and $+V_d$. Using Fourier series, the input voltage can be expressed by Equation (2) [11].

$$V_d(t) = \frac{4V_d}{\pi} \sum_{n=1,3,5,.}^{\infty} \frac{1}{n} Sin(2\pi n f_s t) \tag{2}$$

Where f_s is the switching frequency of the switches in the resonant network. The fundamental component of $v_d(t)$ can be obtained using the FHA analysis. The fundamental component, $v_{d,FHA}(t)$, is then can be obtained as:

$$V_{d,FHA} = (2\sqrt{2}/\pi) V_d \tag{3}$$

Equation (3) does not take into account a varying phase shift between the two legs of the inverter. If this phase shift is represented by angle 'a', the output voltage of the inverter can be written as:

$$(V_O)_h = \frac{4}{nh\pi} V_d Cos(\frac{1}{2} a) \tag{4}$$

The effective output load resistance seen in parallel with the magnetizing inductance Lm is defined as Re. This accounts for the turn's ratio of the transformer and the output load. Using FHA leads to write Re as follows:

$$R_e = \frac{8}{\pi^2} R_O \tag{5}$$

The transfer function of the resonant network, defined as the ratio of the output voltage over the input voltage as shown in Equation (6).

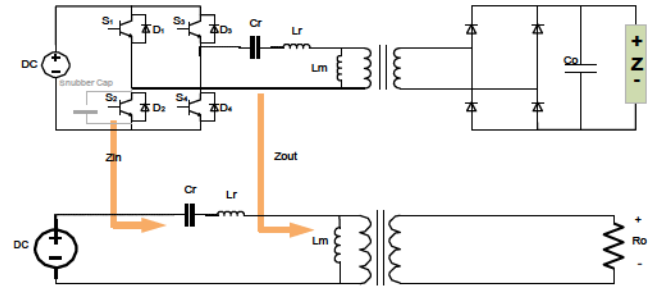Figure 2: Detailed circuit of proposed SST & LLC resonant converter using FHA analysis.

$$H_r = \frac{V_{O,FHA}}{V_{d,FHA}} = \frac{sL_m + R_e}{(sC_r)^{-1}+sL_r+\frac{sL_m+R_e}{sL_m+R_e}} \tag{6}$$

The normalized frequency "f_n" can be written in terms of the switching frequency "fs" and the first resonant frequency "f_r" as follows:

$$f_n = \frac{f_s}{f_r} \tag{7}$$

Where

$$f_r = \frac{1}{2\pi\sqrt{L_rC_r}} \tag{8}$$

The quality factor "Q" and the inductance ratio "k" are given by:

$$Q = \frac{Z_r}{R_e} \qquad Z_r = \sqrt{\frac{L_r}{C_r}} \qquad k = \frac{L_r}{L_m} \tag{9}$$

Using the above terms, H_r can be reformulated as follows:

$$H_r = \frac{\frac{jf_n}{k}}{\frac{Q f_n^2 Q}{k} - \frac{Q}{k} +j[f_n+\frac{f_n}{k} - \frac{1}{f_n}]} \tag{10}$$

The magnitude of H_r is obtained and evaluated at $(j2\pi f_s)$ as follows:

$$|H_r| = \left| \frac{\frac{jf_n}{k}}{\frac{Q f_n Q}{k} - \frac{Q}{k} +j[f_n+\frac{f_n}{k} - \frac{1}{f_n}]} \right| \tag{11}$$

a) Circuit Analysis:

Various series-loaded-resonant (SLR) and parallel-loaded resonant (PLR) converter topologies are readily available. In this study, a topology that could offer advantages from both topologies (SLR and PLR), is presented by forming a series-parallel converter operating in super-resonance CCM mode.

LLC resonant converters that are operated above the resonant frequency show many advantages including, but not limited to: inherent short-circuit protection, zero voltage commutations, limited harmonics in the resonant current, maximum power transfer at minimum switching frequency and transformer leakage inductance included in the resonant link [16].

The proposed resonant converter is operated using Pulse Frequency Modulation (PFM) and Phase Shift Modulation (PSM). It is operated by turning off one set of the H-bridge leg earlier than the other set. The imposed phase shift between the two legs creates three different levels on the output of the inverter: +Vi, -Vi, and 0. Thus, there is a discontinuity in the current every half period, which results in DCM operation at super resonant frequency.

The design aims to insure ZVS and/or ZCS operation of the converter at different load conditions. The converter is operated under varying switching frequency and phase shift between the legs of the H-bridge. It results in ZCS for the lagging leg across full load range. As for the leading leg, ZVS operation at turn on is achieved for all switches.

The ZVS operation of the switches on the primary side of the converter (leading leg) is very important for minimizing losses and stress. Adding a snubber capacitor in parallel with the 2nd switch (Fig. 2) the ZVC is obtained for the leading lag. The snubber capacitor maintains the bus voltage during the turn off transition and keeps the potential difference on the switch to zero for turning it on.

b) Gain Curve Analysis:

The gain curve of the resonant converter can be plotted using the following Equation (12):

$$IH_r I = \cfrac{\frac{f_n}{k}}{\sqrt{\left[\frac{Q}{\kappa} - \frac{f_n^2 Q}{k}\right]^2 + \left[f_n + \frac{f_n}{k} - \frac{1}{f_n}\right]^2}} \tag{12}$$

There are two resonant frequencies f_{r1} and f_{r2} in Fig. 3. The frequencies are the result of L_r and the combined inductances L_r and L_m, respectively. The gain of the resonant converter has to be monotonically decreasing within the operating frequency range. Taking the derivative of Equation (12) and setting it to less than zero, the following inequality is obtained:

$$Q < \sqrt{\frac{B(f_n)}{A(f_n)}} \tag{13}$$

Where $A(f_n)$ and $B(f_n)$ are given as follows:

$$A(f_n) = f_n^4 \left(\frac{-1}{2k^2}\right) + f_n^2 \left(\frac{-1}{2k}\right) + \frac{1}{k^2} \tag{14}$$

$$B(f_n) = f_n \left(\frac{1}{k^2} + \frac{1}{k} - \frac{2-2k}{2} + \frac{3}{2}\right) + \left(\frac{3}{k}\right) + \frac{3}{2f_n^2} \tag{15}$$

R_o can be expressed as a function of the output voltage and output current. Using the condition obtained in (14), a condition for the maximum load current, $I_{o,max}$, can be derived as follows:

$$I_{o,max} < \frac{8V_o Q_{max}}{n^2 Z_r} \tag{16}$$

Alternatively, a condition for maximum Z_r at a given $I_{o,max}$ can be derived:

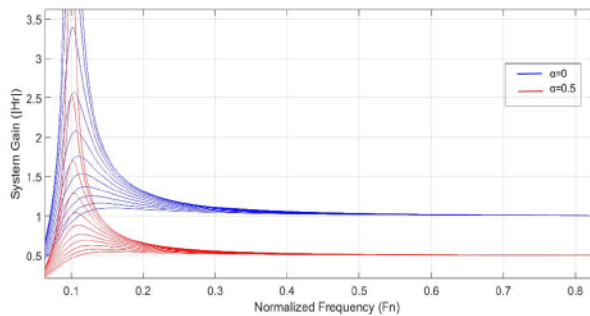$$Z_r < \frac{8V_o Q_{max}}{n^2 I_{o,max}} \tag{17}$$

Figure 3: Resonant converter gain plot versus normalized frequency at various values of Q (increments of 0.01) for two values of Alpha

III. CONTROLS

It is extremely important to maintain a regulated output DC voltage to support a varying load requirement. A combination of two control schemes, PSM and PFM, is utilized to control the converter. PFM is applied by varying the switching frequency fs to adjust the point of operation on the gain curve (Figure 3). PSM is then implemented by adjusting the duty ratio of S_3 and S_4 in order to increase or decrease the overlap between the two leg's voltages. This overlap, described as the angle "a", corresponds to a zero state (zero voltage) seen at the terminals of the inverter.

Using both PFM and PSM, it is possible to support a wider range of load. Adjusting duty cycle enables holding to a specific switching frequency for a varying load. Alternately, the converter can be operated at lower switching frequencies for lower duty cycles for a fixed load. Figure. 4 shows a plot of fs vs duty ratio for two different load requirements that are fixed at 18A and 20A. In this case, decreasing both fs and duty ratio permits the controller to support a fixed load requirement and regulate a specific desired voltage level. Figure. 5 shows that a wider range of output voltage is realized when both PFM and PSM are used.

Conventionally, a converter that uses PFM would have a fixed gain curve (for a fixed load). In Fig. 5, the whole dotted area between the upper and the lower curves that correspond to duty ratio of 1 and 0.1 represents possible points of operation. The emulation of the circuit and the controller was performed using MATLAB/Simulink and PLECS. Simulink was used to build the controller and generate the gate signals G1 through
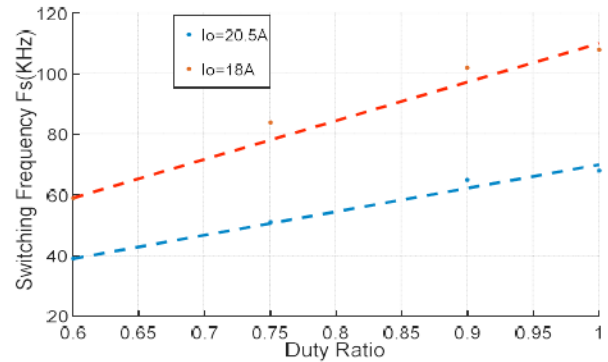
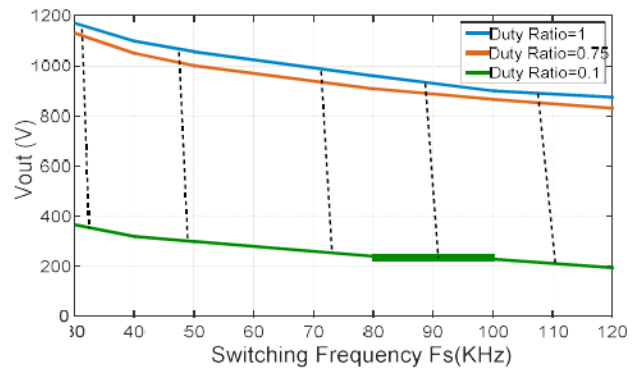Figure 4. Switching frequency versus duty ratio

Figure 5. V_{out} at different duty ratios for a spectrum of f_s.

G4. PLECS was used to simulate the SST and look at the switching transients of the four switching devices.

Table 1 summarizes the parameters used in the simulation. PI_1 and PI_2 correspond to the two PI controllers in the PSM and PFM control loops, respectively. The selection of these parameters guarantees that a switching frequency f_s of 30 kHz is above the resonant frequency of the system. In addition, the selection of the magnetizing inductance.

TABLE 1: SIMULATION PARAMETERS

Lr	10 µH
Lm	200-300 µH
Cr	4 µF
$Cout$	1000 uF
PI_1	Kp=1; Ki=0.0001
PI_2	Kp=0.4 ; Ki=20
V_{in}	700 V

IV. SIMULATION AND EXPERIMENTAL ANALYSIS:

The disturbance response of the controller was tested by changing the output load from high to low. The output voltage is regulated at 1000 V. Looking at Figure 3, operating above f_{r2} implies that increasing f_s decreases the gain of the converter. Therefore, the PFM controller reacts to the event of a sudden decrease of the load by increasing the switching
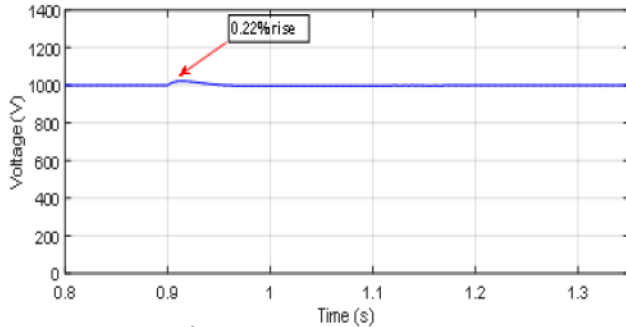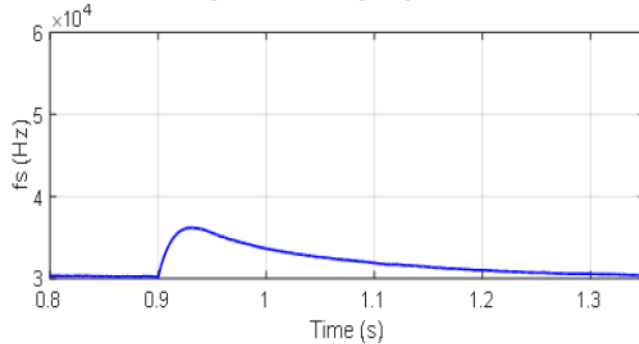

Figure 6. Load voltage response
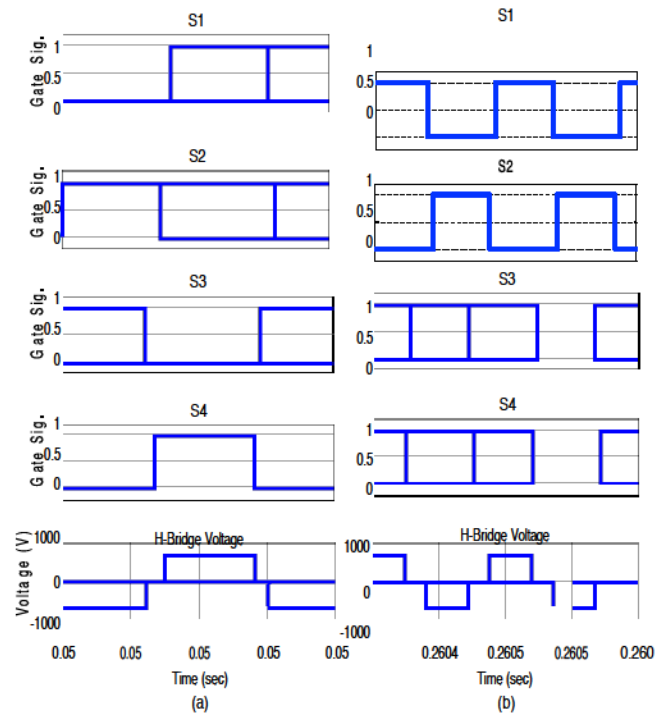

Figure 7. Switching frequency response.

Figure 8. H-bridge output voltage: a) High load b) Low load

frequency fs to reach a point on the gain curve that matches the required output voltage. As the switching frequency increases, the PSM controller increases the phase shift a. This results in a decrease in the switching frequency, and by selecting f_{ref}, it is possible to operate at different points. Figure 6 shows the load voltage at the described event of load change. The change in f_s is shown in Fig. 7. The output voltage of the H-bridge at high and low load is shown in Fig. 8. The angle of phase shift a can be noticed by looking at the gate signals of switches S_3 and S_4. Comparing Fig. 8 (a) to Fig. 8 (b), the phase shift is larger in the case of smaller load.

V. EXPERIMENTAL RESULTS

The series resonant solid state transformer introduced in this study has been designed and assembled to verify the results through lab tests. Figure 10 shows the primary results of the test. Soft start was used to ramp up the output voltage from 0 to the set reference. The converter was run to give 1000 V DC at the output. The yellow (upper) curve shows the output DC which the converter regulates properly. The purple curve is the gate signal and the green (lower) curve is the primary ac current of the HF transformer. Figure. 11 shows the startup waveforms of the converter where pulses of current were applied for very short periods of time. In the next test, (Fig. 12), the load power is low and consumes only 15kW. The SST can handle up to 150kW. In the last test the converter was almost close to its nominal power rating and it is evident by looking at the terminal voltage of the inverter (purple) square wave signal. Phase shifting in this case is minimum and the controller takes advantage of most of the duty cycle. Therefore, the converter meets the power demand by increasing the duty cycle and decreasing the switching frequency, while maintaining soft switching. Comparing the results of low and high load test it

can be seen that the more load power, the bigger duty ratio, and the current waveform is more sinusoidal.
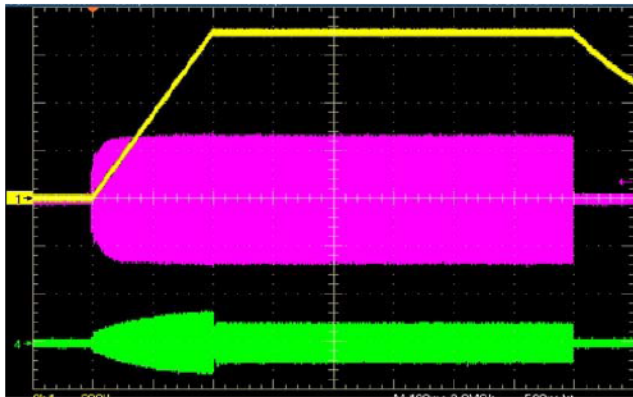

Figure 9. Output DC, gate signal and HF Primary current of the SST showing startup to steady state duration.
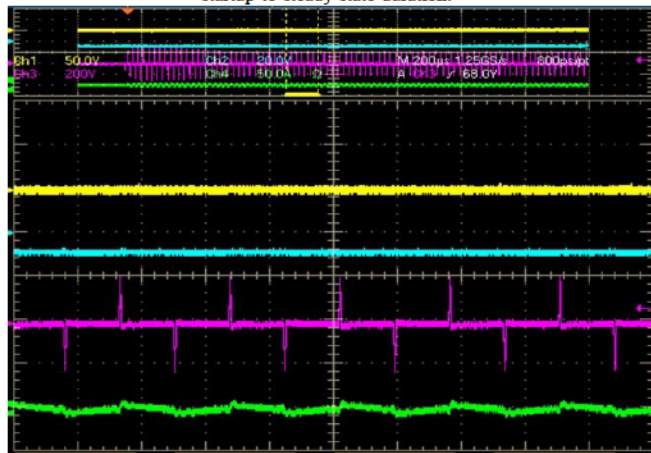

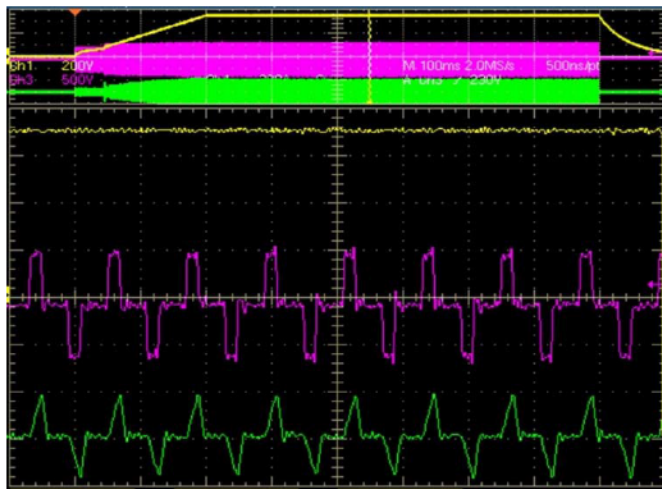Figure 10. Converter test results during startup.

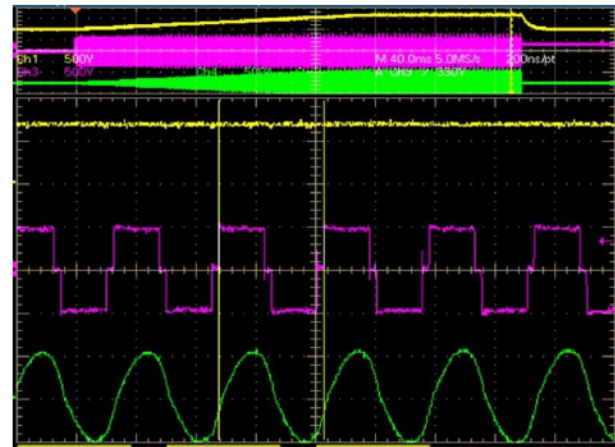Figure 11. Converter test results for low power load of 15kW.

Figure 12. Converter test results for high power load of 140kW.

V. CONCLUSIONS

In this research study, a new control structure has been presented and tested for an LLC resonant SST. The discussed topology has several advantages compared to conventional topologies that rely only on transformers or power electronics circuitries. It provides load regulation, power flow control, and galvanic isolation. Soft-commutation has been achieved by adding a resonant tank and designing its parameters. A mathematical analysis was conducted to obtain the transfer function of the converter which used to plot the gain curve of the converter. Design considerations and limitations for various parameters of the system were discussed in detail. The proposed controller adjusts the output voltage of the SST by varying the switching frequency f_s and the phase shift a between the two legs of the H-bridge. Having two parallel loops on the controller for each of f_s and a, the SST can be set to operate around a desired switching frequency instead of having no control on its value in conventional PFM controllers. Simulation results using Simulink and PLECS were presented in detail for this research study, along with experimental testing which complies with the simulation.

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