A Method for Open-Circuit Faults Detecting, Identifying, and Isolating in Cascaded H-Bridge Multilevel Inverters

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Abstract — **The increasing importance of power electronic converters in supplying electrical energy to utility grids places a higher priority to detect and protect against fault conditions. Fault detection and isolation are particularly important for inverters that provide black-start recovery for microgrids since these converters provide the energy source for restoration after a power outage. This paper presents a new fault detection and location method for Cascaded H-Bridge (CHB) multilevel inverters. The new fault detection method is based on monitoring the output voltage of each cell and output current directions along with each switch's state. By monitoring each cell's output voltage and current direction, the faulty cell can be detected and isolated. After the faulty cell is detected, the faulty switch can be located by comparing the current direction with the switching states. This technique is implemented with Level-Shifted Pulse Width Modulation (LS-PWM) in order to maintain acceptable total harmonic distortion (THD) levels at the converter. The proposed method can be implemented for a CHB with any number of cells, can operate with nonlinear loads, and offers very fast detection times. Simulation and experimental results verify the performance of this method.**

Keywords— Cascaded H-Bridge, with Level-Shifted Pulse Width Modulation (LS-PWM), Modular Multilevel Converters (MMCs).

I. INTRODUCTION

Power electronic converters are increasingly used in electric power delivery systems due to the accelerated adoption of renewable energy sources such as solar photovoltaics and wind turbine generators. For microgrid systems, the use of distributed energy resources (DER) presents challenges for ensuring system resiliency [1]. Battery energy storage has been investigated for assisting in outage recovery [2]. Consequently, power electronic converters used for enhanced system resiliency need to have high levels of fault detection and isolation capabilities in order to provide electrical power reliably during outage recovery operations.

Multilevel converters have become one of the most attractive topologies in power electronic applications due to their effective performance and high output waveform quality. There are several types of multilevel converters presently in use. Examples include the flying capacitor, neutral point clamped (NPC) and cascaded H-bridge (CHB) modular multilevel converter topologies.

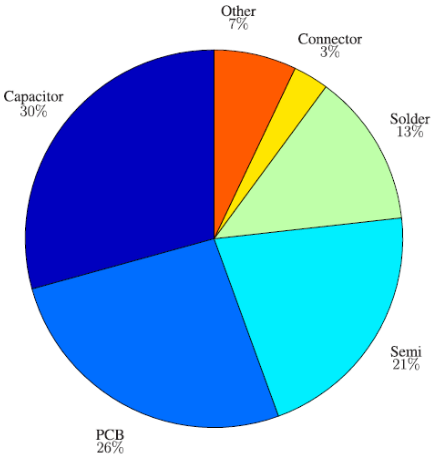

Fig. 1. Distributions of faults in power converters [7]

The CHB multilevel inverter is the most suitable for battery energy storage systems (BESS) in medium-voltage distribution system applications [3]. The possibility of device faults is great since multilevel topologies have a large number of power semiconductors devices.

Different kinds of electric component failures can cause a fault in a power electronic converter and anyone can lead to overall system failure. The components that may cause failures are capacitors, semiconductor devices, soldered joints, connectors, and PCB boards. The percentage of the faults occurrence vary for each component. According to [4]-[5], 52% of the faults in power electronics can be occurred in soldered joints, connectors, and PCB boards. Moreover, 21% of the power electronic failures occurred in semiconductor devices. A survey in [6] at more than 60 companies concluded that the semiconductor power devices are the most fragile components in power electronics representing 31% of the failures.

There are two kinds of device faults that could happen in power electronic applications; short- and open-circuit faults [8]-[9]. The development of methods to detect short-circuit faults have been provided with hardware circuits that are

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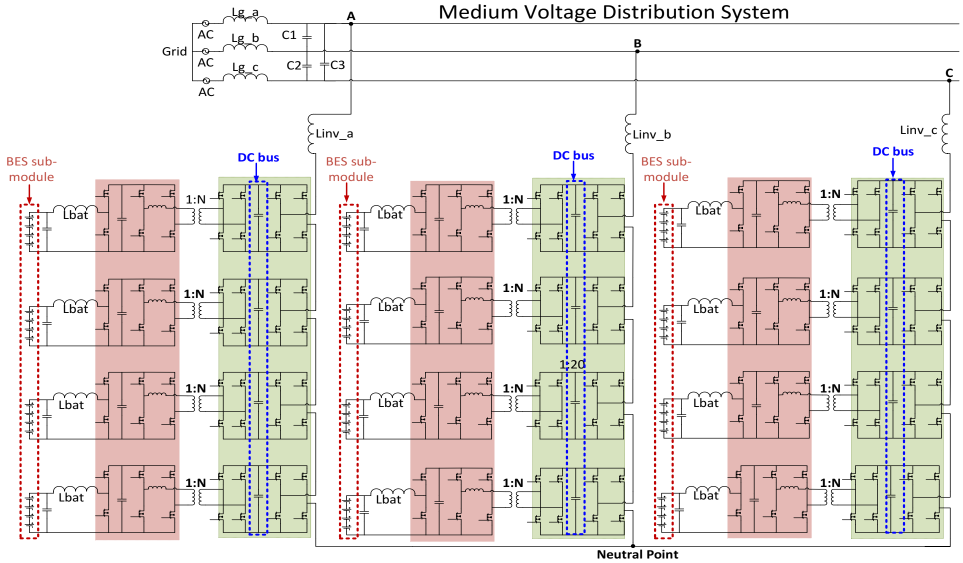


Fig. 2. A nine-level CHB with high gain dc/dc converter integration [23]

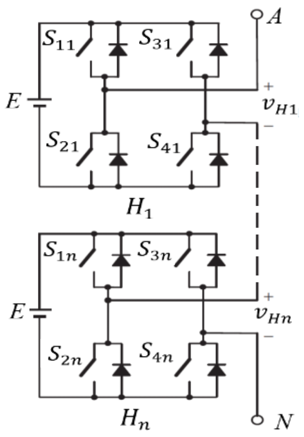


Fig. 3: *n*-level CHB multilevel inverter

integrated with commercial gate drivers to shut-down the device immediately when a short-circuit fault is detected [10]. However, there is no hardware solution to detect open-circuit faults. Open-circuit device faults can be caused by wire bond lift off, and cracking of solder layers [11]. Gate driver's faults can also result in an open-circuit fault. According to [6], around 15% of the power electronic failures is associated with gate drivers.

As the number of cells increases, the probability of a faulty switch also increases and this results in reliability issues. In BESSs, an open-circuit device fault in the CHB results in unbalanced output voltage and current. This may lead to an overall shutdown of the system supplied by the converter and potentially resulting in an expensive downtime situation for commercial and/or industrial loads.

To overcome the reliability concerns for an open-device fault occurrence, there is a need for a fast, simple and accurate fault detection method. Previous results given in [12]-[13] can detect the CHB cell fault, but not the exact faulty device. Therefore, it does not result in sufficiently accurate detection performance. Other works given in [14]-[15] require two cycles of the fundamental frequency to detect an open-circuit device. The complexity of the detection methods and sensing parameters can affect the detection time and may decrease overall reliability. The method in [16] characterizes the voltage pole and its duration time for NPC. The fault condition can be detected but not the faulty switch. The detection method in [17] compares the measured and estimated state values for a modular multilevel converter (MMC). However, it cannot detect the faulty switch despite detecting the fault submodule in about 44 ms. The method in [18] is not suitable for nonlinear loads because it depends upon the output voltage measured during the fault. This method results in reduced accuracy since there are no other parameters to compare other than the measured output voltage.

A method based on a sliding-mode observer was presented in [19] to detect the faulty switch in an eight-cell MMC. The method measures the cell capacitor voltage and each voltage leg independently from the operation frequency. However; the detection mode requires 200 ms to test the operation of each healthy cells. In [20], an open-circuit fault detection of a CHB is implemented using artificial-intelligence-based techniques. The faulty switch can be detected by monitoring the output voltage of the CHB. This method requires a large training data time to cover the operation region, resulting in inaccurate results. In [21], the proposed method successfully identified the faulty switches for a NPC feeding an asynchronous motor drive, but required more current sensors in each of the NPC leg.

Another method to detect an open-circuit fault is the neutral shift method described in [22]. That is suitable for phase-shifted PWM (PS-PWM). In the case of LS-PWM, it would result in less accurate performance. Therefore, there is a need for a method that has: 1) low implementation cost, 2) very high accuracy, and 3) fast response times.

This paper proposes an open-circuit fault detection method for cascaded H-Bridge inverters. The proposed method allows to detect the faulty switch without implementing additional sensors. It takes advantage of the available sensors in the topology. The basic operation of this method is based on comparing the switching states, the current and the voltage to ensure more accuracy. The simulation and experimental results validate the successful operation and performance of the proposed method. This paper is organized as follows. The system description of the CHB, and more details about the proposed method including the open-circuit cell detection, and identification of the failed device location is presented in Section II. Then, the simulation and experimental results for the proposed methods are given in Section III and Section IV, respectively. Finally, conclusions are given in Section V.

II. SYSYTEM DESCROPTION

A three-phase nine-level CBH inverter topology is selected to study the proposed open-circuit fault method; the same one as in [23] and displayed in Fig. 2. Each phase consist of four H-bridge cells and their independent dc power supplies. The purposes of the dc/dc converter are to step the voltage up and to regulate current. The focus of this research is proving the feasibility of proposed method, so a five level-CHB has been implemented. For simplification purposes, a single-phase CHB inverter having *n* cells is shown in Fig. 3. Each cell consists of a dc voltage source, *E*, and four devices. The output voltage of each CHB cell is from v_{H1} to v_{Hn}, and could be equal to *–E, 0,* or *E.* The output voltage of a single phase CHB multilevel inverter (V_{AN}) is the sum of all v_{H1} to v_{Hn}.

A. *Open-Circuit Fault Cell Detection*

The output voltage and current are less than the expected values if there is an open-circuit device fault. Since the faulty device acts as a diode the cell output voltage for the faulty device, due to the antiparallel diode, does not produce the desired voltage. By knowing the relationship between the cell output voltage and the current direction, the faulty cell can be detected. The possible faulty cells for a five-level CHB are listed in Table I.

If the output voltage is less than the expected voltage, then this indicates that there is a fault in one of the devices. The possible faulty cells and devices for a five-level CHB can be determined by the following:

Case 1) When $i > 0$, and $v_{H1} < 0$, there are two possible faulty devices, which are (S_{11} and S_{41}). In this case, cell $H1$ is detected as a faulty cell.

Case 2) When $i < 0$, and $v_{H1} > 0$, there are also two possible faulty devices, which are (S_{21} and S_{31}). In this case, cell $H1$ is detected as a faulty cell.

Case 3) When $i > 0$, and $v_{H2} < 0$, there are two possible faulty devices, which correspond to (S_{12} and S_{42}). In this case, cell $H2$ is detected as a faulty cell.

Case 4) When $i < 0$, and $v_{H2} > 0$, there are two possible faulty devices (S_{22} and S_{32}). In this case, cell $H2$ is detected as a faulty cell.

B. *Identification of the Failed Device Location*

Once the faulty cell is detected, the LS-PWM is tested to identify the exact device that has failed and the subsequent isolation process. The relationship between the faulty device and switching states are based on the previous cases as follows:

Case a) Since there are two possible faulty devices, (S_{11} and S_{41}), S_{41} is chosen. If S_{41} is ON and $i > 0$, and $v_{H1} \leq 0$, then the faulty device is S_{11}. Otherwise, the faulty device is S_{41}. In other words, when $i > 0$, v_{H1} is zero when S_{41} is OFF and v_{H1} less than or equal to zero in case S_{41} is ON.

TABLE I. Relationship between cell fault detection and current direction under an open circuit fault

	Current Direction	v_{H1}	v_{H2}	**Faulty Cell**	**Possible Faulty Switches**
Case 1	$i > 0$	<0	v_{H2}	$H1$	S_{11}, S_{41}
Case 2	$i < 0$	>0	v_{H2}	$H1$	S_{21}, S_{31}
Case 3	$i > 0$	v_{H1}	>0	$H2$	S_{12} , S_{42}
Case 4	$i < 0$	v_{H1}	<0	$H2$	S_{22}, S_{32}

Case b) During this case, S_{21} is monitored and compared to i and v_{H1}. If $v_{H1} \geq 0$ when $i < 0$, and S_{21} is ON, the faulty device is S_{31}. Otherwise, it should be S_{21}.

Case c) If the condition in case 3 happens, the S_{42} state is compared with v_{H2}. When S_{42} is ON and $v_{H2} \leq 0$, then S_{12} is located as the faulty device. Otherwise, S_{42} has the open circuit fault.

Case d) S_{22} is selected for this case to locate the faulty device. If $v_{H2} \geq 0$ when S_{22} is ON, then S_{32} is the faulty device. Otherwise, S_{22} has the open circuit fault.

This algorithm is valid for an unlimited number of CHB cells. Consider the number of H-bridge cells is *n*, and *x* as the H-bridge switches (*x* = 1, 2, 3, and 4) to generalize the algorithm. S_{xn} is the switching state for any H-bridge cell and device. Therefore, the previous four cases can be written as:

i) If $i > 0$, and $v_{Hn} < 0$, the PWM signal for S_{4n} is the monitoring device. If the S_{4n} is ON and $v_{Hn} \leq 0$ then S_{1n} has an open-circuit fault. Otherwise, S_{4n} is the faulty device. The condition for this case can be written as:

$$\sum_{i=1}^{N} S_{4n} V_{Hn} \leq 0 \tag{1}$$

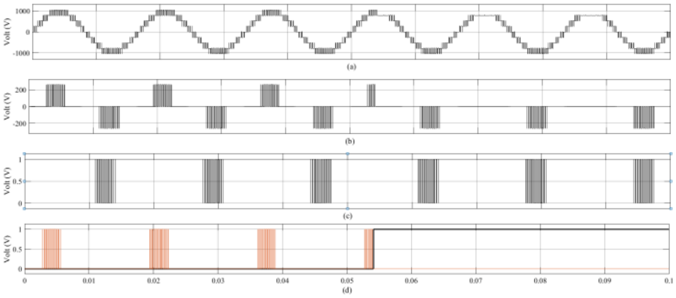


Fig. 4. Simulation results of an open-circuit fault switch on S_{11} at t = 0.054 s, (a) the output voltage; (b) output voltage of *H*1; (c) PWM signal of S_{41}; and (d) S_{11} (red) and the fault detection signal (black).

ii) If $i < 0$, and $v_{Hn} > 0$, the switching state S_{2n} is the monitoring device. If the S_{2n} is ON and $v_{Hn} \geq 0$ then S_{3n} has an open circuit fault. Otherwise, S_{2n} is the faulty device. This case can be expressed as:

$$\sum_{i=1}^{N} S_{2n} V_{Hn} \geq 0 \tag{2}$$

III. SIMULATION RESULTS OF THE PROPOSED DETECTION ALGORITHM

A detailed MATLAB/Simulink^{TM} model was developed to examine the performance of the proposed fault detection method. As a first example, an open-circuit fault has been applied to the nine-level CHB inverter. The simulation results in Fig. 4 verify the fault condition as in Case 1; the inverter is in normal operation and all the signals are as expected, V_{AN} in Fig. 4(a), v_{H1} in Fig. 4(b), and PWM for S_{41}in Fig. 4(c), and PWM for S_{11} (red) and the fault detection signal (black) in Fig. 4(d). However, as shown on Fig. 4(d), suddenly a gate misfiring fault occurs (PWM for S_{11} becomes zero), which results in an open-circuit fault at time, t = 0.054 s. Thus, v_{H1} becomes only either negative or zero, which verifies the identification method described as Case 1 in the previous section. The controller sends a command to isolate the faulty cell upon detecting the fault.

IV. EXPERIMENTAL VERIFICATION OF THE PROPOSED DETECTION ALGORITHM

A five-level CHB inverter, having two H-bridge cells, has been built using SiC MOSFETs as shown in Fig. 5 to validate experimentally the proposed method for detecting open-circuit faults. MicroAutoBox dSPACE has been used to generate the LS-PWM as shown in Fig. 6. The open-circuit faults have been generated assuming gate misfiring faults. Results in Figs. 7 and 8 show the PWM signals of S_{14} and S_{24}, output voltages of cell 1 and cell 2 (v_{H1} and v_{H2}), and the output current, respectively, under normal and fault operations. The experimental results, where (1) and (2) can be applied, verify successful fault detection and isolation for Case 1 (Fig.7) and Case 3 (Fig. 8). Fig. 7(b) shows Case 1 with S_{41} ON and $i > 0$, and $v_{H1} \leq 0$, then the faulty device is S_{11}. In Fig. 8(b), $i > 0$, and $v_{H2} \leq 0$, and S_{42} is ON, then S_{12} is identified as the faulty switch. Fig. 9 shows an open fault on S_{11}; PWM signal of S_{41} (ch1), output voltages of cell 1 (v_{H1}), and fault detection control signals of Case 1.

V. CONCLUSIONS

This paper presented a new method for open-circuit fault detection in a CHB inverter. Simulation and experimental results confirmed the relation between the current, CHB voltage cell, and the switching state. This method was shown to be: 1) Straightforward to implement due to its simple algorithm, 2) accurate for detection and location of the fault within one cycle, and 3) applicable to an unlimited number of CHB cells.

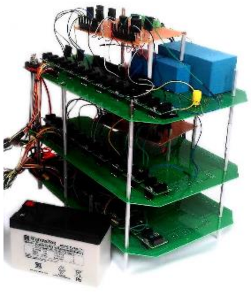


Fig. 5. Five-level CHB

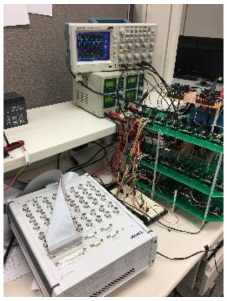
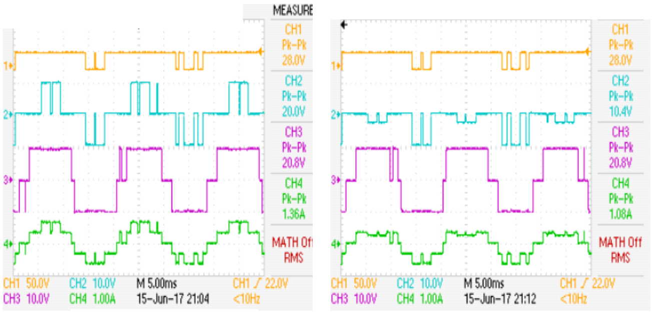
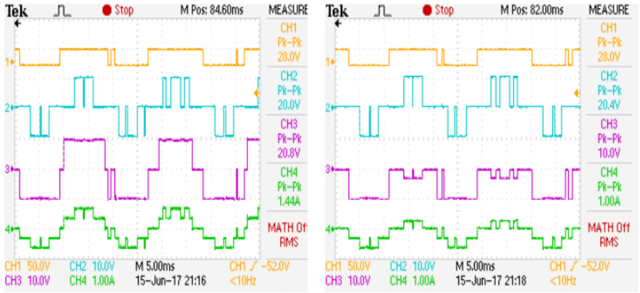


Fig. 6. Low-voltage verification



(a) (b)

Fig. 7. PWM signal of S_{41} (ch1), v_{H1} (ch2), v_{H2} (ch3), and output current (ch4). (a) Normal operation. (b) An open fault on S_{11}.



(a) (b)

Fig. 8. PWM signal of S_{42} (ch1), v_{H1} (ch2), v_{H2} (ch3), and output current (ch4). (a) Normal operation. (b) Fault on S_{12}.

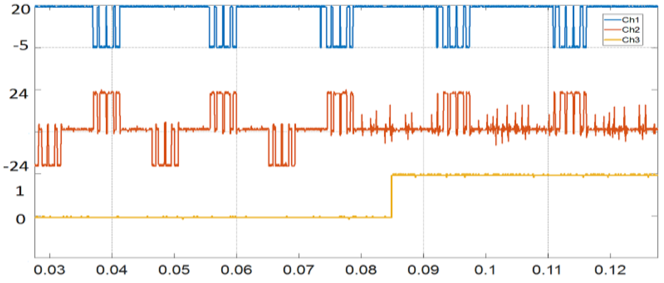


Fig. 9. An open fault on S_{11}; PWM signal of S_{41} (ch1), v_{H1} (ch2), and fault detection control signals (ch3)

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