Evaluation of 1.2 kV SiC MOSFETs in Modular Multilevel Cascaded H-Bridge Three-Phase Inverter for Medium Voltage Grid Applications

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***Abstract*—This paper describes a study evaluating 1.2 kV SiC MOSFETs in modular multilevel cascaded H-bridge (CHB) three-phase inverter for medium voltage ac grid applications. The main purpose of this topology is to remove the need of a bulk 60 Hz transformer that is normally used to step up the output signal of a voltage source inverter to the medium voltage level. Using SiC devices (1.2 kV ~ 6.5 kV SiC MOSFETs), with their high breakdown voltage, enables the system to meet and withstand the medium voltage stress, with a minimized number of cascaded modules. The SiC-based power electronics, when used in the presented topology, they significantly reduce the complexity usually faced when Si devices are used to meet the medium voltage level and the power scalability. The simulation and preliminary experimental results, on a low-voltage prototype, verifies the nine-level CHB topology that is presented in this paper.**

Keywords—SiC Switching Devices; Cascaded H-bridge Inverter; Medium Voltage AC Grid; Energy Storage

I. INTRODUCTION

Power electronics interface to integrate the renewable sources and battery energy storage systems (BESS) in medium voltage grid has drawn attention both in industries and academia. To meet the requirement of medium voltage, paralleling [1] or connecting in series converter cells instead of the power semiconductors is a well-known approach, [2]-[5]. A typical example using a series connection of converter cells is the cascaded H-bridges (CHB) topology. This modular approach can cope with any grid voltage by increasing the number of cascaded modules. However, the circuit structure of a CHB is naturally modular, and the control structure is highly centralized, which makes the overall system more complex. It involves the communication of a large amount of information, complex submodule management, and requires high-bandwidth links for PWM transmission.

The implementation of a modular control presents certain challenges: "coordination schemes and the synchronization of PWM signals". With the purpose of addressing those challenges, SiC devices are used to take advantage of higher voltage ratings, resulting in a greatly reduced number of submodules, thus lowering the total component count, and simplifying the control and management system. Using SiC devices, in Fig. 1, will provide higher temperature capability, which results in relaxing the cooling requirements for the BESS interface. The topology, nine-level CHB three-phase inverter, is fixed throughout the evaluation of SiC devices (1.2 kV to 6.5 kV). Even if the blocking voltages of industrially available semiconductor modules range to several kV, only about 50%–60% of the devices' rated blocking voltage can be utilized in an application in order to limit the susceptibility to cosmic-ray-induced failures [6], [7]. Using 1.2 kV SiC devices in Fig. 1, a 40% safe margin for each switch is considered. Thus, each switch operates at 720 V dc bus for a nine-level CHB three-phase inverter to generate 3 kV rms, 3Φ output. If 6.5 kV SiC devices are used, the dc bus voltage of 3.5 kV for each cell is enough for the inverter to generate 13.8 kV rms, 3Φ output. The nine-level SiC based CHB three-phase inverter is proposed to achieve three optimization goals: i) significantly reduce the number of submodules for the CHB topology, ii) reduce the complexity of control algorithms for medium voltage application, up to 13.8 kV.

The SiC devices are evaluated in modular multilevel, nine-level CHB three-phase inverter to take advantages of their respective benefits, such as high voltage operation, higher thermal conductivity, and higher switching frequency, as shown in Fig. 3. The SiC material has higher bandgap than Si, enabling SiC power devices to operate at higher junction temperatures. The higher breakdown field of SiC also enables higher voltage blocking capability with practical material thickness. Higher thermal conductivity reduces the thermal resistance for heat dissipation.

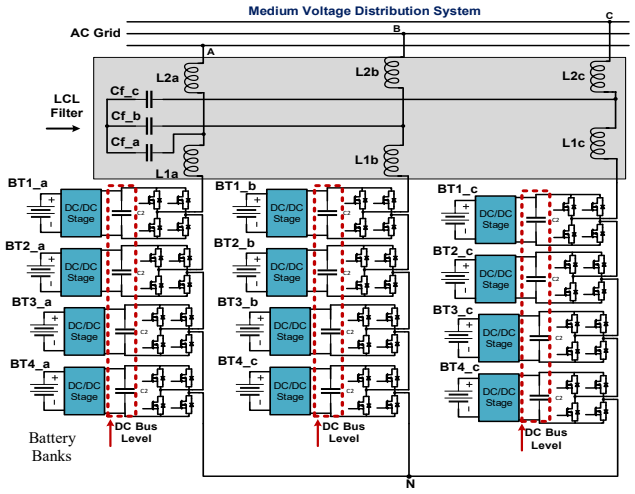

Fig. 1. Nine-level cascaded H-bridge three-phase inverter for modular battery energy storage system

In medium voltage and high power applications, the switching frequency can be extended from below 1 kHz with Si devices to several kHz with SiC devices, enabling higher control bandwidth and potentially reduced filter requirement. In this study with 1.2 kV SiC MOSFETs, the inverter switching frequency is 100 kHz. This paper is organized as follows: Section II shows the description of the topology, section III presents the dc bus requirement for a design with a minimized number of modules. Section IV gives the effect of the switching frequency and the output filter, Section V presents the isolation needed for both the gate drivers and signals' sensing network for the feedback loop. Section VI discusses the distributed control and the strategy to balance the battery system state of charge (SOC). The paper ends with the conclusion in Section VII.

II. Topology Description

The topology shown in Fig. 1 is specifically selected to integrate the battery energy storage system (BESS) into an ac medium voltage distribution system. The inverter is the core element of any battery energy storage system as it charges and discharges batteries to store or provide power according to the application requirement such as frequency control, peak shaving, energy shifting, or voltage control. The optimized number of modules per phase for the inverter to generate 13.8 kV rms, ac 3Φ output voltage is three. As reported in [8], four modules per phase are selected to add another degree of freedom for fault resiliency purpose. Minimizing the number of modules is a goal of evaluating the application of SiC MOSFETs devices. Three-level CHB three-phase inverter uses the lowest number of modules. However, it is not considered for this design. It requires the dc bus voltage level that is higher than the breakdown voltage (≤ 10 kV) of SiC MOSFETs considered in the study.

Papers, [9], [10] give a review and comparison between the most popular power electronics converters for the utility scale BESS. A CHB three-phase inverter, using Si switching devices, turning on and off at a very low switching frequency, lower than 1 kHz, is reported as the most-suitable topology for BESS. When the SiC devices are used in CHB three-phase inverter, they present the advantage of either significantly improve the converter efficiency or reducing a number of modules per phase, as reported in [8]. By taking advantage of the breakdown voltage of SiC MOSFETs, up to 10 kV, the number of modules per phase can be reduced to two for a 13.8 kV medium voltage application. By applying SiC MOSFETs, also the device switching frequency, $f_{sw,dev}$ is increased. With a reduced number of modules, the optimization of the switching frequency should be evaluated.

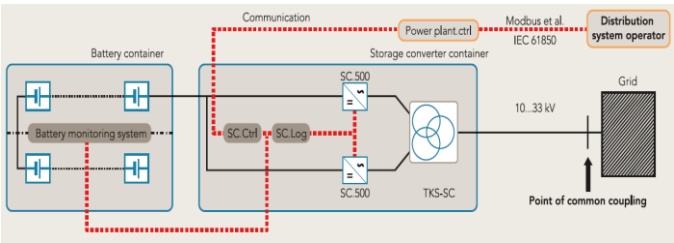

Fig. 2. Typical energy storage system layout [11], and [12]

Many of energy storage power converters use a bulk 60 Hz step-up transformer, such as the example of AEG Power Solutions BESS inverter in Fig. 2, [11], [12]. To eliminate this transformer, much effort has been invested into developing transformerless converters [9], [10]. For a similar purpose, Fig. 1 shows the topology studied to integrate batteries into a 13.8 kV rms distribution system, using SiC MOSFETs as switching devices. With a nine-level CHB three phase inverter, at least a 3.5 kV dc bus is required for each module for the inverter to generate 13.8 kV rms voltage output. A dc/dc stage converter is used to intelligently control the current flowing through the batteries and realize the SOC balancing. With the dc/dc stage in each module, the CHB allows a distributed control over each module, allowing the implementation of balancing schemes, and inherent protection in each battery pack against over-voltage and over-current. This topology presents a flexibility for the controller to follow a battery technology's charging profile. For an example, Fig. 4 shows the lithium battery cell charging profile. For each module, a dc/dc stage follows the control algorithm scheme to regulate the battery current during both charging and discharging modes of the batteries, as previously reported in [8]. For different types of batteries, the controller adaptively follows the respective charging profile.

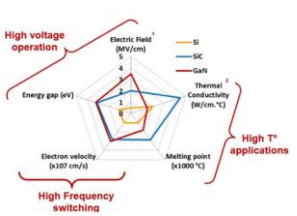

Fig. 3: Wide bandgap device benefits

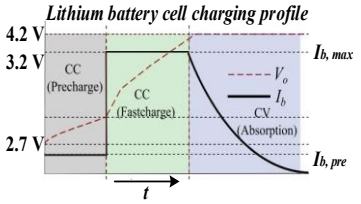

Fig. 4. The cell charging profile [41]

III. Trade-offs Between Minimizing the Number of Modules and the DC Bus Requirement

If 1.2 kV SiC devices are used, the dc bus is controlled and regulated at 720 V. At this dc bus voltage level, the hard-switching can cause damaging over-shoot voltages. The soft-switching mechanism, and intelligent gate driver are recommended, [13]-[18], to prevent a possible voltage over-shoot that is higher than the device breakdown voltage. With a 720 V dc bus, it takes at least 22 modules per phase for the inverter to generate a 13.8 kV rms, 3Φ output. If the number of modules is set at four, like in the Fig. 1, the dc requirement is 3.5 kV, which can be increased to a 4.5 kV dc bus of a seven-level CHB inverter when a fault happens in any cell and causes it to be bypassed. The dc stage converter should be used in each cell to boost the batteries' voltage, regulate the dc bus to a required voltage level and control the current ripple seen by the batteries. Controlling the current ripple contributes to the reliability of the batteries.

While reducing the number of modules for a CHB inverter minimizes the controls' complexity, it creates a trade-off for the dc bus requirement. A minimized number of modules results in a high voltage dc bus requirement. For 13.8 kV rms voltage application, a three-level CHB inverter requires at least 11.3 kV dc bus, a five-level CHB inverter requires 7 kV dc, a nine-level CHB inverter requires 3.5 kV dc bus. If a conventional two-level inverter is used the dc bus requirement for a 13.8 kV system will

be even higher, about 20 kV dc voltage. Boosting the battery bank to 20 kV will result into a less efficient system. If the dc/dc stage is not used, multiple battery banks must be connected in series to reach 20 kV. A BESS application with a medium voltage dc bus presents big technical challenges, such as the insulation. Such high dc bus battery bank will create a coupling capacitor with respect to the ground, which will result into arc faults and high noise from capacitive coupling currents. That will result into a complex system. Moreover, a cell diagnostic method should be implemented for a large scale battery bank, [42]. To avoid the noise coming from capacitive coupling currents, lower battery bank, a typical 400V that is used in data centers [19] provides a better option. The available standards, [20]-[23] for safety are also carefully followed throughout the design. A CHB three-phase inverter with a high power density dc/dc stage is the suitable choice.

For the dc/dc stage, there are many structures to choose from. Synchronous buck/boost converters can be used as a simpler version of dc/dc stage to regulate the current flowing through the battery with lower ripple. The disadvantage of synchronous buck/boost converter is that the gain ratio is lower, thus it still requires high voltage battery banks. The acceptable gain ratio for the synchronous buck boost converter is up to 3x of the battery bank input voltage, otherwise it negatively affects the system overall efficiency. Different types of bidirectional dc/dc converters with possible higher gain are studied in various literatures, [24]-[32]. For higher efficiency and wide-range of dc bus voltage for the system to be connected to 13.8 kV, a high gain step up/down dc/dc converter with a wide-range dc bus regulation is recommended in [8]. For a more compact system, with less switching devices, a current fed-DAB, combined with resonant functionality and soft-switching provides a better option to achieve a high step up/down gain and a significantly reduced ripple in the current flowing into the batteries.

IV. Effect of Swicthing Frequency on The Output Filter Design

The challenges with high voltage SiC MOSFETs devices switching at a high frequency is the dv/dt and di/dt. The soft-switching and intelligent gate drivers are very important to limit the severity of dv/dt and di/dt issues. The requirement for the switches to be turned on under a zero-voltage (ZVS) condition is that the output capacitance, C_{oss} of the switch is fully discharged and the body diode conducts current before the switch turns on [46]. The dead-time interval between the two switches should be longer than the time it takes for C_{oss} to be discharged from the dc input voltage to 0 V. The C_{oss} of the selected SiC MOSFET is 1.54 nF. Equation (1) represents the relationship between the dead-time and drain-source current.

$$\Delta t = \frac{2.C.\Delta V}{i_{ds}} \quad (1)$$

Where Δt is the dead-time interval, C is the output capacitance, ΔV is the voltage across the output capacitor, and i_{ds} is the switch drain-source current. Since the current envelope for the used dc/dc converter is half sinusoidal, there are intervals when the current is near zero. The transformer magnetizing current can also discharge C_{oss}. As long as the dead-time interval is appropriately set, the ZVS during turn-on can be achieved. For bidirectional power flow, either dc-to-ac or ac-to-dc, realizing zero-current (ZCS) turn-off of the switches is the most essential issue. However, given the nature that the operating principle for both directions are not exactly the same, the realization for ZCS requires an adaptive modulation technique. The bidirectional dc/dc stage is designed to realize both soft-switching conditions, ZVS and ZCS.

Besides the soft-switching mechanism, another important part of the ac/dc converter is the LCL filter, which should be designed as a function of the equivalent CHB inverter switching frequency. A value of the converter side inductor is selected according to a specified ripple current flowing through the switching devices. Then, a value of the grid side inductance is determined as a percentage ratio of the converter side inductor. The resonant frequency of the LCL filter should be between ten times of grid frequency, 60 Hz, and half of the inverter switching frequency, 100 kHz. A capacitance value of the LCL filter is selected according to the condition of reactive power absorbed by the filter. For a CHB inverter, generally the switching frequency of the inverter using a phase-shifted modulation is related to the device switching frequency by $f_{sw,inv} = 2Nf_{sw,dev}$, where N is the number of modules per phase. By knowing the phase-to-phase voltage of the grid, the total dc voltage of the inverter can be calculated as a function of modulation index, as shown in equation (2). With a specified operating voltage ($U.V_B$) of the switching device, the number of modules needed per phase can be determined as shown in equation (2).

$$V_d = \sqrt{\frac{2}{3}}\frac{V_{LL}}{ma}. \text{ Thus, } N = \frac{V_d}{U.V_B} \quad (2)$$

Where V_{LL} is the inverter phase-to-phase voltage, ma is the modulation index, U is the percentage utilization of each switching device in CHB, V_B is the break-down voltage of the switching device, and V_d is the total dc voltage.

The LCL filter design for three-phase inverter is described in different literatures, [33]-[37]. The designer specifies an inverter switching frequency ($f_{sw,inv}$), a total dc voltage (V_d), nominal power (P_N), nominal ac voltage, V_{LL} and the maximum allowed current ripple on the inverter side inductor (Δi) and maximum allowed harmonic distortion, specified by the power quality IEEE 519 standard. Moreover, when minimizing the filter, the basic inductance specified in [37], [45] for grid side protection should be satisfied.

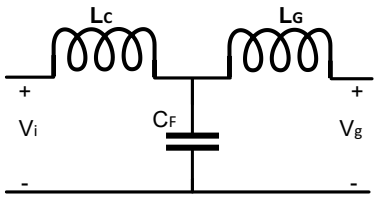

Fig. 5. Per phase LC L filter model

For the LCL filter in Fig. 1, the filter inductors on the inverter side in all phases are equal, $L_{1a} = L_{1b} = L_{1c}$. The same applies for the grid side filter inductors, $L_{2a} = L_{2b} = L_{2c}$.

Similarly, the filter capacitors are equal for all phases, Cf_a = Cf_b = Cf_c. Fig. 5 shows a per phase equivalent model

of the LCL filter. L_C denotes the inductor on the inverter side, L_G denotes the inductor on the grid side, and C_F denotes the filter capacitor. For a 10 kVA system, the design results in following filter parameters: L_C =1.5 mH, L_G = 500 µH, C_F = 1 µF. Calculation of the filter parameters is done in following steps:

a. The inverter side inductor (L_C) calculation according to specified current ripple,(Δi), with equation (3).

$$L_C = \frac{V_d}{8 \,.\, \Delta i \,.\, i_{ph} \,.\, f_{sw,inv}} \tag{3}$$

b. Filter capacitance (C_F) calculation according to specified maximum allowed reactive power absorbed by the filter, Q_F, with equation (4):

$$C_F = \frac{Q_F . P_N}{6\pi . f_g . {V_{LL}}^2} \tag{4}$$

c. Grid side inductor (L_G) calculation using equation (5) according to a specified ripple current on grid side inductor (Δi_g), [33]:

$$L_G = \left| \frac{1 - \Delta i_g}{\Delta i_g . [1 - (L_C . C_F . [2.\pi . f_{sw,inv}]^2)]} \right| . L_C \tag{5}$$

V. Isolation Requirement for Both the Gate Drivers and Sensing Network

The PWM signal generated by the digital controller is 0 to 5 V. To efficiently and fully turn on and off the SiC module, a gate signal from -5 V to 20 V is required. The isolated gate driver is required to provide those voltage levels. The ground on the low voltage digital controller and the high voltage power ground should be separated by an isolation barrier. As shown in Fig. 6, the driver for the upper switch, with *S_Up1a* at a source connection of the upper MOSFET, is separated from the gate driver of the lower switch, with *S_Ls1a* as a source point of lower MOSFET. The digital ground (GND) must be isolated from each MOSFET source. Isolation of the power supply for each gate driver must also be able to isolate the effect of the dv/dt from the primary dc source. Also, the barrier for both the gate driver and the power supply must be able to withstand the highest blocking voltage of the SiC MOSFET. Moreover, for a cascaded structure of the topology in Fig. 1, all the dc buses should be isolated from each other. The isolation within the gate drivers, the power supplies, and the sensing network circuitry must be present and robust to withstand any possible stress coming from faults at high voltage power areas of the topology. The isolated hall effect LEM sensors are used in this study.

The gate driver from Wolfspeed, part# CGD15HB62LP, [44], is used to drive the half-bridge SiC MOSFET power module, [43]. The SiC MOSFET power module switches at speeds beyond what is customarily associated with IGBT-based modules. The special precautions are required to realize the best performance. The interconnection between the gate driver and the module needs to be as short as possible. This will afford the best switching time and avoid the potential device oscillations. Optical fibers provide high transient immunity to the digital signals from the switching dv/dt and di/dt of the MOSFET. Furthermore, a great care is required to ensure minimum inductance between the module and DC link capacitors to avoid excessive drain to source voltage overshoots. More details on minimizing the effect of parasitics when laying out the circuit into the cabinet will be shown in the next paper. The study on mitigating the dv/dt and di/dt issues using active gating and shoot-through protection in intelligent gate driver is reported in [13] – [17], soft-switching mechanism for high voltage SiC modules is also analyzed in [18].

Another issue under high switching speeds (dv/dt) is the so called 'cross-talk' effect, where the turn-on of one device may increase the potential of the gate of the complementary device. If the gate voltage of the complementary device rises above the threshold voltage, this may trigger false turn-on and lead to a shoot-through failure. The high voltage changing rate (dV/dt) is applied across the Miller capacitance of the bottom device during the top device turn on. The resulting current causes a voltage drop on the gate resistance and internal resistance of the gate driver, which raises the gate voltage. In order to avoid the false turn-on of the power device, a negative gate voltage is applied -5V during the off-state. The higher dv/dt and higher gate loop impedance may lead the switching devices to fail, thus the switching speed has to be compromised. In this design an inverter switching frequency of 100 kHz is considered. As the inverter goes through the evaluation process, using different switching devices, SiC MOSFETs (from 1.2 kV to 10 kV), the switching frequency for each voltage level application must be evaluated to optimize the system overall performance.

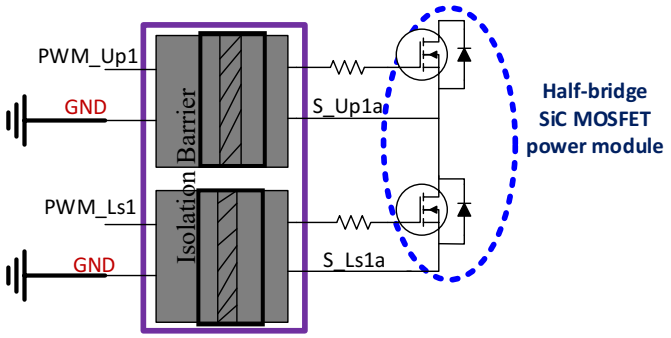

Fig. 6. The isolation barrier required for the gate driver of SiC MOSFETs

VI. The Controls Implementation and SOC Balancing

For the battery SOC balancing the local distributed controllers for each cell's dc/dc stage are implemented to closely monitor the battery bank voltages, currents, and to regulate the dc bus. Three TI DSPs, TMS320F28335, are used to independently control the dc/dc stage converters in respective branches of the inverter, phase A, phase B, and phase C. Each DSP receives the dc bus reference voltage (DC V_{ref}) for the outer voltage loop to follow and generate the reference current for the inner current loop of each cell's control. The central DSP, the fourth, is used for executing a 3Φ PLL, Direct-Quadrature (DQ) rotating frame control computation, active power and ac current control of the overall three-phase inverter. The central DSP, with the feed-forward current controller [8], it sends 3Φ sine references to the Xilinx artix-7 FPGA or Lattice Semiconductor CPLD, MachXO3 device family to generate all the phase-shifted PWMs to respectively switch on and off the twelve H-full bridge cells of the inverter in Fig. 1. The drawing below, Fig. 7, shows the input signals for each control device unit. The DSP for phase

A, uses the sensed signals in each cell to regulate the dc bus in each cell according to the dc bus reference voltage, (DC V_{ref}), received from the central DSP. This is done for all four cells in each phase. For example, Ibat_1A, Vbat_1A, Vdc_1A are the battery current, battery voltage, and dc bus voltage in cell 1 of phase A. The sensed signals in cell 1 of phase B are labeled Ibat_1B, Vbat_1B, Vdc_1B. The sensed signals in cell 1 of phase C are Ibat_1C, Vbat_1C, Vdc_1C. In Fig. 7, the signals of one cell in each phase are only shown for the illustration purpose. Those three DSPs receive the same dc bus voltage reference to ensure that all batteries are charged or discharged at the same rate, and automatically realize the SOC and dc bus voltage balance control required for the BESS CHB three-phase inverter.

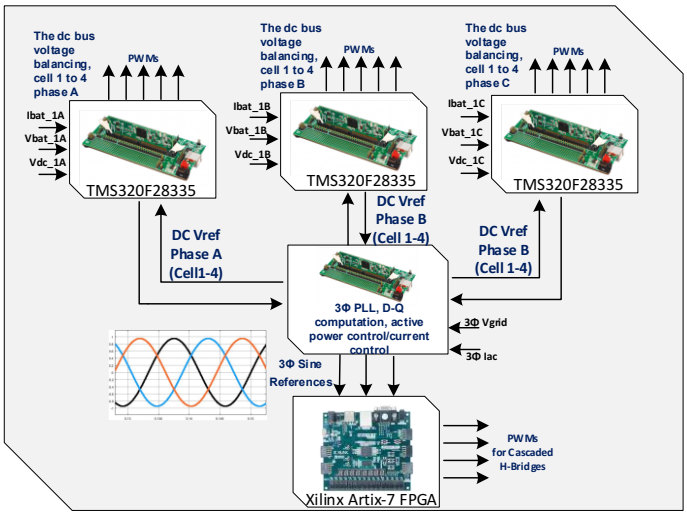

Fig. 7. DSPs and FPGA are used to implement the controls

Besides a SOC balancing control, the designer needs to optimize the design for an efficient interface, with a high power density. The high dc link voltages present a challenge for integrating a BESS in a medium voltage grid. High voltage battery systems exist for different battery technologies. ABB built up a Nickel Cadmium Battery System in Alaska with a dc link voltage of 5 kV [38]. Further, a lithium-ion system with a dc voltage of 5.2 kV was built [39]. To find the optimum string voltage, the types of battery systems are considered and handled differently. Moreover, the string voltage of the battery is only limited by the isolation between the components. The safety precautions are needed for a high voltage dc bus, higher or equal to 400V, [40] to prevent the high battery short circuit currents and possible arch flash incidents. On a battery side dc/dc different topologies are feasible. These converters make a battery management system dispensable because every cell can be operated in its optimum operating point. Another possibility is to connect the batteries in series to a high voltage battery bank which will be connected directly to only one dc-dc converter. The optimum string voltage is not a question of the battery itself. For an optimum design of the overall battery system, it is necessary to know the detailed requirements of the complete system, particularly the planned application and the system environment.

For batteries connected in series to provide high dc bus voltage, it becomes more and more complex to build up compact racks with high energy density. An important challenge for the setup of the storage system is that specifications for high voltage applications are not available for different battery technologies. To ensure a secure operation of the batteries placed in the shelves at medium voltages, there should be an investigation of the dielectric parameters of the components and the electric fields. Dielectric tests for the batteries and the insulation measures for low voltage components like the monitoring system should verified to realize a secure and reliable operation. To ensure the insulation needed for the battery bank, and to avoid the complexity of connecting multiple battery banks in series for a dc medium voltage, 400 V battery bank is selected and boosted to 3.5 kV for a nine-level CHB three-phase inverter to generate for 13.8 kV voltage output. The dc/dc converter with a 9x gain ratio is designed to provide both the isolation and monitoring system for each battery bank, as it is discussed in previous paper, [8].

VII. Prototype and Experimental Results

A scaled down prototype of the topology in Fig. 1 is first designed and tested. The power module, 1.2 kV SiC devices and their respective gate drivers from Wolfspeed are used in the low voltage prototype, Fig. 10. This paper presents the experimental results of the first stage of the testing cycle. Using 1.2 kV in nine-level cascaded H-bridge three-phase inverter, the maximum three-phase voltage that can be generated is 3 kV. The Fig. 8 shows the simulation results for a 208 V grid line. The experimental results for a 208 V grid line are shown in Fig. 13 and Fig. 14. The experimental results at 3 kV will be reported in the next paper, as the testing cycle progresses. The dc/dc stage has been tested independently up to 400 V. To reach 3 kV, the dc bus should be at least 720 V. The dc/dc stage must be tested up to 720 V before the system integrated together and tested at 3 kV rms voltage level.

The cabinet shown in Fig. 10 is donated by Baldor Company, a designer and producer of motor drives. The size of the cabinet was originally customized for a conventional 480 V ac two-level inverter. Thus, the space is not big enough to contain all the dc/dc stages and the full-bridge converters for a nine-level CHB. All twelve full H-bridge converters, the LCL filter, the protection devices, contactors, fuses, and circuit-breakers are populated in one cabinet, then a separate cabinet is used for dc/dc stages. A full design description will be reported in the next paper, showing the details of the cabinet level packaging with minimized parasitic effects and the insulation required for power electronics interface in medium voltage application.

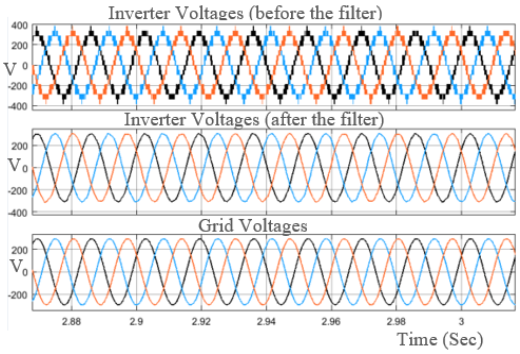

Fig. 8. Simulation results for 208 Vrms, 3Φ

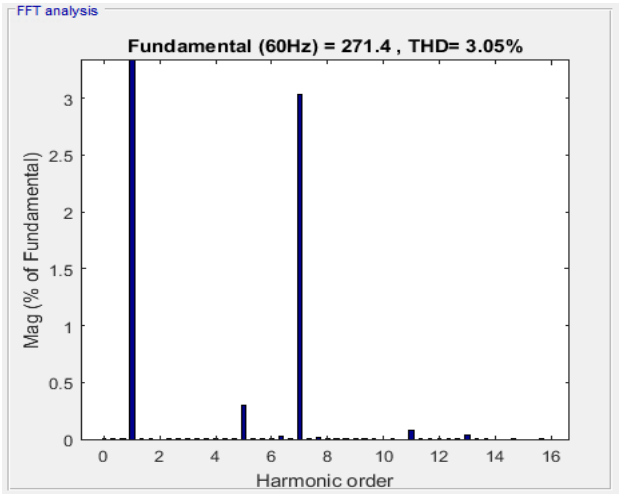

Fig. 9. FFT Analysis at $f_{sw,inv}$ = 100 kHz

TABLE I. THE EVALUATION OF THE OUTPUT FILTER

Filter	*Inverter Switching Frequency, ($f_{sw,inv}$)*	*Rated Power*	*Output Voltage, V_{LL}*	*THD < 5%*
LCL	100 kHz	10 kVA	208 V	3.05%

Fig. 9 and Table I present the results for the FFT analysis of the inverter output voltage after the filter, shown in Fig. 8. Operating the inverter at an inverter switching frequency, $f_{sw,inv}$ of 100 kHz, with the designed filter, the THD is 3.05 %. Similarly, the passive elements in each dc/dc stage is dictated by the switching frequency.

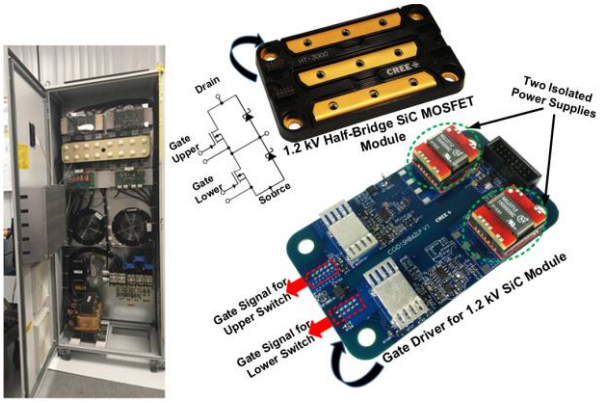

Fig. 10. 1.2 kV SiC devices and gate drivers to be integrated into the cabinet for the medium voltage prototype

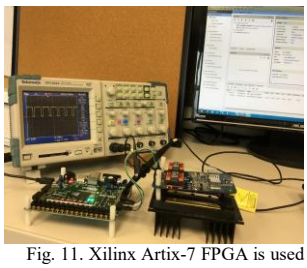

Fig. 11. Xilinx Artix-7 FPGA is used

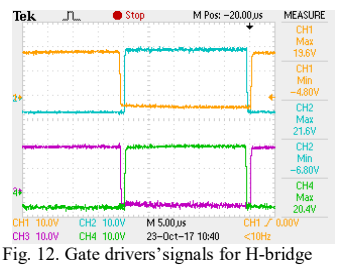

Fig. 12. Gate drivers' signals for H-bridge

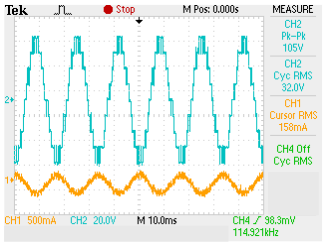

Fig. 13. Output voltage, phase A

Fig. 14. Phase A, grid-connected test

The gate drivers, respectively for each module, are independently tested, as Fig. 11 and Fig. 12 display. Fig. 12 shows the pulse gate signals (+20 V, -5 V) needed to drive the 1.2 kV MOSFETs in order to respectively turn on and off. The inverter is tested at 208 V rms, USA standard 3Φ line, 60 Hz. Fig. 13 shows the preliminary experimental results of the output voltage of the inverter, right before the filter in phase A. The inverter output voltage after the LCL filter is shown in Fig. 14, CH3, synchronized with the grid voltage, CH 2. In Fig. 14, CH4 shows the current flowing into the full H-bridge of one of the cells in phase A, when the inverter is operating in the discharge mode for the BESS to send the power to the grid. The evaluation of the prototype has been tested so far at a 208 Vrms, 3Φ line, 60 Hz. The test will keep progressing up to 3 kV, with 1.2 kV MOSFETs being evaluated as switching devices in the presented nine-level CHB three-phase inverter. Then testing results at 3 kV, 60 Hz, 3Φ voltage will be used to optimize the second prototype using either 6.5 kV or 10 kV SiC MOSFETs half-bridge modules to integrate the BESS into a13.8 kV distribution system.

VIII. CONCLUSION

This paper presented the low-voltage verification of a nine-level cascaded H-bridge three-phase inverter, which has been proposed for integrating a battery energy storage into a medium voltage ac distribution system. 1.2 kV SiC MOSFETs are used for the low-voltage prototype up to 3 kV. High voltage SiC MOSFETs, 6.5 kV or 10 kV will be used in nine-level CHB three-phase inverter to interface the battery energy storage system to a 13.8 kV line. The filter for the inverter is analyzed, with a 100 kHz inverter switching frequency. The THD in output three-phase ac signal is within the specifications of the IEEE 519 standard. Soft-switching mechanism and intelligent gate drivers are considered to mitigate the high dv/dt and di/dt issues that come from high switching frequency of high voltage SiC devices. More details on performance of the 1.2 kV SiC MOSFETs power modules and their respective gate drivers, at 3 kV experimental verification, will be reported in the next paper.

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REFERENCES

[1] Keller and Y. Tadros, "Are paralleled IGBT modules or paralleled IGBT inverters the better choice?," *1993 Fifth European Conference on Power Electronics and Applications*, Brighton, UK, 1993, pp. 1-6 vol.5.

[2] Alessandro L. Matakas, C. Burlacu, and E. Masada, "The connection of converters instead of semiconductor power devices—A high performance solution for the MVA range of power converters," *J. Circuits, Syst. Comput.*, vol. 5, no. 3, pp. 503–521, 1995.

[3] P. Sochor and H. Akagi, "Theoretical and Experimental Comparison Between Phase-Shifted PWM and Level-Shifted PWM in a Modular Multilevel SDBC Inverter for Utility-Scale Photovoltaic Applications," in *IEEE Transactions on Industry Applications*, vol. 53, no. 5, pp. 4695-4707, Sept.-Oct. 2017.

[4] F. Sasongko, K. Sekiguchi, K. Oguma, M. Hagiwara and H. Akagi, "Theory and Experiment on an Optimal Carrier Frequency of a Modular Multilevel Cascade Converter With Phase-Shifted PWM," in *IEEE Transactions on Power Electronics*, vol. 31, no. 5, pp. 3456-3471, May 2016.

[5] J. I. Y. Ota, T. Sato and H. Akagi, "Enhancement of Performance, Availability, and Flexibility of a Battery Energy Storage System Based on a Modular Multilevel Cascaded Converter (MMCC-SSBC)," in *IEEE Transactions on Power Electronics*, vol. 31, no. 4, pp. 2791-2799, April 2016.

[6] J. Dodge, "Reduce circuit zapping from cosmic radiation," *Power Electron. Technol.*, pp. 20–26, Sep. 2007.

[7] N. Kaminski and A. Kopta, "Failure rates of HiPak modules due to cosmic rays (AN 5SYA 2042-04)," ABB Switzerland Ltd., Lenzburg, Switzerland: Tech. Rep., 2011.

[8] J. Umuhoza, H. Mhiesan, K. Mordi, C. Farnell and H.A. Mantooth, " A SiC-Based Power Electronics Interface for Integrating a Battery Energy Storage into the Medium (13.8 kV) Distribution System," *2018 IEEE Applied Power Electronics Conference and Exposition (APEC),* San Antonio, TX, 2018.

[9] G. Wang *et al.*, "A Review of Power Electronics for Grid Connection of Utility-Scale Battery Energy Storage Systems," in *IEEE Transactions on Sustainable Energy*, vol. 7, no. 4, pp. 1778-1790, Oct. 2016.

[10] E. Chatzinikolaou and D. J. Rogers, "A Comparison of Grid-Connected Battery Energy Storage System Designs," in *IEEE Transactions on Power Electronics*, vol. 32, no. 9, pp. 6913-6923, Sept. 2017.

[11] AEG Power Solutions, "Bidirectional Converter for Battery Energy Storage System, AEG Power Solutions".
https://www.aegps.com/en/products/smart-grid-energy-storage/battery-energy-converter/

[12] Alessandro Di Giorgio, Francesco Liberati, Andrea Lanna, "Electric Energy Storage Systems integration in Distribution Grids." Preprint submitted to *15th IEEE International Conference on Environment and Electrical Engineering* (EEEIC 2015).

[13] P. Nayak and K. Hatua, "Parasitic Inductance and Capacitance-Assisted Active Gate Driving Technique to Minimize Switching Loss of SiC MOSFET," in *IEEE Transactions on Industrial Electronics*, vol. 64, no. 10, pp. 8288-8298, Oct. 2017.

[14] A. Kumar, A. Ravichandran, S. Singh, S. Shah and S. Bhattacharya, "An intelligent medium voltage gate driver with enhanced short circuit protection scheme for 10kV 4H-SiC MOSFETs," *2017 IEEE Energy Conversion Congress and Exposition (ECCE)*, Cincinnati, OH, 2017, pp. 2560-2566.

[15] E. P. Eni, S. Bczkowski, S. Munk-Nielsen, T. Kerekes and R. Teodorescu, "Short-circuit characterization of 10 kV 10A 4H-SiC MOSFET," 2016 *IEEE Applied Power Electronics Conference (APEC)*, 2016, pp. 974-978.

[16] S. K. Mainali, S. Madhusoodhanan, A. Tripathi, K. Vechalapu, A. De and S. Bhattacharya, "Design and evaluation of isolated gate driver power supply for medium voltage converter applications," 2016 *IEEE Applied Power Electronics Conference and Exposition (APEC)*, Long Beach, CA, 2016, pp. 1632-1639.

[17] A. Tripathi, K. Mainali, S. Madhusoodhanan, A. Yadav, K. Vechalapu and S. Bhattacharya, "A MV intelligent gate driver for 15kV SiC IGBT and 10 kV SiC MOSFET," 2016 *IEEE Applied Power Electronics Conference and Exposition (APEC)*, Long Beach, CA, 2016, pp. 2076-2082.

[18] D. Rothmund, D. Bortis and J. W. Kolar, "Accurate Transient Calorimetric Measurement of Soft-Switching Losses of 10-kV SiC mosfets and Diodes," in *IEEE Transactions on Power Electronics*, vol. 33, no. 6, pp. 5240-5250, June 2018.

[19] M. M. Krzywosz, "Case study — DC Arc flash and safety considerations in a 400VDC UPS architecture power system equipped with VRLA battery," *2014 IEEE 36th International Telecommunications Energy Conference (INTELEC)*, Vancouver, BC, 2014, pp. 1-9.

[20] IEC60243-2, Electric Strength of Insulating Materials - Test Methods - Part 2: Additional Requirements for Tests Using Direct Voltage, IEC Std.

[21] EN50272-2:2001, Safety requirements for secondary batteries and battery installations - Part 2: Stationary batteries, EN Std., 2001.

[22] EN50191:2009, Erection and operation of electrical test equipment, EN Std., 2009.

[23] IEC60364-4-41:2007, Protection for safety – Protection against electric shock, IEC Std., 2007.

[24] S. Dusmez, A. Khaligh and A. Hasanzadeh, "A Zero-Voltage-Transition Bidirectional DC/DC Converter," in *IEEE Transactions on Industrial Electronics*, vol. 62, no. 5, pp. 3152-3162, May 2015.

[25] L. Zhu, A. Taylor, G. Liu and K. H. Bai, "A Multiple-Phase-Shift Control for A SiC-Based EV Charger To Optimize the Light-load Efficiency, Current Stress and Power Quality," in *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. PP, no. 99, pp. 1-1, 28 March 2018.

[26] M. Kasper, R. M. Burkart, G. Deboy and J. W. Kolar, "ZVS of Power MOSFETs Revisited," in *IEEE Transactions on Power Electronics*, vol. 31, no. 12, pp. 8063-8067, Dec. 2016.

[27] Z. Wang and H. Li, "A Soft Switching Three-phase Current-fed Bidirectional DC-DC Converter With High Efficiency Over a Wide Input Voltage Range," in *IEEE Transactions on Power Electronics*, vol. 27, no. 2, pp. 669-684, Feb. 2012.

[28] S. Bal, A. K. Rathore and D. Srinivasan, "Naturally Clamped Snubberless Soft-Switching Bidirectional Current-Fed Three-Phase Push–Pull DC/DC Converter for DC Microgrid Application," in *IEEE Transactions on Industry Applications*, vol. 52, no. 2, pp. 1577-1587, March-April 2016.

[29] P. Xuewei, A. K. Rathore and U. R. Prasanna, "Novel soft-switching snubberless naturally clamped current-fed full-bridge front-end converter based bidirectional inverter for renewables, microgrid and UPS applications," *2013 IEEE Energy Conversion Congress and Exposition*, Denver, CO, 2013, pp. 2729-2736.

[30] Y. Shi and H. Li, "Isolated Modular Multilevel DC–DC Converter With DC Fault Current Control Capability Based on Current-Fed Dual Active Bridge for MVDC Application," in *IEEE Transactions on Power Electronics*, vol. 33, no. 3, pp. 2145-2161, March 2018.

[31] Li Wang, Qianlai Zhu, Wensong Yu and A. Q. Huang, "A medium voltage bidirectional DC-DC converter combining resonant and dual active bridge converters," *2015 IEEE Applied Power Electronics Conference and Exposition (APEC)*, Charlotte, NC, 2015, pp. 1104-1111.

[32] L. Wang, Q. Zhu, W. Yu and A. Q. Huang, "A Medium-Voltage Medium-Frequency Isolated DC–DC Converter Based on 15-kV SiC MOSFETs," in *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 5, no. 1, pp. 100-109, March 2017.

[33] M. Liserre, F. Blaabjerg, S. Hansen, "Design and Control of an LCL Filter-Based Three-Phase Active Rectifier," *IEEE Transactions on Industry Applications*, vol. 41, no. 5, pp. 1281-1291, September 2005.

[34] S. Piasecki, "High order line filters for Grid Connected AC-DC Converter — Parameters selection and optimization," *2014 IEEE 23rd International Symposium on Industrial Electronics (ISIE)*, Istanbul, 2014, pp. 2691-2696.

[35] S. Pisecki and J. Rąbkowski, "Experimental investigations on the grid-connected AC/DC converter based on three-phase SiC MOSFET module," *2015 17th European Conference on Power Electronics and Applications (EPE'15 ECCE-Europe)*, Geneva, 2015, pp. 1-10.

[36] W. Choi, D. Han, C. T. Morris and B. Sarlioglu, "Achieving high efficiency using SiC MOSFETs and reduced output filter for grid-connected V2G inverter," *IECON 2015 - 41st Annual Conference of the*

IEEE Industrial Electronics Society, Yokohama, 2015, pp. 003052-003057.

[37] T. Guillod, F. Krismer and J. W. Kolar, "Protection of MV Converters in the Grid: The Case of MV/LV Solid-State Transformers," in *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 5, no. 1, pp. 393-408, March 2017.

[38] T. DeVries, J. McDowall, N. Umbricht, and G. Linhofer, "Battery energy storage system for golden valley electric association," ABB Review, vol. 1, pp. 38–43, 2004.

[39] M. T. Holmberg, M. Lahtinen, J. McDowall, and T. Larsson, "Svc light with energy storage for frequency regulation," in *Proc. IEEE Conf. Innovative Technologies for an Efficient and Reliable Electricity Supply (CITRES)*, 2010, pp. 317–324.

[40] Canton, W., and McCleur, S., "DC Arc Flash: 2013 Regulatory Updates and Recommended Battery Risk Assessment Guidelines", *Battcon® 2013 Proceedings*.

[41] S. Biswas, L. Huang, V. Vaidya, K. Ravichandran, N. Mohan and S. V. Dhople, "Universal Current-Mode Control Schemes to Charge Li-Ion Batteries Under DC/PV Source," in *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 63, no. 9, pp. 1531-1542, Sept. 2016.

[42]] A. C. F. Liu, H. S. H. Chung, W. Wang, R. W. H. Lau and J. Zhang, "Diagnostic cell for large-scale battery bank," *2017 IEEE Applied Power Electronics Conference and Exposition (APEC)*, Tampa, FL, 2017, pp. 993-1000.

[43] Wolfspeed, Module Datasheet, part# CGD15HB62LP
https://www.wolfspeed.com/downloads/dl/file/id/967/product/204/cas325m12hm2.pdf

[44] Wolfspeed Gate driver Datasheet, part# CGD15HB62LP
https://www.mouser.com/datasheet/2/90/gd15hb62lp-1290991.pdf

[45] J. E. Huber and J. W. Kolar, "Optimum Number of Cascaded Cells for High-Power Medium-Voltage AC–DC Converters," in *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 5, no. 1, pp. 213-232, March 2017.

[46] M. Wang, Q. Huang, S. Guo, X. Yu, W. Yu and A. Q. Huang, "Soft-Switched Modulation Techniques for an Isolated Bidirectional DC–AC," in *IEEE Transactions on Power Electronics*, vol. 33, no. 1, pp. 137-150, Jan. 2018.