Analysis of a Grid-Connected Shoot-Through Current Immune Three-Phase Converter Topology under Unbalanced Loading Conditions

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***Abstract* — The analysis of a shoot-through-proof converter topology designed to eliminate the need for a dead time between switching transitions is presented. Shoot-through-proof is done by splitting each leg of a normal converter and inserting an inductor to limit the current during transitions. Matlab/Simulink™ simulations based on a 10-kVA laboratory test setup, which was built to validate the proposed ideas, are used to evaluate the system performance. In particular, simulations were used to predict losses associated with the topology and reduce the harmonics injected by the converter. The control system was implemented in a TMS320F28335 DSP, and the results of both the simulations and prototype testing showed very good agreement.**

Keywords— grid-connected converter, power electronics, dead-time compensation, shoot-through current, unbalance compensation

I. INTRODUCTION

High penetration of renewable energy sources, especially a large and growing amount of single-phase distributed generation (DG) in the form of solar power, leads to current imbalances in three-phase distribution systems in which these photovoltaic (PV) arrays are installed. These imbalances cause adverse effects due to the negative- and zero-sequence components [1-6]. Developing reliable solutions is crucial to increase penetration of DG technologies in distribution systems. Several methods were proposed to eliminate these components [7-13]. The method chosen here is similar to that in [14] that consists of three single-phase H-bridges connected to the medium-voltage grid through distribution step-up transformers; this solution is referred as a low-voltage unbalanced current static compensator (LV-UCSC).

Ride-through fault capability is very important for any piece of equipment connected to the grid. For converters in general, one failure mode is shoot-through current through a leg; normally, it is avoided by using a sizeable dead-time between switching transitions. A modified converter no-shoot-through (NST) topology derived from the one proposed in [11] is considered to protect against the catastrophic failure that may occur during a shoot-through current event, and furthermore, to avoid the output voltage distortion that comes from the dead time [15, 16]. This topology splits each leg of a standard converter into two and connects them with an inductor. This is shown on a per-phase basis in Fig. 1 (a) for the resulting six-leg converter. This same concept can be applied to the four-leg converter to reduce the number of switching devices and inductors as depicted in Fig. 1 (b). An analysis of the performance of this topology under the operating conditions for a three-phase LV-UCSC follows.

Overview of the Topology

By inserting an inductor between the cascode IGBTs there is no need to implement a dead-time at switching transitions because the inductor limits any shoot-through current that would otherwise result in catastrophic failure.

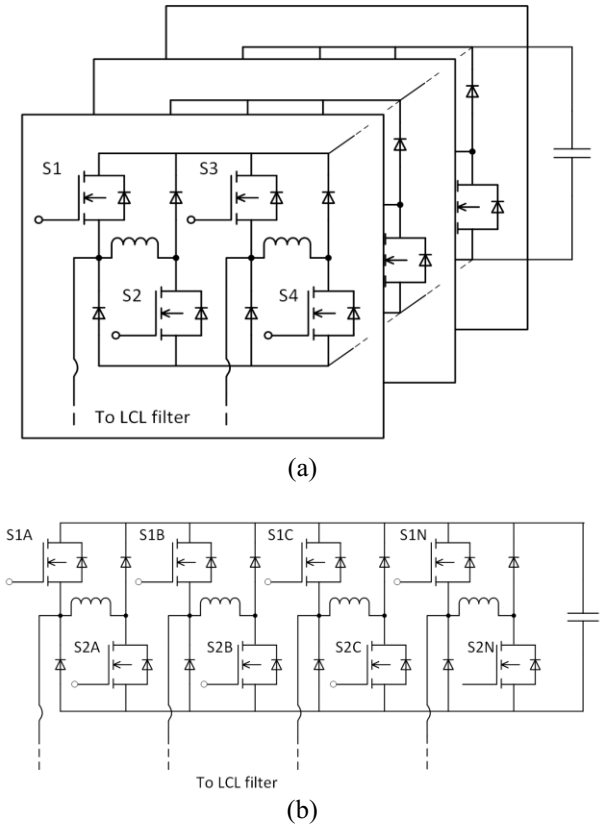

Fig. 1. Shoot-through proof modification to the six-leg converter (a) and four-leg converter (b)

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The addition of two diodes in cascode with the now IGBT split arrangement allows for the excess energy built up within the inductor to dissipate through freewheeling action.

A single leg of the NST converter during operation is shown in Fig. 2. When current is leaving a leg, the inductor and bottom switch are essentially removed from the circuit as the voltage is clamped to the dc bus rails by S1 and D1. The inductor becomes part of the circuit when the current is entering a leg. Fig. 3 displays the resulting current waveforms; Fig. 3 (a) contains the waveforms when the S1 pulse, t_{S1} is SHORTER than that of S3 pulse, t_{S3} (the top switch of the other leg of the converter) - Mode I. The waveforms in Fig. 3 (b) occur when t_{S1} is LONGER than t_{S3} - Mode II. The variable definitions are shown in Fig. 2. The next sections present an analysis of the losses shown in these waveforms.

II. Converter Loss Analysis

The amount of time spent in either of the operating modes shown in Fig. 3 must be determined before determining the losses of the converter. This is dictated by the power factor of the converter load. The phase shift α is found using:

$$a = \cos^{-1}(\text{pf}) \tag{1}$$

with *pf* the power factor. The number of switching cycles in one fundamental period, *N,* is given by:

$$N = \frac{f_{sw}}{f_g} \tag{2}$$

where f_g is the fundamental grid frequency. The number of switching cycles in Mode I, k, is calculated as:

$$k = \left\lfloor \left(1 - \frac{a}{\pi}\right)\frac{N}{2} \right\rfloor \tag{3}$$

and the number of cycles in Mode II becomes $(N - k)$. This holds true if the converter is injecting power into the grid.

If the converter is drawing power from the grid, then k becomes:

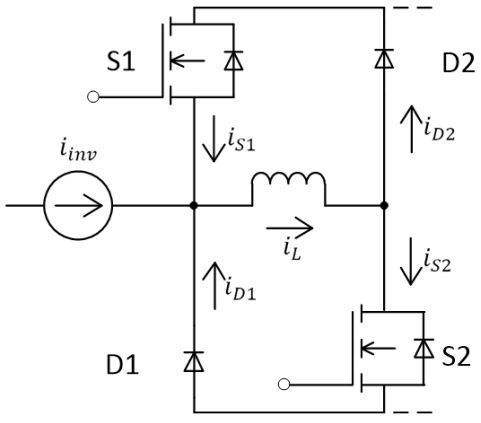


Fig. 2. Current flows within a converter leg

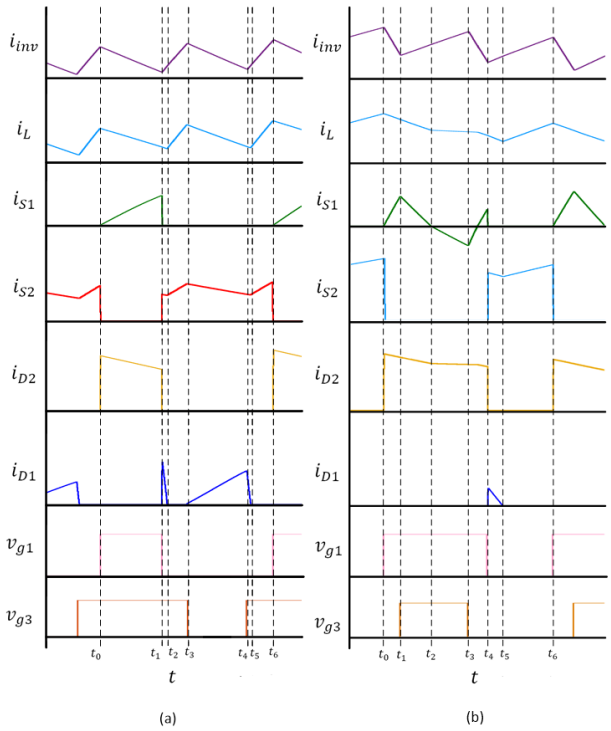


Fig. 3. Current flows during Mode I (a) and Mode II (b)

$$k = \left\lfloor \frac{aN}{2\pi} \right\rfloor \tag{4}$$

The converter current is chosen as the 0° reference angle for the phase-shift instead of the voltage because its direction determines if losses are incurred. The current at each switching instant is:

$$I_{inv} = \sqrt{2} I_{ref} \sin\left(\frac{2\pi n}{N}\right) \tag{5}$$

where n is the switching instant. The resulting grid voltage then becomes:

$$V_g = \sqrt{2} V_{L-N} \sin\left(\text{a} + \frac{2\pi n}{N}\right) \tag{6}$$

Due to the presence of the filter impedance, V_g is not indicative of the actual converter output, V_{inv} which is calculated using:

$$V_{inv} = V_g + I_{inv}\left[\sqrt{2}\omega L_{coup} \sin\left(\text{a} + \frac{2\pi n}{N}\right)\right] \tag{7}$$

The modulation index, m, under standard unipolar switching is determined by:

$$m = \left(\frac{V_{inv}}{2V_{bus}}\right) + 0.5 \tag{8}$$

with V_{bus} as the converter nominal dc-bus voltage. Using m and the switching period, T_{sw}, the pulse lengths t_{S1} and t_{S3} are defined as follows:

$$t_{S1} = (1 - m)T_{sw} \tag{9}$$

$$t_{S3} = mT_{sw} \quad (10)$$

These pulses are always centered upon one another due to the symmetrical switching waveform in the modulation process.

A. MODE I

At t_0, inductances L_{coup} and L_{sc} have been charged by the grid voltage. From t_0 to t_1, S1 is ON and the coupling inductance L_{coup} discharges resulting in a negative current slope:

$$\Delta I_{L_{T2}} = -\frac{V_g - \mathrm{sgn}(V_g)(I_{inv}R_{eq4} - V_{IGBT} - V_d)}{L_{coup} + L_{sc}} \quad (11)$$

with R_{eq4} is defined as:

$$R_{eq4} = R_{L_{coup}} + R_{L_{sc}} + R_{IGBT} + R_d \quad (12)$$

R_{Lcoup} is the resistance of the filter inductors, R_{Lsc} is the resistance of the short-circuit inductor, R_{IGBT} is the resistance of the IGBT, and R_d is the resistance of the diode. Inductance L_{sc}, with its voltage clamped by the upper devices in the converter leg, is discharged at a different rate:

$$\Delta I_{L_{sc}} = -\frac{V_d + V_{IGBT} + I_{inv}R_d + I_1(2R_d)}{L_{sc}} \quad (13)$$

The difference in these discharge rates results in a current that produces losses in S1 and D2. The peak of this current, $\hat{I}_1$ is given by:

$$\hat{I}_1 = \begin{cases} (\Delta I_{L_{sc}} - \Delta I_{L_{T2}})t_{S1} & (\Delta I_{L_{sc}} - \Delta I_{L_{T2}}) > 0 \\ 0 & (\Delta I_{L_{sc}} - \Delta I_{L_{T2}}) < 0 \end{cases} \quad (14)$$

$\hat{I}_{sc}$ is the additional current from the switching transition between S1 and S2. This is calculated as:

$$\hat{I}_{sc} = t_{on}\left(\frac{V_{bus}}{L_{sc}}\right) \quad (15)$$

where t_{on} is the time required for the IGBT to turn on. $\hat{I}_{sc}$ is neglected and $\hat{I}_1$ becomes zero when the discharge slope of L_{sc} is greater than that of L_{coup}.

At t_1, S1 turns OFF and S2 turns ON. Inductance L_{sc} continues to discharge through D1 and S2 until the current in L_{coup} equals the current in L_{sc}. The peak current during this time, $\hat{I}_2$ is equal to $\hat{I}_1$ [16].

The slope of the charging current for L_{coup} becomes:

$$\Delta I_{L_{T1}} = -\frac{V_{bus} - V_g - \mathrm{sgn}(V_g)(I_{inv}R_{eq3} + 2V_{IGBT})}{L_{coup} + L_{sc}} \quad (16)$$

with R_{eq3} defined as:

$$R_{eq3} = R_{L_{coup}} + R_{L_{sc}} + 2R_d \quad (17)$$

The period $t_2 - t_1$, referred to as t_{x1} is the found using:

$$t_{x1} = \frac{\hat{I}_1}{\Delta I_{L_{T1}} - \Delta I_{L_{sc}}} \quad (18)$$

The inductors are charged again from t_2 to t_3, and the sequence above occurs for a second time within the switching period. The energy lost during every switching cycle can then be determined using the following:

$$P_{L1} = 2\sum_{n=0}^{k} t_{S1}\left[I_1(V_d + V_{CE} + I_{inv}R_{IGBT}) + I_1{}^2R_{eq2}\right] \quad (19)$$

$$P_{L2} = 2\sum_{n=0}^{k} t_{x1}\left[I_2(V_d + V_{CE} + I_{inv}R_{IGBT}) + I_2{}^2R_{eq2}\right] \quad (20)$$

with R_{eq2} defined as:

$$R_{eq2} = R_{L_{sc}} + R_{IGBT} + R_d \quad (21)$$

and the rms currents I_1 and I_2 calculated using:

$$I_x = \sqrt{\frac{\hat{I}_x}{2}} \quad (22)$$

The factor of two in P_{L1} and P_{L2} is included because the sequence occurs twice every switching cycle.

B. MODE II

At t_0, both inductances are charged with the same current flowing through them. From t_0 to t_1 again, there is an additional amount of current that flows through S1 and D2 due to the discharge current slope mismatch between the inductances L_{coup} and L_{sc}. The peak current through the devices during this interval, $\hat{I}_3$ is given by:

$$\hat{I}_3 = \begin{cases} (\Delta I_{L_{sc}} - \Delta I_{L_{T3}})\left(\frac{t_{S1} - t_{S3}}{2}\right) + \hat{I}_{sc} & (\Delta I_{L_{sc}} - \Delta I_{L_{T3}}) > 0 \\ 0 & (\Delta I_{L_{sc}} - \Delta I_{L_{T3}}) < 0 \end{cases} \quad (23)$$

At t_0, S4 turns OFF and S3 turns ON. Inductance L_{sc} continues to discharge through D1 and S2 until the current in L_{coup} equals the current in L_{sc}. The peak current during this time, $\hat{I}_4$ is equal to $\hat{I}_3$. The time period $t_2 - t_1$, referred to as t_{x2}, is determined using:

$$t_{x2} = \frac{\hat{I}_3}{\Delta I_{L_{T2}} - \Delta I_{L_{sc}}} \quad (24)$$

From t_2 to t_3, L_{coup} is charged again while the current in L_{sc} has a negligible change. This is because of the assumption that the voltage across the anti-parallel diode of the IGBT and D2 are the same. This results in a near 0 V applied across L_{sc} because the current through L_{sc} is clamping S1's diode.

At t_3, S3 turns OFF and S4 turns ON. The current through L_{coup} begins to decrease with a slope given by:

$$\Delta I_{L_{T3}} = -\frac{V_g + V_{bus} - \mathrm{sgn}(V_g)(I_{inv}R_{eq3} - 2V_d)}{L_{coup} + L_{sc}} \quad (25)$$

The time within the interval from t_3 to t_4 where the current through S1's diode goes to zero, t_{x3} is calculated as follows:

$$t_{x3} = \frac{\Delta I_{L_{coup}}(t_{S3} - t_{x2})}{-\Delta I_{L_{T1}}} \quad (26)$$

After t_{x3} excess current again flows through S1 and D2 with of peak value, $\hat{I}_5$ which is calculated using:

$$\hat{I}_5 = \begin{cases} \left(\Delta I_{L_{sc}} - \Delta I_{L_{T1}}\right)\left(\left(\frac{t_{S1} - t_{S3}}{2}\right) - t_{x3}\right) & \left(\Delta I_{L_{sc}} - \Delta I_{L_{T1}}\right) > 0 \\ 0 & \left(\Delta I_{L_{sc}} - \Delta I_{L_{T1}}\right) < 0 \end{cases} \quad (27)$$

At t_4, the S1 turns OFF and S2 turns ON. The excess energy in *Lsc* is drained through D1 and S2 with a peak current $\hat{I}_6 = \hat{I}_5 + \hat{I}_{sc}$ and that stops at time, t_{x4} which is given by:

$$t_{x4} = \frac{\hat{I}_6}{\Delta I_{L_{T2}} - \Delta I_{L_{sc}}} \quad (28)$$

The energy lost in every switching cycle can then be determined using the following:

$$P_{L3} = \sum_{n=0}^{[f_{sw}-k]} \left(\frac{t_{S1} - t_{S3}}{2}\right)\left[I_3(V_d + V_{CE} + I_{inv}R_d) + {I_3}^2 R_{eq2}\right] \quad (29)$$

$$P_{L4} = \sum_{n=0}^{[f_{sw}-k]} t_{x2}\left[I_4(V_d + V_{CE} + I_{inv}R_d) + {I_4}^2 R_{eq2}\right] \quad (30)$$

$$P_{L5} = \sum_{n=0}^{[f_{sw}-k]} \left(\frac{t_{S1} - t_{S3}}{2}\right)\left[I_5(V_d + V_{CE} + I_{inv}R_d) + {I_5}^2 R_{eq2}\right] \quad (31)$$

$$P_{L6} = \sum_{n=0}^{[f_{sw}-k]} t_{x4}\left[I_6(V_d + V_{CE} + I_{inv}R_{IGBT}) + {I_6}^2 R_{eq2}\right] \quad (32)$$

with the rms currents I_3, I_4, I_5 and I_6 calculated using (22). The limits for P_{L1} and P_{L2} need to be switched with the limits for P_{L3}, P_{L4}, P_{L5} and P_{L6} when the direction of the power flow is changed to into the converter.

C. Total Losses

Because of the turn-on snubber action of L_{sc}, the switching losses for the devices can be reduced to a much lower value; however, the current that flows through the devices during the shorting time does results in a loss, P_{L7} calculated by:

$$U_{L7} = \left(I_{sc}V_{IGBT} + {I_{sc}}^2(2R_{IGBT})\right)t_{on} \quad (33)$$

with I_{sc} calculated using (22). The total power loss for each of the converter legs can be calculated by adding up all the losses P_{L1} through P_{L6} and multiplying by the fundamental grid frequency. For the four-leg topology the above procedure can also be used; however, the applied voltages that give the appropriate discharge slopes and the current magnitude will need to be changed. This is due to the current vector addition that occurs at the neutral node and the differing current paths that result.

III. LV-UCSC Simulation Results

The 3 kVA laboratory prototype was simulated using MATLAB/SIMULINK™; the system parameters are given in Table I and a switching frequency of 5 kHz was chosen.

A. Simulation of Losses

Table II gives a comparison between the losses calculated using the above procedure versus those calculated from the simulation results. The losses are similar with the latter losses slightly overestimating the losses for the 0.1 mH inductance and underestimating those for the higher inductance.

TABLE I. Prototype Component Parameters

Component	Part
IGBT	IRG4PC30FDPbF, 600 V, 31 A
DC bus capacitor	2200 uF, 450 V
Filter Inductor 1	2.2 mH, 10 A
Filter Capacitor	10 uF
Damping Resistor	3.2 Ω
Filter Inductor 2	0.5 mH, 10 A
Shorting Inductors	100 µH

TABLE II. Simulation vs Calculated Losses when using the Shorting Inductor

Shorting Inductor (mH)	Output Current (A)	PF (lag)	Simulation		Calculated
			L Filter Losses (W)	LCL Filter Losses (W)	L Filter Losses (W)
0.1	12.7	0.76	0.55	0.85	0.77
0.1	7.8	1	0.63	0.95	0.7
0.1	9.72	0.87	0.58	0.88	0.72
0.5	11.7	0.76	1.63	2.00	1.49
0.5	7.8	0.87	1.40	1.85	1.38
0.5	6.3	0.98	1.40	1.8	1.33

The procedure in Section II assumed that the filter is a simple L filter so the simulation losses using an L filter and then an LCL filter were compared to determine the validity of this assumption. Overall, the LCL filter losses were higher than those of the L filter. The simulations do not account for the shorting current or the associated switching losses, so $\hat{I}_{sc}$ had a value of 0 A in the calculations.

B. Simulations of Unbalanced Current Operation

Fig. 4 and Fig. 5 illustrates the converter current from simulations. The six-leg converter currents show a decrease in harmonic content from the standard to the shoot-through-proof topology from to 9.38 to 5.54%. The four-leg converter has significant even harmonics (40% - 50%) in the output due to the shorting inductor.

The voltage drop across the shorting inductor along with the output current of the converter is displayed in Fig. 6 (a). The voltage across the inductor results in a significant second harmonic voltage at the converter output. An FFT of the shorting inductor voltage is given in Fig. 6 (b). In a full-bridge converter the neutral leg current is always equal to the phase current. This means that the voltage drop shown in Fig. 6 is the same for both shorting inductors and offset by π radians. The overall effect is then a fundamental frequency voltage subtracted from the output, which can be simply compensated by the current controller. In the case of the four-leg converter, the neutral current does not always equal any of the phase currents, so the voltage drop becomes an issue and causes even-order harmonics like in Fig. 5 (b).

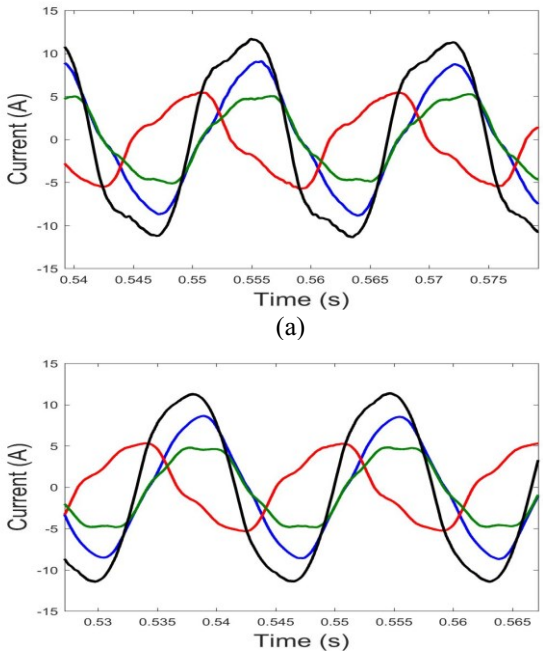


Fig. 4. Simulation converter currents for the six-leg three-phase converter in the (a) standard and (b) shoot-through-proof topologies

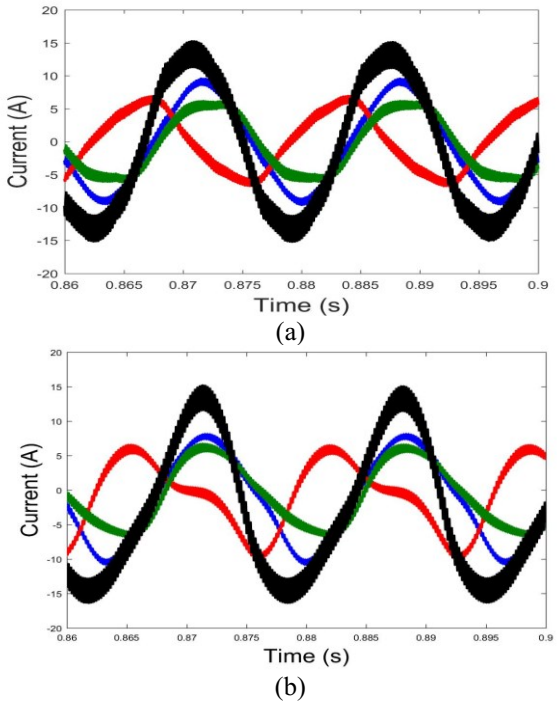


Fig. 5. Simulation converter currents for the four-leg three-phase converter in the (a) standard and (b) shoot-through-proof topologies

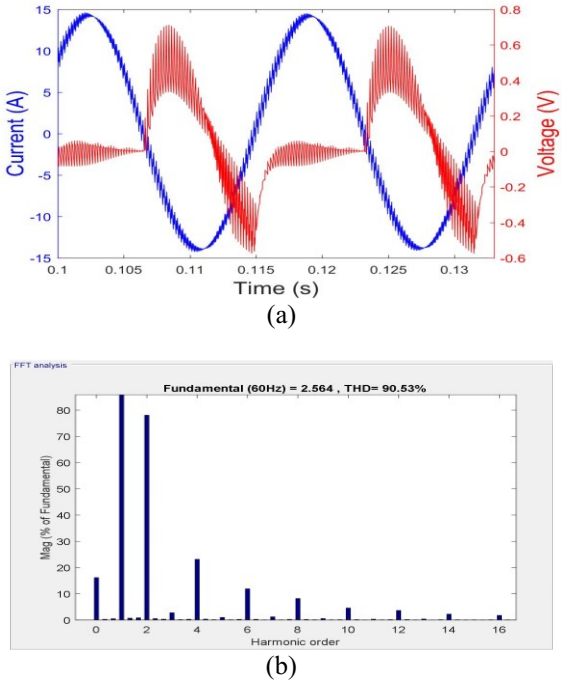


Fig. 6. (a) Converter current and L_sc voltage, (b) FFT of L_sc voltage from simulations of the prototype

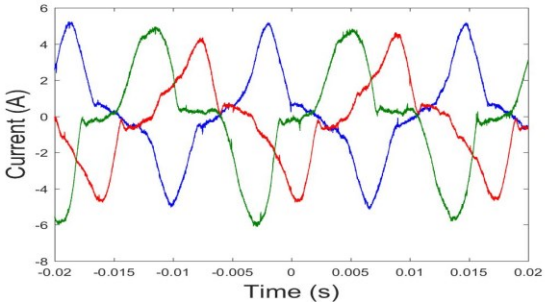
IV. LV-UCSC EXPERIMENTAL RESULTS

A three-phase 120 V, 3 kVA converter is used to confirm the results from the simulations. First, the six-leg converter was used in the standard configuration, three single-phase converters with a dead-time of 1 µs between switching transitions. The measured converter currents are displayed in Fig. 7 (a). The converter currents under the same loading conditions, but in the shoot-through-proof topology are presented in Fig. 7 (b). The THD of the converter current has been reduced from 53% to 36%.

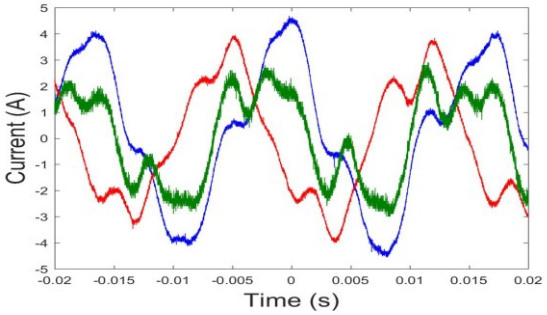
The same comparison for the four-leg prototype is made in Fig. 8 (a) and Fig. 8 (b). In Fig. 8 (b) the odd harmonics have been reduced, but as demonstrated in Section IV, significant low-order even harmonics have been introduced due to the shorting inductors. This disadvantage was mitigated by using the SOGI-based harmonic compensation techniques in [17] for the second and fourth harmonics. The results are illustrated in Fig. 9 (the black waveform is the neutral current). The second and fourth harmonics have been significantly reduced leaving only the original odd harmonics. The THD has been reduced from 53% to 45% for the same operating conditions.

V. CONCLUSIONS

An analysis of a new variation on the inductor-based shoot-through-proof converter was presented. An iterative computational method for determining the losses due to the presence of the shorting inductor was shown and compared with loss calculations using simulations.

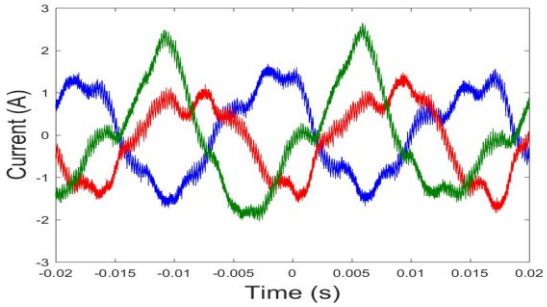


(a)

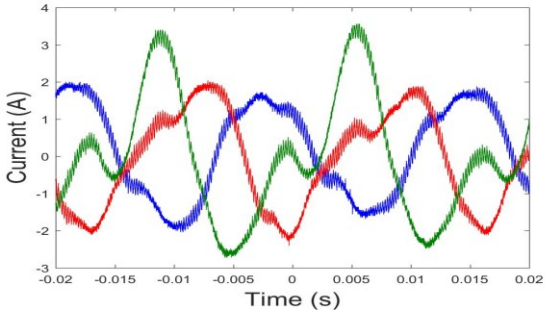


(b)

Fig. 7. Testing converter currents for the six-leg three-phase converter in the (a) standard and (b) shoot-through-proof topologies



(a)



(b)

Fig. 8. Testing converter currents for the four-leg three-phase converter in the (a) standard and (b) shoot-through-proof topologies

Results from simulations and prototype testing of six-leg and four-leg, standard and shoot-through-proof converters used as a grid-connected low-voltage unbalanced current static compensator were shown.

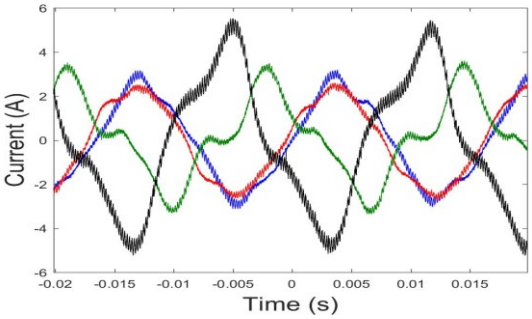


Fig. 9. Testing converter currents for the shoot-through-proof topology with harmonic compensation.

The elimination of the dead time between switch transitions in the converter leg had a positive impact on the odd-order harmonic content of the converter currents. In the case of the four-leg converter in the shoot-through-proof configuration, low-order even harmonic currents appeared as a result of the shorting inductors paired with the mismatch in the phase and neutral currents. These low-order even harmonics were significantly reduced by using SOGI-based harmonic compensation.

The shoot-through-proof configuration increases the reliability of a grid-connected converter by limiting shoot-through current and has the potential to decrease the THD, but it required an inherent increase of the cost due to the extra inductors and diodes. In the case of the four-leg converter the reduction in the number of components led to other challenges. The dc-bus voltage must be increased to accommodate the same grid voltage, which led to an increase in the size of the shorting inductors. Even-order harmonics in the converter current appeared as a result of the inductors, which were partially compensated by the converter controller. The size of the inductance could be significantly reduced by using Si MOSFETs or wide-bandgap devices, which can switch much faster (e.g., 10-80 ns) than the Si IGBTs used in the prototype (i.e., 250-400 ns). Reducing the necessary size of the inductance should lessen the effect of the disadvantages mentioned above.

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