

Large-Area, Ultrathin Metal-Oxide Semiconductor Nanoribbon Arrays Fabricated by Chemical Lift-Off Lithography

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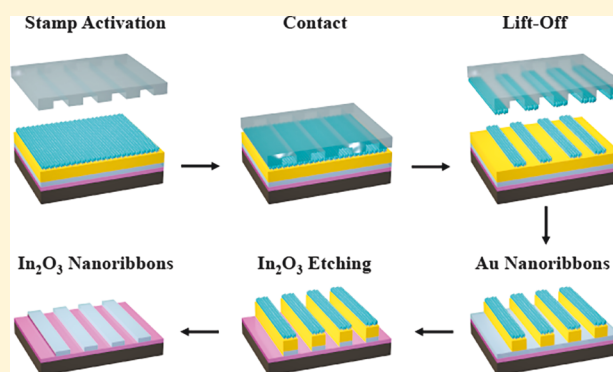
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Supporting Information

ABSTRACT: Nanoribbon- and nanowire-based field-effect transistors (FETs) have attracted significant attention due to their high surface-to-volume ratios, which make them effective as chemical and biological sensors. However, the conventional nanofabrication of these devices is challenging and costly, posing a major barrier to widespread use. We report a high-throughput approach for producing arrays of ultrathin (~ 3 nm) In_2O_3 nanoribbon FETs at the wafer scale. Uniform films of semiconducting In_2O_3 were prepared on Si/SiO₂ surfaces via a sol-gel process prior to depositing Au/Ti metal layers. Commercially available high-definition digital versatile discs were employed as low-cost, large-area templates to prepare polymeric stamps for chemical lift-off lithography, which selectively removed molecules from self-assembled monolayers functionalizing the outermost Au surfaces. Nanoscale chemical patterns, consisting of one-dimensional lines (200 nm wide and 400 nm pitch) extending over centimeter length scales, were etched into the metal layers using the remaining monolayer regions as resists. Subsequent etch processes transferred the patterns into the underlying In_2O_3 films before the removal of the protective organic and metal coatings, revealing large-area nanoribbon arrays. We employed nanoribbons in semiconducting FET channels, achieving current on-to-off ratios over 10^7 and carrier mobilities up to $13.7 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$. Nanofabricated structures, such as In_2O_3 nanoribbons and others, will be useful in nanoelectronics and biosensors. The technique demonstrated here will enable these applications and expand low-cost, large-area patterning strategies to enable a variety of materials and design geometries in nanoelectronics.

KEYWORDS: Soft lithography, chemical lift-off lithography, indium oxide, metal oxide semiconductors, field-effect transistor, nanoribbon



One-dimensional (1D) nanomaterials, such as nanowires, nanotubes, and nanoribbons, possess large surface-to-volume ratios and tunable physical properties. These characteristics can be leveraged to achieve superior performance over bulk materials in a variety of applications, including electronics,^{1–5} optics and photonics,^{6–10} energy-storage and conversion devices,^{11,12} biological and chemical sensors,^{13–19} intracellular delivery of bioactive molecules,²⁰ and medical devices.^{21,22} For example, Si nanowires (SiNWs) and carbon nanotubes (CNTs) have been employed as channel components in field-effect transistors (FETs) for highly effective sensing of proteins,^{23,24} DNA,^{25,26} viruses,²⁷ and neurotransmitters.²⁸ However, sig-

nificant problems remain to be solved before 1D nanomaterials find widespread use.

Bottom-up techniques, such as chemical vapor deposition (CVD) and solution processes,^{29–33} dominate 1D-nanomaterial fabrication. However, these strategies have poor control over the orientations of as-grown nanostructures, often on substrates other than the final devices. Bottom-up methods require additional steps to transfer nanostructures and then to control their positions and orientations in devices.^{34,35} For example,

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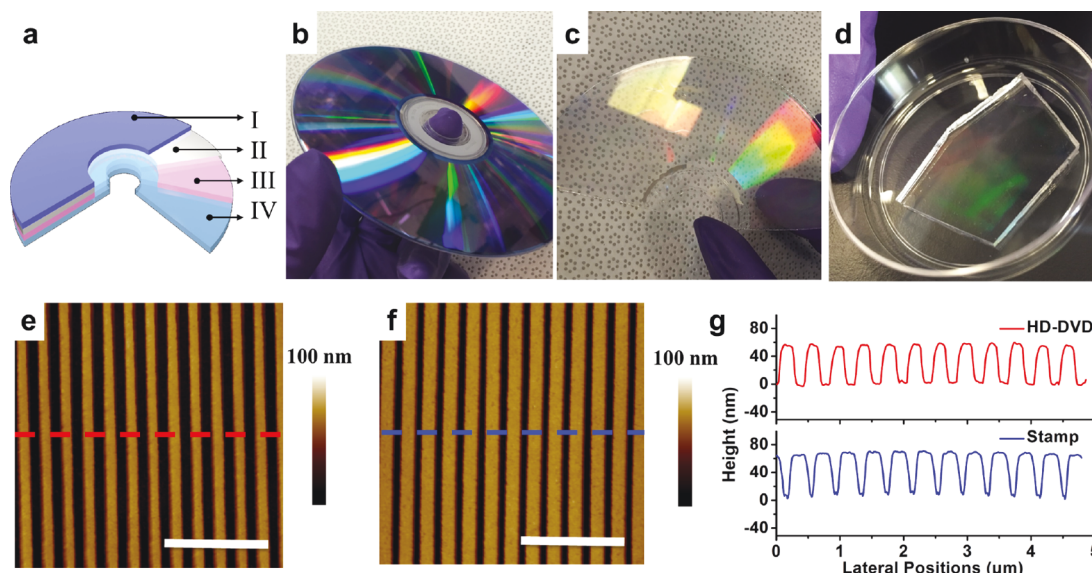


Figure 1. (a) Schematic architecture of a high-definition digital versatile disc (HD-DVD): layer I, polycarbonate protective layer; layer II, mirror-like metal film; layer III, data recording film; layer IV, polycarbonate layer containing concentric rings with typical widths of 250 nm and periodicities of 400 nm. (b–d) Photographs of an HD-DVD, an HD-DVD master (layer IV), and a patterned polydimethylsiloxane (PDMS) stamp, respectively. Atomic force micrographs of (e) a representative HD-DVD master and (f) a patterned PDMS stamp. Scale bars are 2 μm . (g) Topographic profiles across the corrugated features in panels e and f.

SiNWs and CNTs, typically synthesized by CVD, require precise control over specific growth parameters to produce high-quality 1D nanomaterials suitable for electronic devices.^{29,36} Moreover, nanowires synthesized by CVD are randomly oriented, greatly increasing the complexity of device fabrication.³⁷ Performance is limited by poor control over the number of functional nanowires present in devices.^{38,39}

Top-down approaches, including photolithography and electron-beam lithography (EBL), are widely used in the semiconductor industry to fabricate 1D nanomaterials. Top-down methods enable precise control over the final shapes, sizes, positions, and orientations of the as-fabricated structures,^{40,41} providing ready integration with devices and high reproducibility.^{42,43} Nonetheless, top-down techniques suffer from substantial equipment and usage costs. Patterns produced via photolithography are limited by the costs of masks and photon sources. In contrast, EBL achieves nanometer-resolution patterning but at the expense of time-consuming serial writing processes. These drawbacks represent significant barriers for many users, hence the need for alternative high-throughput, economical nanoscale patterning strategies.

Recently, we reported a straightforward, high-fidelity nanopatterning technique called chemical lift-off lithography (CLL),^{44–49} wherein oxygen plasma-activated polydimethylsiloxane (PDMS) stamps selectively remove portions of a self-assembled monolayer (SAM) in contacted areas without observable lateral diffusion at feature edges. The remaining SAM molecules in the non-contacted regions act as molecular resists during subsequent etching of the freshly exposed underlying substrate. We previously demonstrated that CLL can be used to simplify device fabrication as well as to enable biomolecule patterning to investigate DNA hybridization and spin-selective electron transport.^{50–54} High-fidelity chemical patterns with line widths as narrow as 40 ± 2 nm were achieved using CLL, with the possibility of features as narrow as 5 nm (corresponding to ~ 10 molecules).⁴⁶ As with other top-down patterning approaches, however, CLL relies on expensive

nanofabricated masters to create PDMS stamps to produce nanoscale structures. Masters for CLL have been produced using low-throughput EBL methods, limiting impact.^{47,48}

Many top-down nanofabrication processes, including CLL, have focused on patterning metals and group IV and III–V semiconductors (e.g., Au and Si).⁵⁵ Metal oxides represent an increasingly important material class in numerous applications due to their electronic, mechanical, and optical properties.^{45,56–58} To date, top-down approaches for fabricating metal-oxide nanomaterials are underdeveloped compared with patterning methods for other types of materials, yet patterned semiconductors are of interest for applications including electronics; displays and lighting; ultrasensitive biosensors; and wearable, flexible sensors.^{59–61}

We report on the fabrication of large-area In_2O_3 nanoribbon arrays using CLL but without using masters generated via EBL. We utilize metal oxide nanoribbons as semiconducting channels in FET architectures. Through this demonstration, we extend the range and applicability of CLL patterning to nanoscale features on semiconducting metal oxides for functional electronic devices, achieving current on-to-off ratios of $\sim 10^7$ and a peak mobility of $13.7 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$, in a low-cost, high-throughput manner.

Most commonly used thin-film metal oxide deposition strategies rely on physical and chemical vapor deposition methods, such as pulsed-laser deposition,⁶² sputtering,⁶³ and atomic-layer deposition,⁶⁴ requiring complex processes, extreme conditions (e.g., high temperature or a vacuum), and costly equipment. Recently, simple, scalable sol–gel-based processes have emerged as alternatives for preparing high-quality semiconducting metal-oxide films.^{65–68} Here, thin films of In_2O_3 were prepared via a sol–gel process. Aqueous solutions (0.1 M) of $\text{In}(\text{NO}_3)_3$ were spin-coated onto SiO_2/Si substrates (100 nm, thermally grown SiO_2 dielectric on heavily doped, *p*-type Si substrates with resistivities of 1–5 $\text{m}\Omega\cdot\text{cm}$). Following deposition, substrates were heated to 100 $^\circ\text{C}$ for 5 min and annealed at 350 $^\circ\text{C}$ for 3 h. The thicknesses of the resulting

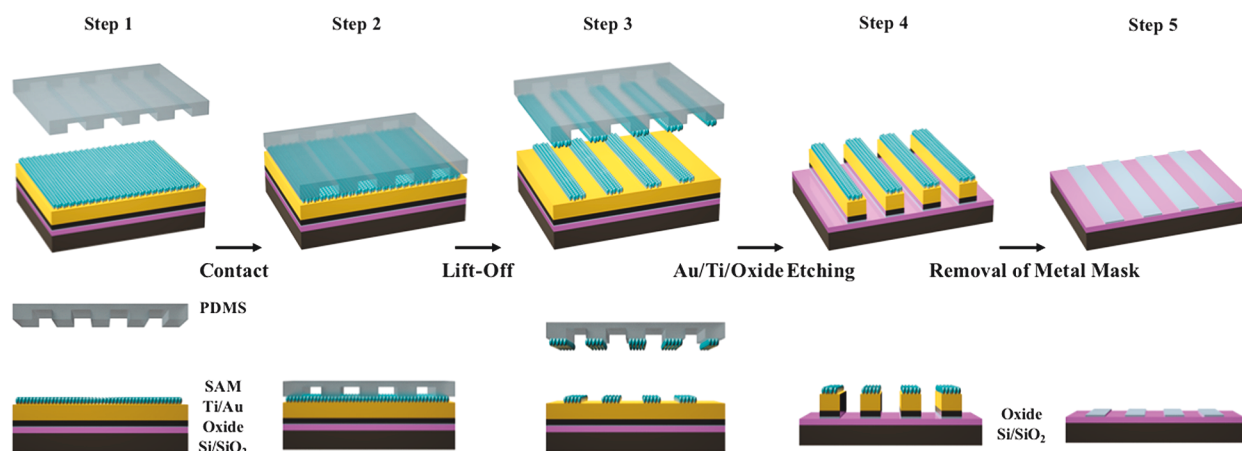


Figure 2. Fabrication scheme of In_2O_3 nanoribbons. Step 1: a thin film of 3 nm In_2O_3 is deposited on a SiO_2/Si substrate via a sol-gel process followed by Au (30 nm)/Ti (10 nm) deposition and functionalization with a self-assembled monolayer (SAM). Step 2: a PDMS stamp, activated by an oxygen plasma, is brought into conformal contact with the substrate. Step 3: Upon lifting the stamp from the surface, SAM molecules in the contacted areas are removed, transferring the pattern (periodic lines and spaces) into the SAM. Step 4: Successive selective etch processes remove Au/Ti and In_2O_3 layers from unprotected regions on the surface. Step 5: Remaining SAM, Au, and Ti are removed to produce In_2O_3 nanoribbon arrays.

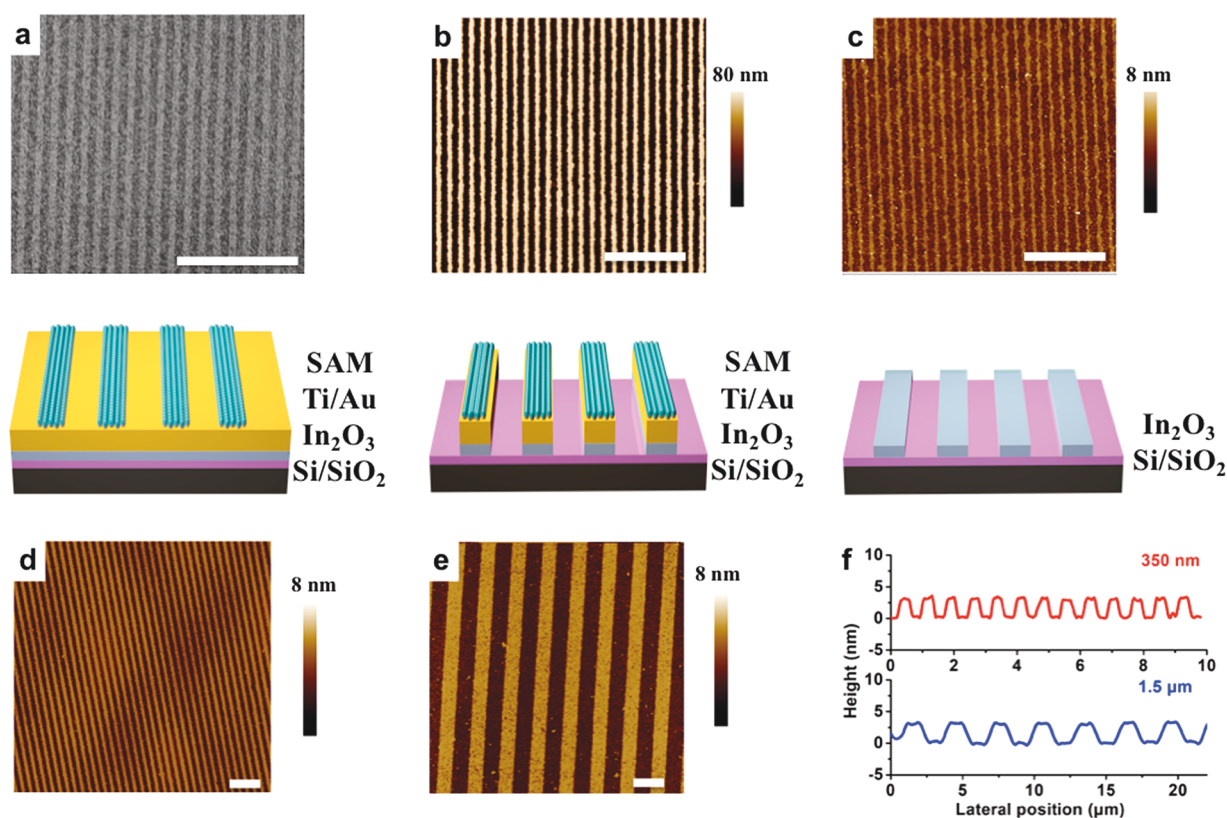


Figure 3. (a) (top) Scanning electron microscope image and (bottom) schematic of a self-assembled monolayer (SAM) patterned via chemical lift-off lithography. (b,c) (top) Topographic images measured using atomic force microscopy (AFM) and (bottom) schematic illustrations of SAM/Au/Ti/ In_2O_3 and bare In_2O_3 nanoribbons, respectively, with line widths of ~ 200 nm. Atomic-force topographs of In_2O_3 nanoribbons with line widths of (d) 350 nm and (e) $1.5\ \mu\text{m}$. Thicknesses of each set of In_2O_3 nanoribbons (shown in panels c–e) were measured as ~ 3 nm by AFM. (f) Height profiles of (top) 500 nm wide In_2O_3 nanoribbons and (bottom) $1.5\ \mu\text{m}$ wide nanoribbons. Scale bars in all images are $3\ \mu\text{m}$.

In_2O_3 films were ~ 3 nm with a typical average surface roughness of ~ 0.06 nm, determined via atomic force microscopy (AFM) (Figure S1). Note that the In_2O_3 films fabricated via the sol-gel process are amorphous.⁴⁵

Commercially available optical storage media, such as compact discs (CDs) and digital versatile discs (DVDs) are patterned with submicron periodic gratings that can be used

directly as economical templates for soft lithography. We employed high-definition DVDs (HD-DVDs) as masters for CLL PDMS stamps. The HD-DVDs have quasi-1D feature widths of ~ 200 nm, spaced at a pitch of 400 nm. As shown in Figure 1a, each HD-DVD is composed of a protection layer (I), a reflective layer (II), a recording layer (III), and a polycarbonate layer (IV) composed of embossed concentric rings that form the

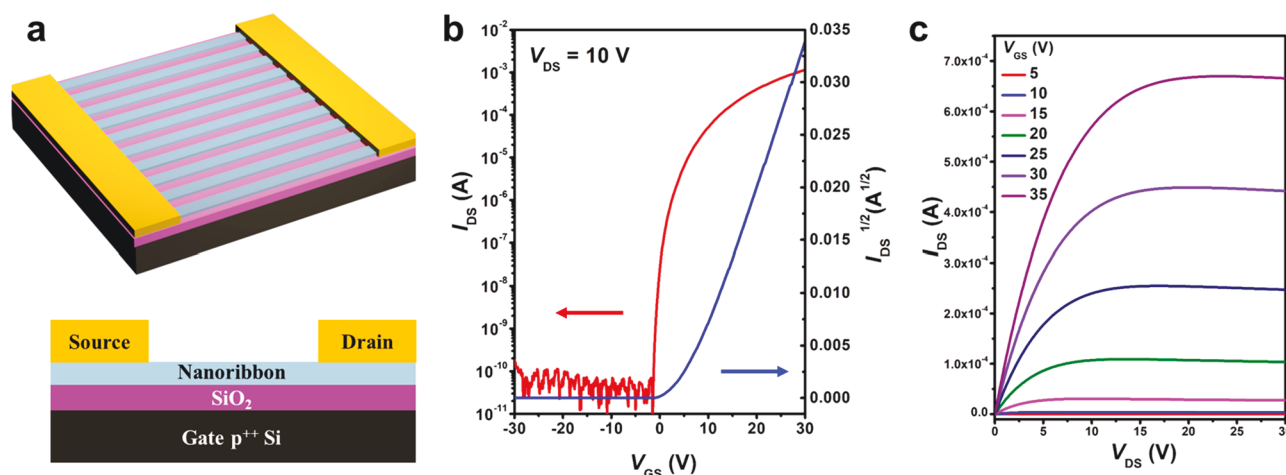


Figure 4. (a) Schematic illustrations of an In_2O_3 field-effect transistor (FET) in a bottom-gate-top-contact configuration. Gate: $\text{Si}(\text{p}^+)$. Source/drain: Au. Semiconducting channel: In_2O_3 nanoribbons. The widths and lengths of the interdigitated electrodes are 1300 and 45 μm , respectively. The widths and pitches of the nanoribbons are 200 and 400 nm, respectively. (b) Transfer and (c) output characteristics of an ultrathin In_2O_3 nanoribbon FET, showing the measured current between the drain and source (I_{DS}) in response to varying gate to source voltages (V_{GS}) and source to drain (V_{DS}) potentials, relative to the source. Devices displayed n -type pinch-off behavior with carrier mobilities of $10.0 \pm 2.6 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$, averaged over 10 devices with a peak value of $13.7 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$, and a current on-to-off ratio of $>10^7$.

basis of the patterns used herein. Layer IV was exposed simply by removing layers I and II with a razor blade and dissolving layer III with ethanol (Figure 1c). Atomic force microscopy confirmed the expected, grooved pattern on the surface of layer IV, as seen in Figure 1e. To replicate layer IV features precisely, hard PDMS (h -PDMS) was used as the stamp material due to its stiffness compared to regular (soft) Sylgard 184 PDMS.⁶⁹ Unpolymerized h -PDMS was spin-coated onto masters (2 cm $\times$ 2 cm, 40 s at 1000 rpm) and cured at 65 $^\circ\text{C}$ for 10 min to form thin and robust films. A layer of soft PDMS (~ 5 mm) was then applied and cured at 65 $^\circ\text{C}$ overnight to form a support for the pattern-containing h -PDMS film and to prevent cracking, prior to demolding stamps from masters. These stamps (Figure 1d) are reusable and can be employed for repeated, wafer-scale CLL patterning. Atomic-force micrographs of patterned PDMS surfaces (Figure 1f) confirmed precise replication of HD-DVD features with depths of ~ 60 nm.

The scheme used to fabricate In_2O_3 nanoribbons is illustrated in Figure 2. Step 1: layers of Ti (10 nm) and Au (30 nm) were deposited on previously prepared In_2O_3 films. The Au/Ti/ In_2O_3 / SiO_2 / Si stacks were then incubated in 1 mM solution of 11-mercapto-1-decanol ($\text{HSCH}_2(\text{CH}_2)_9\text{SH}_2\text{OH}$) in ethanol to form SAMs terminated with $-\text{OH}$ moieties, enabling CLL patterning. Step 2: oxygen plasma was used to “activate” PDMS stamp surfaces, generating siloxyl groups (SiOH). Stamps were then brought into conformal contact with SAMs. Condensation reactions occur between the hydroxyl ($-\text{OH}$)-terminated SAMs and the SiOH groups of the activated h -PDMS, forming covalent linkages ($\text{Si}-\text{O}-\text{SAM}$). Step 3: Upon removal of the stamps, molecules within the contacted regions of the SAMs were selectively removed, transferring the stamp pattern to the monolayer. Notably, in the lift-off process, monolayers of Au atoms are also removed because Au-S bonds (between SAM molecules and the underlying Au substrate atoms) are stronger than Au-Au bonds in the substrates.^{44,49}

Scanning electron microscopy of CLL-patterned SAMs (Figure 3a) confirmed the presence of 1D features (200 nm line widths) over large areas, matching those on the stamps (Figure 1f). Step 4: intact monolayers in the noncontacted regions acted as resists for successive etching by solutions of

$\text{Fe}(\text{NO}_3)_3$ and thiourea (removing exposed Au) and EDTA disodium salt, NH_4OH , and H_2O_2 (removing Ti), thereby transferring the SAM patterns through the metal layers. The metal layers acted as etch masks, protecting the underlying In_2O_3 films from removal by glacial acetic acid. The resulting Au/Ti/ In_2O_3 nanoribbons were investigated by AFM (Figure 3b) and found to have heights of ~ 45 nm, corresponding to the sum of the expected heights of the constituent layers above the surrounding Si/SiO_2 surfaces exposed by previous etching processes. Step 5: metal layers were completely removed to expose arrays of In_2O_3 nanoribbons extending over centimeter length scales (Figure 3c). The widths (~ 200 nm) and heights (~ 3 nm) of the metal oxide nanoribbons are the smallest, to our knowledge, fabricated via top-down approaches.

To demonstrate the versatility of CLL patterning for additional feature sizes, In_2O_3 nanoribbons of different line widths (350 and 1500 nm) were fabricated using alternate master patterns (panels d and e of Figure 3, respectively). The Au nanoribbons produced as an intermediate product of this process (step 4) can also be used for a variety of applications, such as surface plasmon resonance biosensors. Note that In_2O_3 nanoribbon edges are rougher than those of similarly produced Au nanoribbons and the feature sizes are reduced; this is a common phenomenon associated with isotropic etch processes, which can undercut regions below the protective masks.

Field-effect transistors have key advantages over optical or electrochemical platforms for biosensing applications, including low detection limits, real-time and label-free measurements, and simple integration with standard semiconductor-device processing.⁴⁵ To evaluate the performance of In_2O_3 nanoribbons in devices, we constructed FETs in a bottom-gate, top-contact configuration, as shown in Figure 4. Gold electrodes were deposited atop arrays of as-prepared In_2O_3 nanoribbons via electron-beam evaporation through conventional photolithography. The device measurement setup is shown in Figure S2. As shown in Figure S3, interdigitated electrodes with widths of 1300 μm and lengths of 45 μm were used.

The spatially ordered arrangement of In_2O_3 nanoribbons on surfaces facilitated the straightforward fabrication of FETs with consistent numbers of channels per device, controlled by the

widths of the contact electrodes. Here, ~ 3000 200 nm wide In_2O_3 nanoribbons were incorporated into each FET device. These FETs had high field-effect mobilities ($\mu_{\text{sat}} = 10.0 \pm 2.6 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$), averaged over 10 devices with a peak value of $13.7 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$ and a current on-to-off ratio of $>10^7$. We attribute the variations in mobilities to imperfections of the sol-gel-processed thin-film material itself (such as defects), as we have observed similar variations in analogous thin film FETs.⁴⁵ These nanoribbon FETs have similar electronic properties to In_2O_3 thin-film transistors⁴⁵ but have higher surface-to-volume ratios. The performance of these devices, such as the current on-to-off ratio, exceeded those previously reported for 1D nanowire-based devices fabricated via bottom-up approaches.^{15,16} High-performance In_2O_3 nanoribbon FETs can be used in a variety of applications, such as electronic devices and ultrasensitive FET-based pH, gas, chemical, and biological sensors, where the surface of In_2O_3 can be functionalized with a variety of molecules including antibodies and aptamers using linkers such as (3-aminopropyl)trimethoxysilane.^{45,57,59,65}

In summary, we report a high-throughput, large-scale strategy enabling fabrication of ultrathin, metal oxide nanoribbons that are readily integrated into devices. We leverage and extend the capabilities of CLL, in combination with selective etching processes, to pattern, successively, SAMs, metal films, and ultrathin layers of In_2O_3 to create arrays of periodic, 1D nanostructures. Nanoribbons fabricated by this approach are uniform and continuous over centimeter scales. We demonstrate high-performance FETs fabricated using In_2O_3 nanoribbons having carrier mobilities up to $13.7 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$ and on-to-off current ratios of $>10^7$. By employing widely available low-cost HD-DVDs as nanostructured master patterns, in conjunction with CLL, a scalable and high-fidelity chemical patterning technique that does not require sophisticated equipment and facilities, we lower barriers to nanostructure and device fabrication. The advances demonstrated here serve to extend large-area nanofabrication and to broaden application and user bases by providing alternative patterning strategies to photo- and electron-beam lithographies. This work provides a general approach for the facile and large-scale patterning of semiconductor 1D nanostructure arrays with high surface-to-volume ratios, which have a broad range of applications in electronic devices, optical devices, displays, and biochemical sensors.

■ ASSOCIATED CONTENT

Supporting Information

The Supporting Information is available free of charge on the ACS Publications website at DOI: 10.1021/acs.nanolett.8b02054.

Additional experimental details. Figures showing atomic force microscopy images, fabricated devices and test configuration, and a photograph of a representative device. (PDF)

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Author Contributions

The experiments were designed by C.Z., A.M.A., and P.S.W. Data were collected by C.Z., X.X., S.H.B., Q.Y., W.L., J.N.B., and K.M.C. and were analyzed by C.Z., X.X., Y.S.M., Y.Y., A.M.A., and P.S.W. Figures were prepared by C.Z. and X.X. The manuscript was written by C.Z., X.X., A.M.A., and P.S.W. with assistance from all other authors.

Notes

The authors declare no competing financial interest.

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