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PEDOT-PSS nanoribbon and cast film field effect transistors with ferroelectric gating

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ABSTRACT

Poly(3,4-ethylenedioxythiophene) doped with poly(styrene sulfonic acid) – PEDOT-PSS was electro-spun to produce high aspect ratio nano-ribbons. Individual nano-ribbons and cast films of varying thicknesses were electrically characterized in a field effect transistor configuration with ferroelectric poly(vinylidene fluoride-trifluoroethylene)-PVDF-TrFE as the gate insulator. The devices showed p-type behavior consistent with hole transport, and a ferroelectric memory effect. Thinner films exhibited stronger field effect compared to thicker films. As the thicknesses increased, relative changes in the gate induced currents decreased, while the threshold voltage and memory window width increased. The mobility was ~0.5 cm^2/V-s and the induced charge density was 2.3 x 10^{18}/cm^2 for the 10nm film device. A simple application of non-volatile charge storage was demonstrated via the use of ± 50V erase/write pulses applied to the gate. The device operated successfully with no degradation in the write/erase functionality, and is the first demonstrating a ferroelectric field effect in PEDOT-PSS thin films.

1. Introduction

Poly(3,4-ethylenedioxythiophene)-polystyrene sulfonic acid (PEDOT-PSS) is a commercially available p-doped conducting polymer. It is water soluble, highly conducting and has a band gap of ~1.6 eV. PEDOT-PSS exhibits good visible transmittance in spun coated thin films and a low oxidation potential makes it stable in air [1]. Because of its high conductivity, PEDOT-PSS is sometimes used as a hole transport layer or as metal contacts in a variety of polymer based electronic devices [2]. The current in PEDOT-PSS should be unaffected by an external electric field due to the large density of intrinsic charge carriers available and the screening of the electric field at the atomic scale. Several studies however have reported using PEDOT-PSS as the active material in an electrochemical transistor (ECT) [3–9]. In such a device, where an electrolyte is in contact with PEDOT-PSS, the mobile ions are directed toward the PEDOT-PSS/electrolyte interface by an external gate voltage. Some ions diffuse into and chemically react with PEDOT-PSS altering its conductivity. A few reports also show electrostatic doping in PEDOT-PSS as in a standard field effect transistor (FET) [10–12]. The critical difference between these two mechanisms (electrochemical vs. electrostatic) is the permeability of the PEDOT-PSS layer to the ions in the electrolyte. During ECT operation, the ions penetrate PEDOT-PSS to stabilize charge in the polymer resulting in a doping/de-doping process. In FET operation there is an electrostatic induction of charges into PEDOT-PSS and possible neutralization of PSS^- ions due to the high electric field at the PEDOT-PSS/gate insulator interface [11,12]. Recently, we reported observing both ECT and FET modulation of the current in a PEDOT-PSS nanoribbon via ionic liquid gel gating [13].

PEDOT-PSS is a very stable conducting polymer unlike other thiophene derivatives and is also not degraded after contact with some organic solvents. Finding novel applications for PEDOT:PSS is therefore very desirable. Herein we show once again an electrostatic field effect in PEDOT-PSS films using ferroelectric poly(vinylidene fluoride-trifluoroethylene)-PVDF-TrFE as the gate insulator. This is the first study to report on a ferroelectric field effect in PEDOT-PSS. The device exhibits non-volatile memory due to the ferroelectric properties of the gate. Thinner films have a much more pronounced field effect compared to thicker films, where it is negligible. Under normal operation at room temperature, the induced charge density is ~ 10^{18} holes/cm^2 and the mobility is ~ 0.5 cm^2/V-s for the 10 nm thin film device. In addition, the memory window width increased from 31 V to 91 V as the film thickness increased from 10 nm to 800 nm respectively. An application taking advantage of the non-volatile functionality of this device operating for several write/erase cycles is demonstrated. Lastly, since PEDOT-PSS is sometimes used as metal contacts in organic devices, we suggest that only thick films (> 1μm) be used in order to avoid detrimental effects of unintentional electrostatic doping of the polymer.

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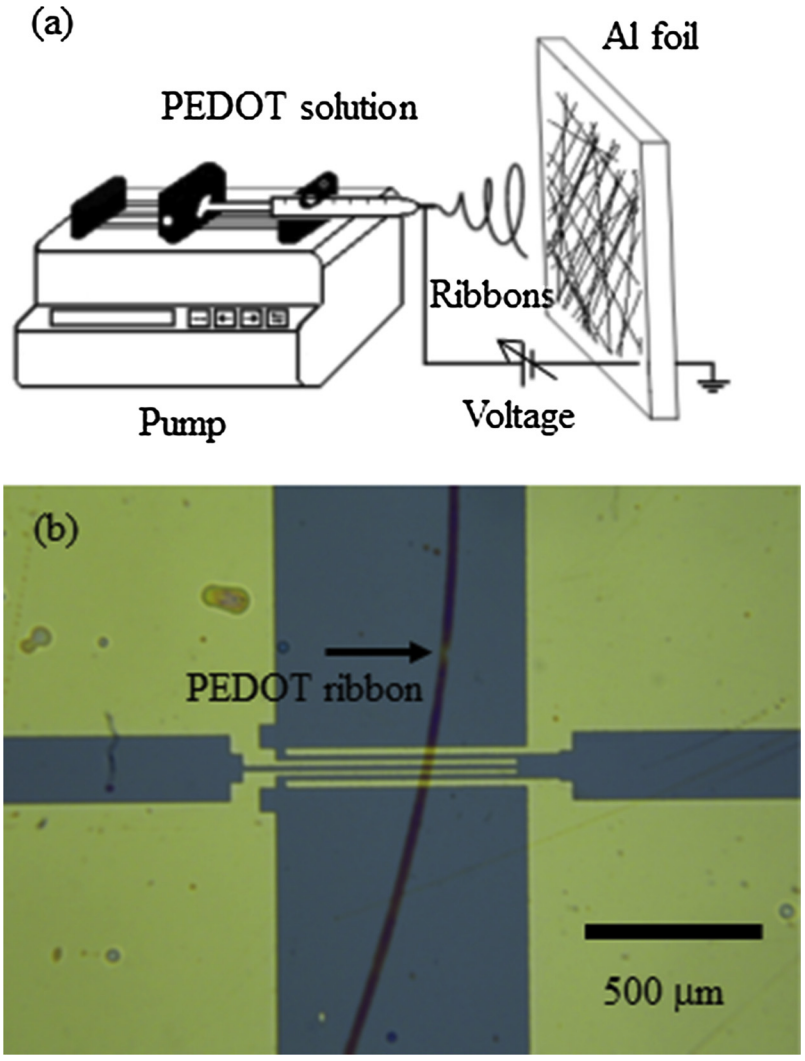

Fig. 1. (a) Basic electrospinning apparatus for fabricating polymer nano-ribbons. (b) An electro-spun PEDOT-PSS nanoribbon captured on a pre-patterned Si/SiO_2 substrate. The ribbon sticks firmly to the substrate and cannot be moved without causing permanent damage.

2. Experimental

PEDOT-PSS was obtained from Agfa Gevaert N.V. and used as received. It is a water soluble complex that is chemically stable under normal laboratory conditions. Nano-ribbons of this polymer were fabricated via electrospinning [13–17]. Fig. 1(a) shows the schematic diagram of the electrospinning apparatus. The main elements include a hypodermic needle (½ cc tuberculin syringe), a syringe pump, a high voltage power supply and an Al foil. In its present form as purchased, PEDOT-PSS does not have the right consistency to form nano-ribbons. In order to fabricate nano-ribbons, a 1 wt% of polyethylene oxide (PEO) (MW:2×10^6) was dissolved in it. PEO makes the solution viscous and acts as a plasticizer. To prepare nano-ribbons, the hypodermic needle is filled with the PEDOT-PSS/PEO solution and placed on the syringe pump programmed to allow a flow rate of 0.2 mL/h. The needle is connected to the positive terminal of the power supply and the negative to an Al foil shown in Fig. 1(a). As the voltage to the needle is increased, the electrical forces on the droplet at the needle end overcome the surface tension. This results is a fine jet driven from the tip of the needle toward the grounded Al foil. As the solvent evaporates, fine ribbons of the polymer are seen to deposit themselves randomly on the Al foil. In order to capture isolated ribbons, a pre-patterned Si/SiO_2 wafer was quickly passed between the needle tip and Al foil, perpendicular to the path of the jet in a downward sweeping action. This resulted in several isolated ribbons sticking to the substrate, some of which lie across the pre-patterned electrodes as seen in Fig. 1(b). The substrate is then placed in an oven at 70 °C for several hours to remove all moisture. The ribbons stick to the substrate firmly and cannot be removed without causing permanent damage to them. Atomic Force Microscope measurements on the electro-spun PEDOT-PSS show a ribbon like surface profile unlike fibers which tend to be more cylindrical [18].

Poly(vinylidene fluoride-trifluoroethylene)-PVDF-TrFE (75/25) is a room temperature ferroelectric copolymer [19] and was purchased from Kureha, Japan. A 9 wt% of this polymer dissolved in N,*N*,-dimethylformamide (DMF) was prepared and spin coated to form the gate insulator in a FET configuration. Fig. 2(a) shows a top view optical microscope image of an isolated PEDOT-PSS nano-ribbon (thickness 10 nm) lying on the pre-patterned Si/SiO_2 substrate. This PEDOT-PSS film (i.e. channel) touches two Au electrodes (source (S) and drain (D)) of the device as seen within the black circle. A thin film (800 nm) of PVDF-TrFE was subsequently spin coated (4000 rpm/45 s) over the substrate and dried in an oven at 70 °C for 24 h to remove trace amounts of DMF. Fig. 2(b) shows the same substrate in 2(a) after coating with PVDF-TrFE. Using a slit in an Al foil as a shadow mask, a narrow fringe of Ag was thermally evaporated to cover the nanoribbon and was used as the gate (G) electrode as seen in Fig. 2(c). Fig. 2(d) shows a schematic structure of the top gated FET with all the components labelled. In this study, PEDOT/PSS ribbons of thickness 10 nm, 300 nm and

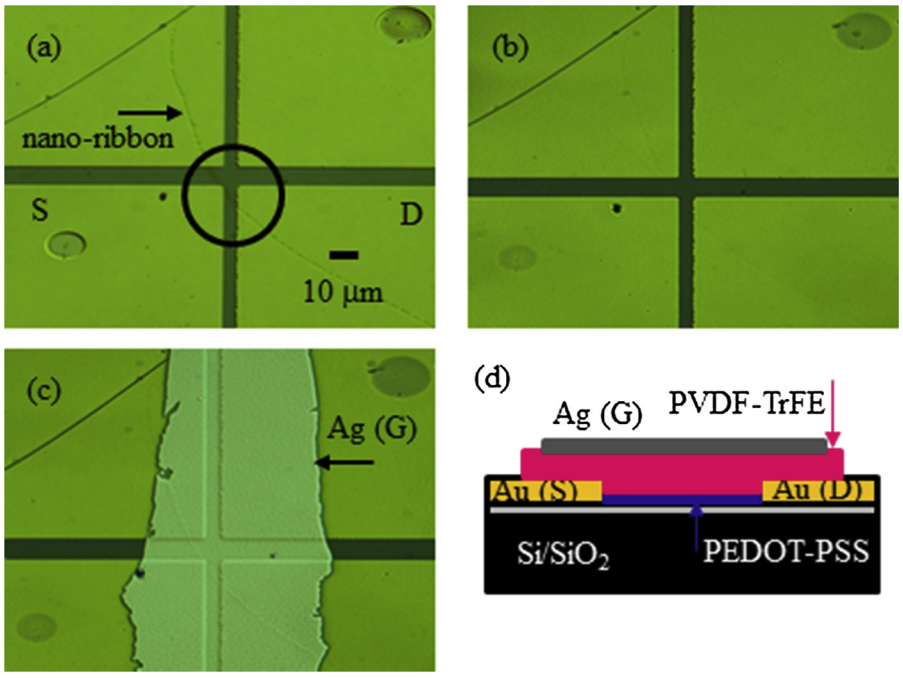

Fig. 2. (a) Optical microscope image of an electro-spun PEDOT-PSS nano-ribbon (inside black circle) making contacts to three separate Au electrodes. Two of them are the source and drain terminals of the device. (b) Same as in (a) but after spin coating a uniform thin film of PVDF-TrFE. (c) Same as in (b) but after thermal evaporation of the Ag film over the PEDOT-PSS nano-ribbon. This is the gate electrode of the device. (d) Schematic diagram showing the cross-section of the device and the various components.

Table 1
Tabulated values of the dimensions and of the calculated parameters related to the operation of each device. L = channel length, W = channel width, t = channel thickness, R = channel resistance at zero gate, V_{TH} = threshold voltage, μ = mobility, n = charge density, ΔI = relative current change, ΔV_m = memory window width. The dashes imply that no value could be determined from the data.

PEDOT-PSS Shape	Length L (μm)	Width W (μm)	Thickness t (nm)	R (Ω)	V_{TH} (V)	μ (cm^2/V-s)	n (holes/cm^2)	ΔI/I	ΔV_m (V)
Ribbon	6	2	10	1.8×10^6	4.5	0.5	2.3×10^{18}	104	31
Ribbon	2	6	300	5.0×10^3	21.3	2.7	1.3×10^{19}	37	86
Ribbon	4	50	800	4.8×10^2	26.0	0.3	–	2	97
Drop	10	400	1300	6.5×10^1	–	–	–	0	–

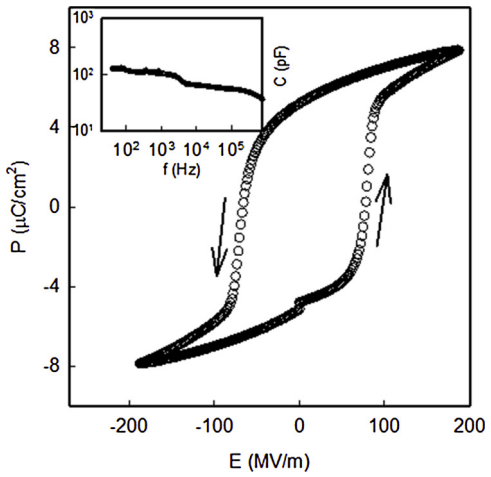

Fig. 3. Ferroelectric hysteresis loop for a PVDF-TrFE thin film used as the gate insulator in the device measured at 1 Hz. The inset shows the frequency dependent capacitance of the PVDF-TrFE thin film. At 40 Hz the capacitance approaches a value of 128 pF.

800 nm were prepared via electro-spinning, while thickness of 1300 nm was a drop cast film. The electro-spinning technique produces ribbons with a range of widths and thicknesses. The length of the ribbons however is several millimeters to centimeters long, and we assume that over the distance between the S/D electrodes (a few microns) of each device, the thickness variation of the ribbon is insignificant. The device fabrication process for the 300 nm, 800 nm and 1300 nm films follow the same method as described above for the fabrication of the 10 nm device. Table 1 summarizes pertinent information about the devices. The differences in channel length (L) and width (W) for the devices did not affect device performance or parameter computation.

Electrical characterization was performed using a Keithley electrometer model 6517 A for the drain-source voltage (V_{DS}) and drain-source current (I_{DS}), while a Keithley source meter model 2400 supplied the gate voltage (V_{GS}) and measured the leakage current (I_{GS}). An Agilent Technologies model 4294 A Impedance Analyzer and a Radiant Technologies Model RT66C Precision Materials Analyzer was used to characterize the ferroelectric copolymer. All measurements were carried out at room temperature in a closed chamber under vacuum of 10^{-2} Torr to avoid the effects of adsorbed moisture.

3. Results and discussion

Electrostatic doping in a FET is a result of capacitive coupling between the gate terminal and the active semiconducting material between the source and drain terminals. Prior to device characterization the ferroelectric nature of PVDF-TrFE was investigated. A capacitor with a spin coated thin film of PVDF-TrFE (thickness 800 nm) sandwiched between metal electrodes was fabricated and had an effective surface area of $\sim 1.1 \times 10^{-3}$ cm^2. Its polarization and capacitance were then measured as a function of frequency. Fig. 3 shows the ferroelectric polarization (P) vs. applied electric field (E) of this capacitor measured

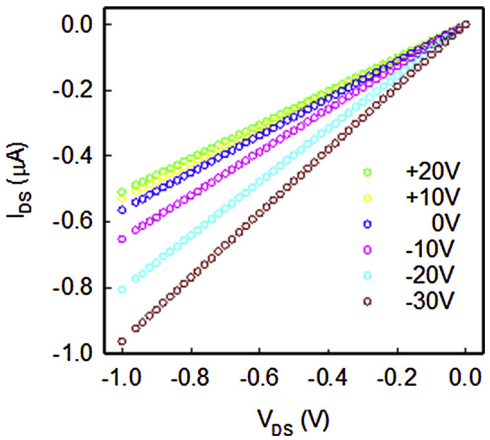

Fig. 4. I_{DS} vs. V_{DS} for the device shown in Fig. 2(c) for different V_{GS}. An increasing negative V_{GS} increases I_{DS} and an increasing positive V_{GS} decreases I_{DS}.

at 1 Hz. The coercive electric field was seen to be ~75 MV/m. The counterclockwise hysteresis loop seen in Fig. 3 shows a remnant polarization of ~5μC/cm^2 and is similar to previous results on this copolymer [20,21]. The saturated hysteresis curve in Fig. 3 demonstrates that the PVDF-TrFE used in the device is ferroelectric, and is capable of retaining polarization in the absence of an electric field. The inset to Fig. 3 shows the variation of the capacitance with frequency. A value of 128 pF was approached at 40 Hz while at higher frequencies the capacitance gets smaller [19]. The specific capacitance of this material was calculated to be 1.2 × 10^{-7}F/cm^2.

Fig. 4 shows the drain-source current (I_{DS}) versus the drain-source voltage (V_{DS}) of the device shown in Fig. 2(c) for various top gate voltages (V_{GS}). As the gate is made more negative, I_{DS} increases for increasing negative V_{DS}. This is consistent with the p-doped nature of PEDOT-PSS where the majority carriers are holes [22]. At V_{GS} = 0 V the channel resistance was calculated to be 1.8MΩ yielding a conductivity of 1.7 S/cm which rises to 3 S/cm when V_{GS} = -30 V due to the gate induced charges, comparable to previous measurements [15]. The linear variation of I_{DS} with V_{DS} for all gate voltages, and the high conductivity shows that the contact resistance between PEDOT-PSS and the metal electrodes is Ohmic and is negligible compared to the channel resistance. Applying a positive voltage to the gate reduces I_{DS} as seen in Fig. 4.

PEDOT-PSS thin films are known to have a morphology where there is a segregation of PEDOT-PSS rich clusters that are surrounded by weakly conducting PSS^- anionic shells [23]. The PEDOT-PSS rich clusters are believed to be crystalline and highly conducting. They act to screen the effects of an external electric field to modulate the current transported within the clusters. Bulk charge transport however is controlled by the weakly conducting PSS^- rich amorphous regions between the highly conducting clusters. The electric field due to the gate voltage was proposed to affect charge transport in this amorphous region [24] resulting in electrostatic current modulation as seen in Fig. 4 and explained below. Since the gate insulator does not contain mobile ions, the observed effect is electrostatic and not electro-chemical.

In order to study the effect of ferroelectric gating on device operation, the trans-conductance curve was measured. Fig. 5(a) shows the variation of I_{DS} with V_{GS} while V_{DS} was held constant at -1V in the same device as in Fig. 4. V_{GS} was swept in the following sequence: 0 → $+V_{GSmax}$ → $-V_{GSmax}$ → 0 at a rate of 40mV/s. A slight difference is observed in the current after the sweep due to incomplete polarization recovery in the gate insulator. The ON and OFF currents correspond to the maximum and minimum currents indicated in Fig. 5(a). The device is in the normally ON state in the absence of a gate voltage due to the intrinsic conductivity of PEDOT-PSS. V_{TH} is defined as the minimum gate threshold voltage required to initiate a rapid decrease in the

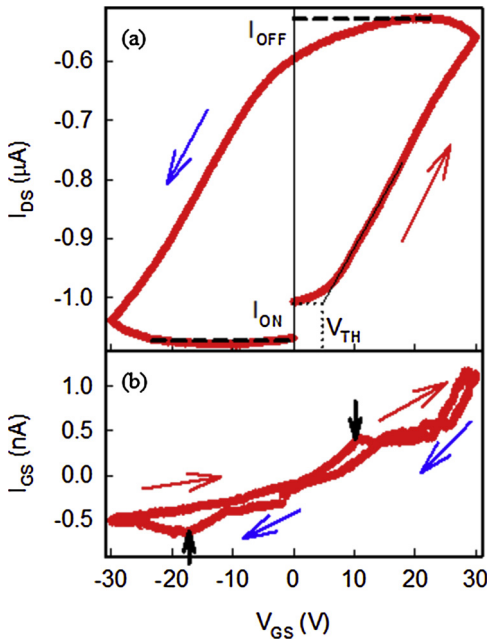

Fig. 5. (a) Device trans-conductance curve I_{DS} vs. V_{GS} for a fixed V_{DS} = -1 V. I_{OFF} and I_{ON} represents the minimum and maximum currents recorded during the gate sweep. These currents retain their values even when the gate voltage is reduced to zero. V_{TH} is the threshold voltage below which the current decreases sharply as the gate voltage is decreased. (b) The gate leakage current as a function of gate voltage. The leakage currents are several orders of magnitude smaller than the channel current and do not affect device performance. The **black** arrows indicates peaks related to electrostatic doping.

channel current from the ON to the OFF state. Fig. 5(a) shows how this parameter is determined. Two important features of this plot are the counterclockwise hysteresis behavior and the p-type response of the current to the gate voltage. The decrease(increase) in I_{DS} with positive (negative) V_{GS} is consistent with the I_{DS} vs. V_{DS} plot in Fig. 4 and the fact that the charge carriers in PEDOT-PSS are holes [22]. In addition, we observe a never before reported hysteresis effect in PEDOT-PSS due to the ferroelectric property of the gate insulator. Under zero gate voltage the device is normally ON as mentioned above. As the gate is made more positive, the electric field across the PVDF-TrFE film begins to polarize (down) [21] the dipoles within it, consistent with the polarization plot of Fig. 3. This resulted in a net positive bound charge at the interface with PEDOT-PSS, reducing channel conduction by increasing the barrier for hole injection into the polymer at the S/D contacts. The bound charge could also neutralize the PSS^- anionic shells making it harder for charge transport through the amorphous regions of the polymer. The result is lower measured current and the device is turned OFF at V_{GS} = +30V. Reducing the gate voltage to zero left a remnant polarization in PVDF-TrFE that maintained the channel current in the OFF state. As the gate voltage was made negative and exceeded the coercive voltage, the polarization changed direction (up) again. Now, a net negative bound charge at the interface with PEDOT-PSS increased channel conduction by reversing the changes brought about by the positive bound charge and returning the device to the ON state. The device stays ON even as the gate voltage is brought back to zero. Increasing V_{GS} above 0V once again repeats the process. When V_{GS} exceeded the coercive voltage, the polarization switched direction again and the device was turned OFF. The memory window width (ΔV_m) for this device was 31V and corresponds to the mid-section width of the hysteresis curve in Fig. 5(a). Fig. 5(b) shows the gate leakage current that is much lower than the channel current and hence leakage does not influence device operation. The presence of peaks in Fig. 5(b) however is another indication of electrostatic doping via charge injection into the channel at negative or positive gate bias [13,25]. Using a

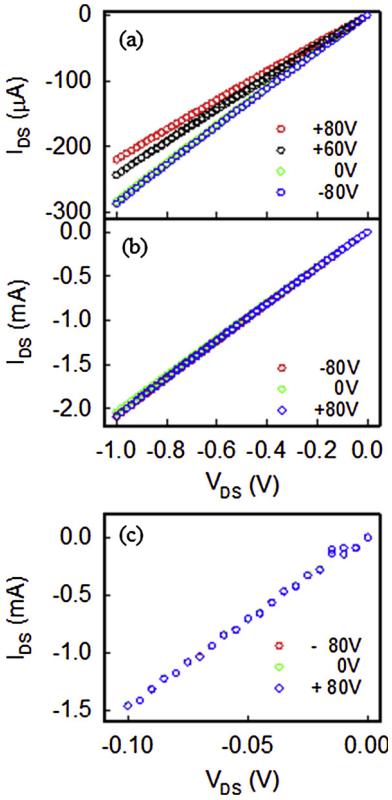

Fig. 6. I_{DS} vs. V_{DS} curves for different specified gate voltages for devices having varying PEDOT-PSS channel thickness (a) 300 nm, (b) 800 nm (c) 1300 nm. The drain-source voltage in (c) was not increased beyond -0.1 V in order to not exceed the instrument current limit (± 10 mA).

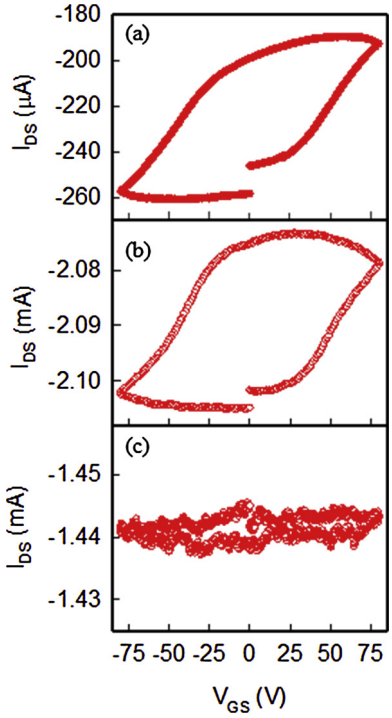

Fig. 7. Device trans-conductance curves I_{DS} vs. V_{GS} for devices having varying PEDOT-PSS channel thickness (a) 300 nm, (b) 800 nm (c) 1300 nm. V_{DS} was held fixed at -1 V for 300 nm and 800 nm device and at -0.1 V for the 1300 nm device during the measurement.

gate voltage sweep rate of 40mV/s, we calculate the area under the I_{GS} vs. t curve corresponding to the negative peak in Fig. 5(b) of 44 nA-s [25]. From this value the induced charge density ($= \frac{\int I_{GS}dt}{Gated\ area}$) is $2.3x10^{18}$ holes/cm^2 at a gate voltage of -18V and is higher than that reported earlier for a lower gate voltage [13].

It has been reported that the electric field effect in 2-D organic semiconductors is confined inside the semiconductor film near the interface with the gate insulator [26]. In order to corroborate this effect in PEDOT-PSS, devices with varying thicknesses were fabricated and studied. Fig. 6(a)–(c) shows the device (I_{DS}-V_{DS}) characteristics for film thicknesses of 300nm, 800nm and 1300nm respectively. The changes in I_{DS} (for a fixed V_{DS}) as the gate voltage is changed, decrease as the film thickness get thicker. Thicker films also needed a larger gate voltage to observe the field effect. For the thickest film the current stays the same for all gate voltages (i.e. no observable change in the slope) as seen in Fig. 6(c). The applied V_{DS} was only increased up to 0.1V (Fig. 6(c)) so as not to exceed the current limit of the electrometer (10mA) at V_{DS} = 1V. Fig. 7(a)–(c) shows the trans-conductance curve of the corresponding devices as seen in Fig. 6. Here too one notices that the field effect gets smaller as film thickness in increased i.e. the ON and OFF currents cannot be distinguished for the thickest film. The width of the hysteresis (memory window: ΔV_m) I_{DS} vs. V_{GS} curves also get wider as the film gets thicker. The relative changes in the current ($I_{DS/ON}$ - $I_{DS/OFF}$)/$I_{DS/OFF}$ i.e. ΔI/I gets smaller as the film thickness is increased. This is consistent with the observation that the field effect is confined to the polymer layers near the PVDF-TrFE interface. For thicker films, it implies that I_{DS} flows relatively unaffected through the bulk of the film away from the interface, hence the weaker field effect. It also means that a higher voltage (i.e. V_{TH} increases) is needed whose field effect penetrates deeper into the PEDOT-PSS channel to affect changes in I_{DS}.

The device trans-conductance curves were analyzed to extract the mobility (μ) in the PEDOT-PSS active layer of each device. As seen in Figs. 4 and 6, the current does not saturate up to V_{DS} = -1 V and therefore the device operates in the linear regime. In such cases, the trans-conductance (g_m) was calculated from the linear portion of the I_{DS} vs. V_{GS} curves in Figs. 5 and 7 as follows [27]:

$$g_m = \frac{\partial I_{DS}}{\partial V_{GS}};\ V_{DS}\,constant$$

From which the charge mobility was calculated using:

$$\mu = \frac{g_m L}{W C_i V_{DS}}$$

where L and W are the channel length and width respectively. C_i is the specific capacitance of the gate insulator (1.2×10^{-7}F/cm^2). As seen in Figs. 5 and 7, g_m is the same for each device in the ON to OFF and the OFF to ON portions of the corresponding curves i.e. the slopes are similar. This indicates that the electrostatic charge injection into the PEDOT/PSS channel is symmetric and reversible. It also suggests that the electrical contacts of the drain and source electrodes with PEDOT-PSS, and the electrical contact of PDVF-TrFE with the drain, source and gate electrodes were symmetric. Mobility values for the different devices are tabulated in Table 1 and show a maximum value of ~2.7 cm^2/V-s for the 300 nm thick channel. For thinner films, charge trapping and scattering due to phonons will lower the mobility since there are fewer pathways to circumvent these defects. For thicker films, a conducting channel between S/D electrodes away from the PEDOT-PSS/PVDF-TrFE interface is unaffected by the electric field. This permits a field independent current to flow in PEDOT-PSS leading to lower g_m. Since no current saturation was observed in the device characteristics, V_{TH} is determined as the minimum gate voltage that results in rapid changes to the channel current. This value increases as film thickness increases due to the limited penetration of the field effect into the film. For the film with thickness of 1300 nm, there was no observable field effect as seen in Fig. 7(c) and hence μ together with a few other parameters could not be determined. The device dimensions, charge mobility,

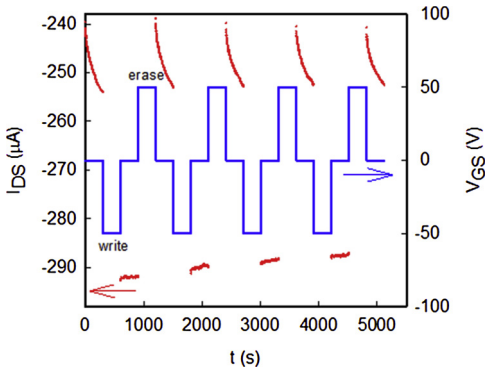

Fig. 8. Write/erase operation using the (300 nm) PEDOT-PSS ferroelectric FET. V_{DS} is fixed at -1 V. A -50 V write pulse is applied to the gate for 300 s and then turned off for 300 s. The current stays high (write) during this period (write). Then a +50 V erase pulse is applied to the gate for 300 s and turned off for 300 s. The current stays low (erase) during this period. These write/erase cycles can be switched for several minutes and the device still retains well defined high and low current values.

charge density, relative current changes, threshold voltage and memory window width are all tabulated in Table 1. One observes from this Table that thin PEDOT-PSS films (< 1μm) show electrostatic field effect while thicker films (> 1μm) do not, and are more appropriate for use as metal contacts in organic electronics.

The I_{ON}/I_{OFF} ratio of the PEDOT-PSS FET is limited due to the high current in the OFF state. Using a ferroelectric gate however, offers the advantage of a possessing a polarization based non-volatile memory effect. The trans-conductance curves of Figs. 5 and 7 show that I_{DS} has two distinct values at zero gate voltage. This motivated us to test the FET as a memory device for write/erase functionality. Fig. 8 shows the plot of I_{DS} as a function of time (V_{DS} = -1 V fixed) as erase and write pulses (± 50 V) were applied to the gate terminal. A recording period of 300 s was allowed for the write/erase operation followed by 300 s of storage time. Applying -50 V to the gate initiates the write cycle, after this pulse is turned off (300 s), the current stays recorded at its maximum value. A +50 V erase pulse is then applied to erase the written information and the current is reduced. When this pulse is turned off (300 s) the current stays low, although a slow increase in the current is observed. These write/erase cycles were applied to the device for several minutes. As seen in Fig. 8, there is a clear separation between the write and erase recorded currents. This is the first study to show that PEDOT/PSS with ferroelectric gating is capable of operating as a non-volatile memory chip in electronic devices.

4. Conclusions

We report electrostatic doping in electro-spun PEDOT-PSS nano-ribbon and thin film field effect transistors via ferroelectric gating. The devices could be turned OFF by applying a positive gate voltage and maintained in that state upon its removal. Applying a negative gate voltage reversed the effect. Electrostatic doping was also observed in PEDOT-PSS films of different thicknesses. As the thicknesses increased however, relative changes in the gate induced currents decreased while the threshold voltage and memory window width increased. This is consistent with the limited penetration of the field effect into the film. The mobility was ~0.5 cm^2/V-s and the induced charge density was $2.3 \times 10^{18}/cm^2$ for the 10 nm film device. A simple application of non-volatile charge storage was demonstrated via the use of ± 50 V erase/write pulses applied to the gate. The device operated successfully for several minutes with no degradation in the write/erase functionality, and is the first demonstrating a ferroelectric field effect in PEDOT-PSS thin films. Lastly, our results suggest that only thick PEDOT-PSS films be used as metal contacts in conducting polymer devices.

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