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Germanium Quantum-Well Josephson Field-Effect Transistors and Interferometers

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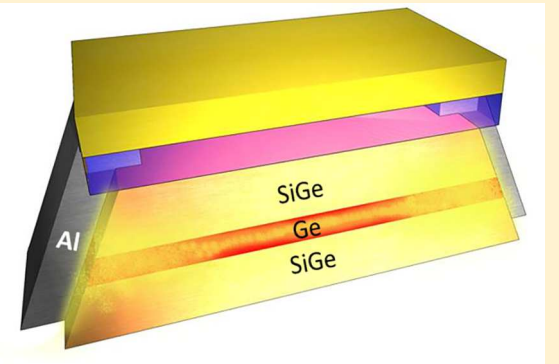
S *Supporting Information*

ABSTRACT: Hybrid superconductor−semiconductor structures attract increasing attention owing to a variety of potential applications in quantum computing devices. They can serve the realization of topological superconducting systems as well as gate-tunable superconducting quantum bits. Here, we combine a SiGe/Ge/SiGe quantum-well heterostructure hosting high-mobility two-dimensional holes and aluminum superconducting leads to realize prototypical hybrid devices, such as Josephson field-effect transistors (JoFETs) and superconducting quantum interference devices (SQUIDs). We observe gate-controlled supercurrent transport with Ge channels as long as one micrometer and estimate the induced superconducting gap from tunnel spectroscopy measurements. Transmission electron microscopy reveals the diffusion of Ge into the Al contacts, whereas no Al is detected in the Ge channel.



KEYWORDS: *superconducting quantum interference device, two-dimensional hole gas, proximity-effect-induced superconductivity, Josephson field-effect transistor, Ge quantum well*

Modern quantum nanoelectronics take increasing advantage of newly synthesized hybrid superconductor−semiconductor (S−Sm) interfaces.[1] One of the main motivations is the search for Majorana zero modes that are predicted to appear in a topological superconductor.[2−6] A Josephson field-effect transistor (JoFET) is one of the basic devices. It consists of a gate-tunable semiconductor channel allowing Cooper-pair exchange between two superconducting contacts mediated by the superconducting proximity effect.[7] Gate control on the Josephson coupling has eventually led to the realization of electrically tunable transmon quantum bits, now often referred to as gatemons.[8−10]

Many of the reported experimental realizations of hybrid S−Sm devices rely on bottom-up fabrication starting from semiconductor nanowires or carbon nanotubes.[11−21] Recently, new hybrid S−Sm devices were demonstrated using top-down fabrication processes based on two-dimensional systems made of graphene,[22] InAs,[23,24] GaAs,[25] InGaAs,[26] or Ge/SiGe.[27,28]

Top-down nanoscale devices offer significant advantages in terms of complexity and scalability. Those based on p-type SiGe heterostructures are readily compatible with silicon technology,[29] and thanks to their intrinsically strong spin−orbit coupling, they are an attractive candidate for the development of topological superconducting systems.[27,30−37]

In this work, we present proof-of-concept S−Sm devices in which the semiconducting element consists of an undoped SiGe heterostucture embedding a strained Ge quantum well (QW). A high-mobility two-dimensional hole gas (2DHG) is electrostatically accumulated in the QW by means of a surface gate electrode. Hole mobilities as high as 5×10^5 cm^2/(V s) were reported for similar heterostructures.[15,27,38,39] The superconducting proximity effect induces gate-tunable superconductivity in the 2DHG, enabling JoFET operation. This functionality is exploited for the realization of gate-controlled superconducting quantum interference devices (SQUIDs). Finally, we present tunnel-spectroscopy measurements of the induced superconducting gap as well as a microscopic

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inspection of the S−Sm interface by cross-sectional transmission electron microscopy.

All devices have Al superconducting leads deposited on the sidewalls of a wet-etched mesa structure. The etching process yields a sidewall slope of $\theta \approx 10°$ which enables direct side contacts to the QW (Figure 1 (a,b)). The channel length, L, defined by the distance between the two Al/Ge contacts, ranges between 0.6 and 1 μm. The surface gate electrodes are made of Ti/Au and are fabricated after the atomic layer deposition (ALD) of an insulating oxide layer (Figure 1(c)). We distinguish between two types of top gates, namely, those aimed at inducing hole accumulation to create a conducting hole channel and those aimed at causing local charge depletion resulting in a tunnel barrier.

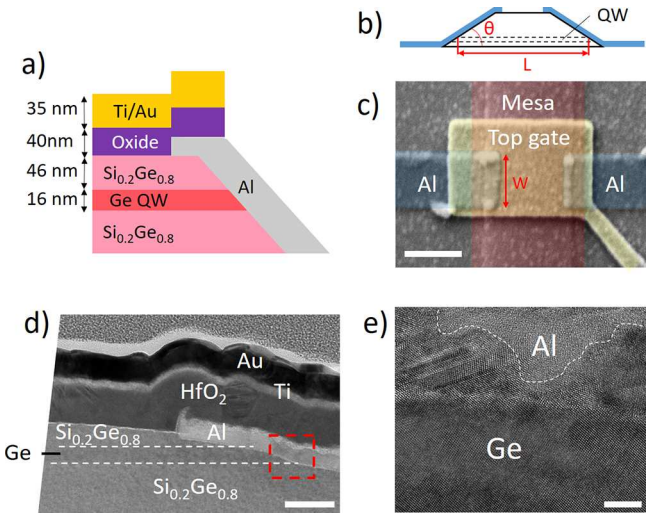

Figure 1. (a and b) Schematic cross section of the quantum-well and device structure. (c) False color SEM picture of a device consisting of a top gate covering two Al contacts and a mesa. The scale bar is 500 nm. (d) TEM cross-sectional image of a single-junction device cut at the level of the Al−Ge QW junction. The scale bar is 50 nm. (e) High-resolution TEM image of the Ge−Al interface in the area inside the red dashed square in panel (d). The scale bar is 5 nm.

We investigate the interface between the Al contacts and the Ge QW with TEM analysis. First, we observe direct contact between the Al and the QW (Figure 1 (d)). Second, diffusion of Ge atoms into the Al layer is found at the Al/QW interface, seen as the darker contrast in Figure 1 (d and e) on the Al side opposite of the QW and confirmed by EDS analysis (additional results in Figure S1 of the Supporting Information). We speculate that this occurs during the gate oxide deposition by ALD, when the samples are heated at 250 °C for 2.5 h. Under similar conditions, the diffusion of Al (or Pt) atoms through a SiGe barrier into the Ge QW has been observed and used to produce low-resistivity electrical contacts from the top.[16−18,27,38,40] In general, interdiffusion at the S−Sm interface can lead to high critical supercurrents due to reduced interface resistance. However, we do not find evidence of Al diffusion down through the SiGe barriers or from the side directly into the Ge QW in these devices.

In order to demonstrate JoFET functionality, we perform two probe transport measurements on a single junction device at 15 mK using a standard lock-in technique. The sample is in series with low-temperature RC filters and high-frequency filters. All transport data shown in this Work are corrected to remove the contribution from the total series resistance of the measurement circuit (about 45 kΩ).

Figure 2(a) shows a measurement of differential resistance (dV/dI) as a function of bias current I and top-gate voltage V_g

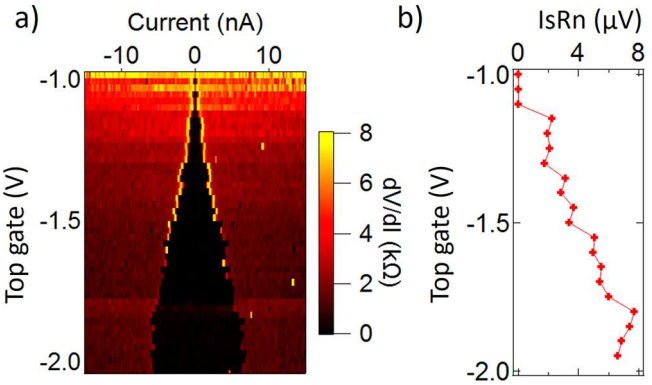

Figure 2. (a) Differential resistance of the single-junction device versus top-gate voltage and current. (b) The product of I_sR_n versus gate voltage from the results presented in panel (a).

in a single-junction device similar to the one shown in Figure 1(c) with $L = 1$ μm. A negative top-gate voltage of $V_g < -0.9$ V induces the accumulation of holes in the strained Ge channel, as revealed by the onset of channel conduction. Note that the gate-induced electric field is partially screened at the contacts due to the Al source and drain electrodes partially overlapping the mesa. Nevertheless, this does not appear to prevent the injection of holes from the Al electrodes. As V_g is made increasingly negative, the zero-bias device resistance drops and eventually vanishes (this enables an accurate measurement of the circuit series resistance). Above a switching current I_s, the device resistance takes a finite value R_n of the order of a few kiloohms (kΩ).

As V_g is tuned toward more negative values, I_s increases while R_n decreases. The observed gate-voltage dependence of I_s demonstrates JoFET operation. I_s and dV/dI are roughly symmetric around zero bias, which is characteristic of an overdamped regime. The product of I_sR_n reaches the highest value of about 8 μV for the most negative gate voltages (Figure 2(b)). The observed I_sR_n is similar to the values recently reported for Ge 2DHG devices[27] but is small in comparison to those reported for Ge−Si core−shell nanowires.[17,18,20] We estimate the hole mean free path of the channel on the order of $l_h = 2$ μm (see the Supporting Information), which is consistent with a ballistic junction. This gives a Thouless energy around $E_{th} \approx 100$ μeV, which is considerably larger than the I_sR_n product. This estimation suggests that I_s is mainly limited by the contact transparency. The influence in the contact transparency of the Ge diffusion in the Al and the electrostatic screening of the gate by the source and drain electrodes are not fully understood. This should be further investigated in the future with various device geometries and fabrication recipes.

Next, we present the realization of SQUIDs consisting of two independently controlled JoFET positions in the two arms of a superconducting Al ring with an inner (outer) surface area of about 12 (27.5) μm^2 (Figure 3 (a)). The JoFET layout in this SQUID geometry is noticeably different from the one discussed above (Figure 1(c)). In fact, both superconducting contacts and the accumulated hole channel in between now lie

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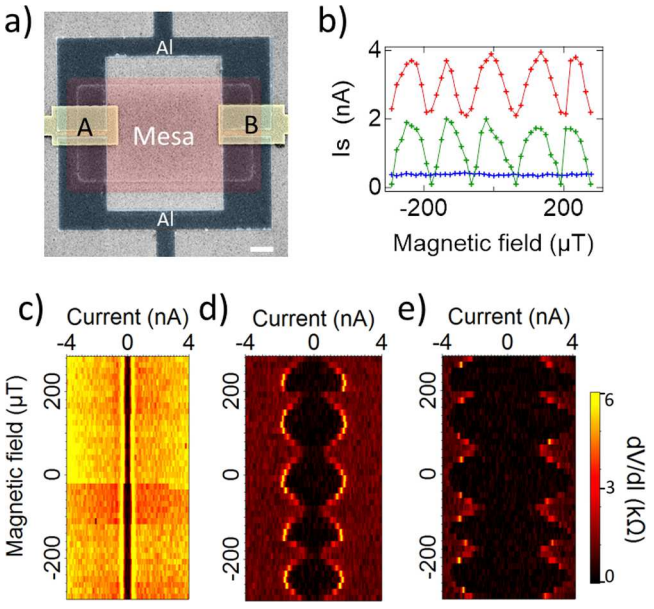

Figure 3. (a) False color SEM picture of a SQUID device. The scale bar is 1 μm. (b) Switching current versus magnetic field in three different regimes obtained from differential resistance measurements shown in (c) blue, (d) green, and (e) red. (c–e) Differential resistance versus current and magnetic field measured for gate A = −980 mV and different settings of gate B = −300 mV (c), −500 mV (d), and −600 mV (e).

on the same edge of the mesa. This geometry is less susceptible to the screening of the gate-induced electric field by the Al contact electrodes. On the other hand, the hole mobility in the Ge channel is most likely lowered by the proximity to the mesa edge.

To investigate SQUID operation, we measure dV/dI in a four-probe configuration and apply a magnetic field, B, perpendicular to the device plane. We begin by characterizing one Josephson junction at a time. This is straightforward since the junctions are off (i.e., fully insulating) when no voltage is applied to the respective gates. We find that both junctions have I_sR_n values consistent with those obtained for the device geometry of Figure 2. The results are presented in Figure S2 of the Supporting Information.

When both junctions are simultaneously on (i.e., in the superconducting regime), we can observe periodic SQUID oscillations in the switching current as a function of the out-of-plane magnetic field. Representative results are given in Figure 3(c–e), which shows color maps of dV/dI as a function of bias current and B. The three data sets are obtained with a fixed voltage on gate A, turning the left junction on, and three different voltages on gate B, resulting in correspondingly different values of the switching current in the right junction.

We note that when the right junction is off, the supercurrent is carried uniquely by the left junction, and I_s shows no B-induced oscillations (Figure 3 (c)).

When both junctions are turned on, I_s exhibits pronounced periodic oscillations (Figure 3 (d)). The modulation period $\Delta B_0 \approx 120\,\mu$T corresponds to a magnetic flux quantum $h/2e$ threading an area of 17.2 μm^2, which is consistent with the size of the Al ring. At the minima, I_s is close to zero, suggesting that for these gate voltages the two junctions have approximately the same critical current.[41] The full set of measurements is available in Figure S3 of the Supporting Information.

After the voltage on gate B is tuned to further negative values, the right junction becomes dominant and the SQUID is no longer balanced, as shown in Figure 3 (e) . In this configuration, the average value of I_s increases while the oscillation amplitude, which is determined by the smaller critical current of junction A, remains the same, as in Figure 3(d).[42] As a consequence, I_s values no longer vanish at the minima.

In order to probe the superconducting gap Δ^* induced in the Ge 2DHG, we use a JoFET with a constriction in the accumulation top gate and additional side gates designed to create a quantum point contact with tunable transmission (Figure 4(a)). In an earlier work,[37] the same device geometry

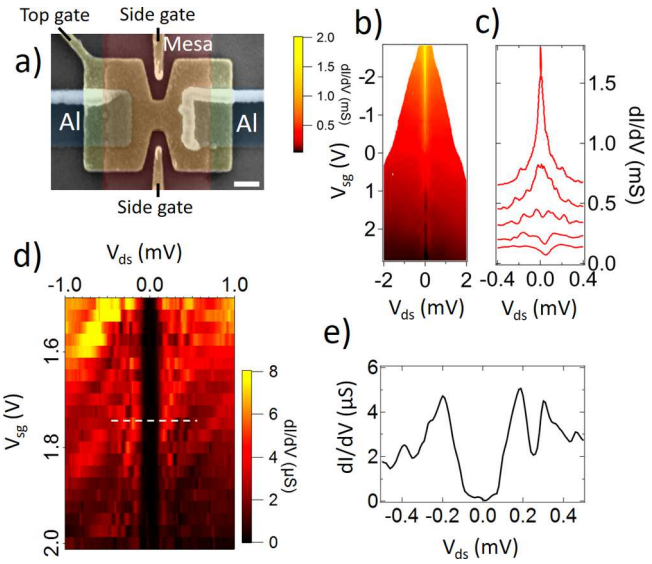

Figure 4. (a) False color SEM picture from the side gate device. The scale bar represents 200 nm. (b) Differential conductance versus side gate voltage and bias voltage measured in a 3He fridge at 258 mK with a top-gate voltage of −1.8 V. (c) Differential conductance line cut of panel (b) from V_{sg} = 2 V (bottom curve) to V_{sg} = −2 V (top curve) by steps of 0.5 V. The central picture of the V_{sg} = −2 V curve is attributed to a superconducting transition. (d) Differential conductance versus side gate voltage and bias voltage, measured in a dilution fridge at 17 mK, at a top-gate voltage of −1.41 V. (e) Line cut of panel (c) at the side gate voltage indicated by the white dash line at V_{sg} = 1.7 V.

was used to demonstrate conductance quantization in nonsuperconducting quantum point contact devices. In the regime of full depletion, the potential barrier at the constriction can be used to perform tunnel spectroscopy of the local density of states.

As before, the top gate is negatively biased in order to accumulate holes and make the channel a conducting channel. Then, we apply a positive voltage V_{sg} to both side gates simultaneously. As V_{sg} increases the differential conductance, dI/dV values drop since the transmission of the junction is reduced (Figure 4(b)). At low bias V_{ds} = −0.2 and 0.2 mV, we can see features characteristics of normal superconducting junctions (Figure 4(c)). For negative V_{sg}, dI/dV values are enhanced by the process of Andreev reflection.[43] For very negative V_{sg}, a superconducting transition (I_s of a few nanoamps (nA)) is obtained despite the high temperature of the measurement (258 mK). For positive V_{sg}, the dI/dV drops

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because the transport is dominated by the tunneling current due to the decreasing transmission of the junction.[43]

We are interested in the tunneling regime at a high positive V_{sg}. Figure 4 (d) shows a color map of dI/dV, measured at 17 mK, as a function of V_{sd} and V_{sg}. We observe a region of suppressed dI/dV around $V_{sd} = 0$ (Figure 4 (e)), which is due to the presence of an induced superconducting gap centered around the Fermi energy. On the basis of the expected behavior of superconductor−insulator−superconductor tunnel junctions, the region of suppressed dI/dV should extend between $V_{sd} = -2\Delta^*/e$ and $V_{sd} = 2\Delta^*/e$, assuming the same Δ^* on both sides of the tunnel point contact. According to this hypothesis, we estimate $\Delta^* = 0.10$ meV.

Gate-dependent peak/dip structures can been seen outside the gap region. We attribute them to mesoscopic resonances associated with quasi-bound states in the channel on either side of the gate-defined middle barrier. Temperature and magnetic field evolution of the gap are available in Figure S4 of the Supporting Information.

In conclusion, this work provides ample evidence of gate-tunable induced superconductivity in a high-mobility 2DHG confined to a Ge QW. JoFET functionality in single junctions is corroborated by the observation of $h/2e$-periodic oscillations in the switching current of SQUID-type devices, which can find application in phase sensitive experiments.[42,44,45] Our device processing approach permits a direct contact between the Al-based superconducting electrodes and the Ge QW. The I_sR_n product, however, is small, suggesting low contact transparency. Efforts will be required to make better contact for quantum device application. In particular, the role of the Ge diffusion in the Al has to be better understood. Despite the low I_sR_n, we observe an induced gap comparable to the one of bulk aluminum. The size of the contacts could be further reduced to the 100 nm range, enabling ample versatility in device design. Finally, the developed contact scheme can be readily applied to other types of superconducting materials.

Fabrication Method. High mobility SiGe/Ge/SiGe heterostructures were grown by reduced pressure chemical vapor deposition (see Figure 1(a) for a cross-sectional diagram). Details on the growth process can be found in ref 38. Mesa structures have a typical of depth of 80 nm and lateral sizes in the micrometer width range. They are defined by electron-beam (e-beam) lithography and chemical wet etching in a solution of H_2O/HF(10%)/HNO_3(69.5%) at a ratio of 2:1:2.6.[46] Contacts are defined by e-beam lithography and e-beam evaporation of 20 nm of aluminum.[25] Argon plasma etching is used to remove the native oxide prior to metal deposition. Then, a dielectric layer of 30−40 nm of HfO_2 (Al_2O_3 for the side gate device) is deposited by ALD at a temperature of 250 °C. Finally, 10/25 nm of Ti/Au top gate is patterned by e-beam lithography followed by metal e-beam evaporation and lift-off.

■ ASSOCIATED CONTENT

Supporting Information

The Supporting Information is available free of charge on the ACS Publications website at DOI: 10.1021/acs.nanolett.8b04275.

Additional TEM analysis of a single-junction device, including high-angle annular dark-field scanning transmission electron microscopy and energy-dispersive spectroscopy; mean free path and Thouless energy estimation from Hall measurements on devices from a similar wafer; individual characterization of the two junctions of the SQUID device by differential resistance measurements versus top-gate voltage and current; additional measurements of the switching current evolution with magnetic field of the SQUID device with different gate configurations; and temperature and magnetic field evolution of the gap measured with the side gate device (PDF)

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Notes

The authors declare no competing financial interest.

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